Supplementary material

Room temperature two terminal tunnel magnetoresis-tance in lateral graphene transistor

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Materials and Methods

A - Graphene characterization

The quality of the CVD graphene utilized in this work can be observed by the huge flakes showed in the SEM image of Figure S1A and in the good results obtained from the electrical characterizations. In Figure S1B we present the electrical contacts developed by optical lithography and the zoom view of the Hall bar for the measurements, with defined graphene channel in Figure S1C. Fabrication processes is carefully described below. In Figure S1D is presented the resistance as a function of gate voltage while the very high mobility measured is shown in Figure S1E. Figure S1F displays the channel resistance as a function of temperature.

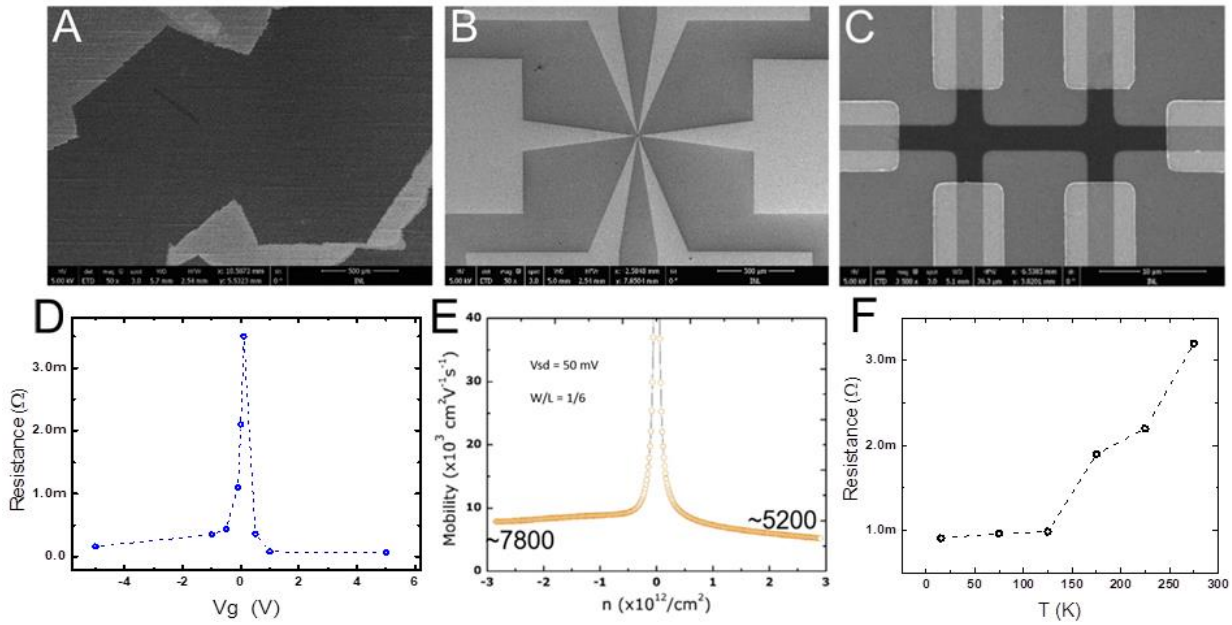

Figure S1 – Quality of the graphene layer: a) SEM image of graphene obtained after CVD process on copper, b) Hall bar device designed for CVD graphene electrical characterization, c) zoom view of defined graphene sheet channel, d) resistivity as a function of gate voltage, e) CVD graphene carrier mobility and f) evolution of graphene resistance as a function of temperature.

B - Device fabrication

The process described below is summarized in Figure S2. The stack $Ni_{81}Fe_{19}$ 100/CuN 50/Ta 5/CuN 50/Ta 5/Al_2O_3 100 (thicknesses in nm) is deposited on a 200 mm p-doped silicon wafer (Figure S2A). The process starts with a direct-write lithography step using 405 nm laser wavelength in a 600 nm thick photoresist AZ1505 (Figure S2B), to define the area of each device (Figure S2C).

A milling for 60s at 75° from normal is performed as a sidewall cleaning to remove redeposited materials, then photoresist is removed by plasma ashing (230 W, O_2:Ar 1:1, 0.6 mbar) for 780s. A second lithography step is performed to define the pillars, followed by ion milling for 540s until the milling process remove completely the Permalloy layer and etch

halfway the top copper nitride layer (Figure S2D). This etch keeps Permalloy on the pillar and removes it from the gate and from the contact lines, leading to a gate lower than the pillar level. The photoresist is removed by plasma.

A layer of SiO_2 with thickness of 295 nm as measured by optical interferometry is deposited by plasma-enhanced CVD as presented in Figure S2E and low angle ion milling planarization is performed up to the contacts be opened (Figure S2F).

A fifth lithography is realized in order to define a large contact area and then ion milling is performed for 600s, removing the silicon oxide until reach the copper nitride (Figure S2G). At this step, the tunnel barrier on top of the pillar is added (Figure S2H). For this, the wafer is first sputtered with 1.4 nm of $Al_{98.5}Si_1Cu_{0.5}$ (mass percentages) and then this layer is oxidized in plasma asher, using the same parameters as above for 360s. The graphene is then transferred onto the wafer according to the procedure described in detail below (Figure S2I).

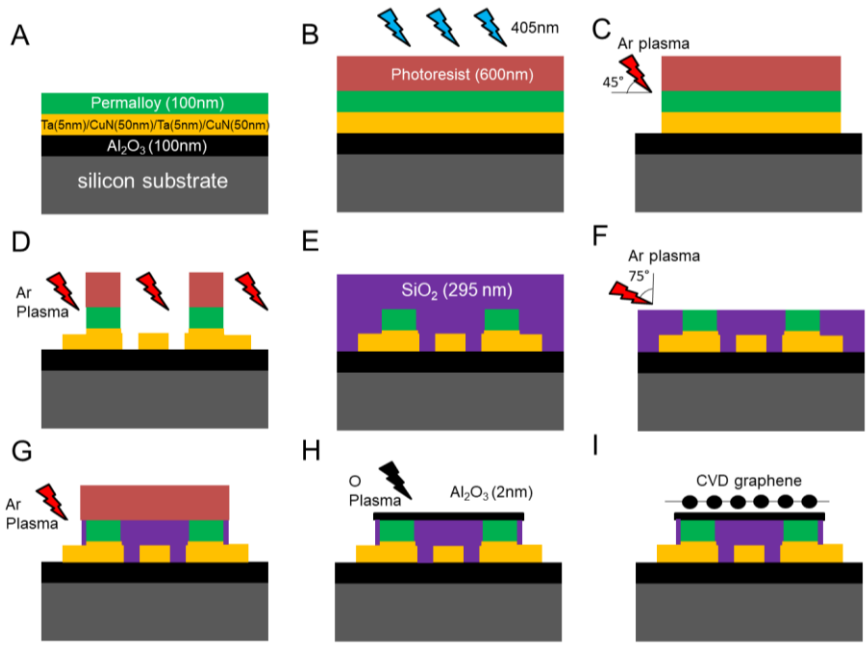

Figure S2 – Fabrication process: a) Layers deposition, b) photoresist spinning and sensibilization, c) definition of each device area, d) pillars definition by milling e) oxide deposition by CVD, f) planarization, g) electrical contacts definition, h) tunnel barrier deposition and i) graphene transference.

C - Transfer process

CVD graphene was grown on Cu foils. In order to transfer graphene onto the as-fabricated devices, short-chained polymethylmethacrylate (PMMA) mediated supporting layers were prepared for the low-residue transfer. The 3 wt% PMMA solution is a mixture of 2g PMMA-550k (Alfa Aesar, 43982) and 1g PMMA-15k (Sigma-Aldrich, 200336) powder dissolved in 97g anisole (Merck, 801452), which was treated by 24-hour stirring process using a magnetic stirrer with a magnetic follower at 1000 rpm. Because graphene grows on both sides of Cu foil, only the selected side of graphene/Cu foil was spin-coated with PMMA at 3000 rpm for 30 sec, following by drying PMMA/graphene/Cu foil in a chemical fume hood for 8 hr without baking. Graphene on the other side of the Cu foil without PMMA deposition was removed by oxygen plasma (4×10^{-1} mbar, 250 W, 90 seconds). PMMA/graphene/Cu foil was then placed over $FeCl_3$ etchant (0.5 M) for 1.5 hr. The PMMA-coated graphene was afterward rinsed 3 times in DI water and scooped up to a receiving substrate. Before removal of PMMA, the device covered by PMMA-coated graphene was ahead moved into a vacuum chamber which was evacuated down to the pressure of 1×10^{-4} Torr for 30 min. The purpose is to eliminate extra water and increase contact without additional thermal treatment. For PMMA removal, the entire sample was dipped into acetone bath over 3 hr. After that, the exposed graphene on the receiving substrate was dipped into isopropanol (IPA) and then DI water bath for 1 hr, respectively. Finally, the graphene on the device was blow-dried by N_2. The whole process was carried out in class-100 cleanroom.