Electronic Supplementary Material (ESI) for Nanoscale.
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Supporting Information for

# Floating Gate Negative Capacitance $MoS_2$ Phototransistor with High Photosensitivity

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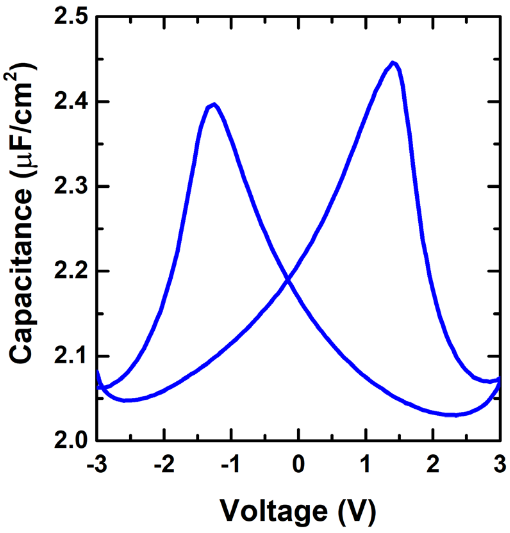
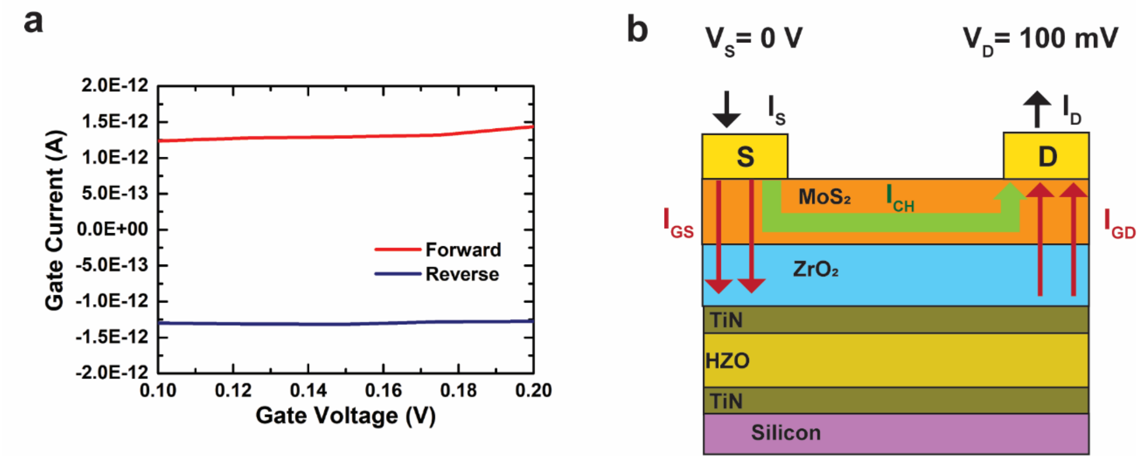


**Supplementary Figure 1.** Capacitance-voltage of MFM at 1kHz.



**Supplementary Figure 2.** (a) Gate current as a function of the gate voltage. (b) Schematic of current flow in the device.

In the low subthreshold region it is was found that $I_D < I_G$; therefore, reporting $SS_{min}$ in this region can misleading due to the contribution of the gate current to the measured drain current. In order to evaluate $SS_{min}$, we observed that in the region around $V_G = 0.1$ V, $I_G$ is constant as seen in Supplementary Figure 2a. The total current flow in the device is in Supplementary Figure 2b.

The total currents in this back-gated device[2] is:

$$I_G = I_{GS} - I_{GD}$$

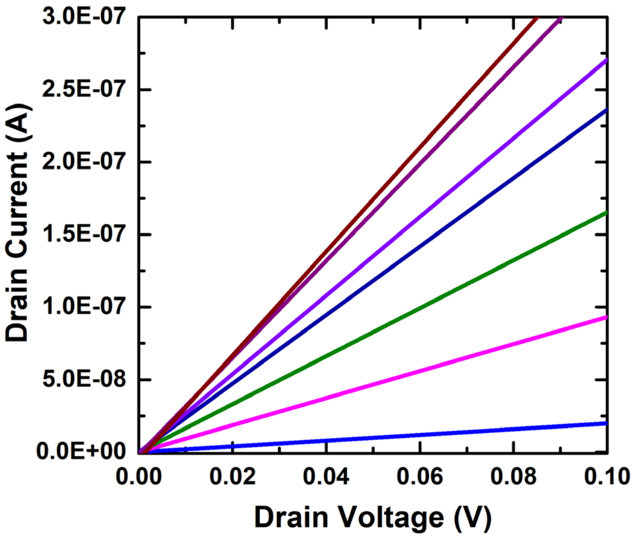
$$I_D = I_{ch} + I_{GD}$$
$$I_S = I_{ch} + I_{GS}$$

Since $I_G$ = constant, we make an approximation that $I_G$ can be divided into two equal parts where:

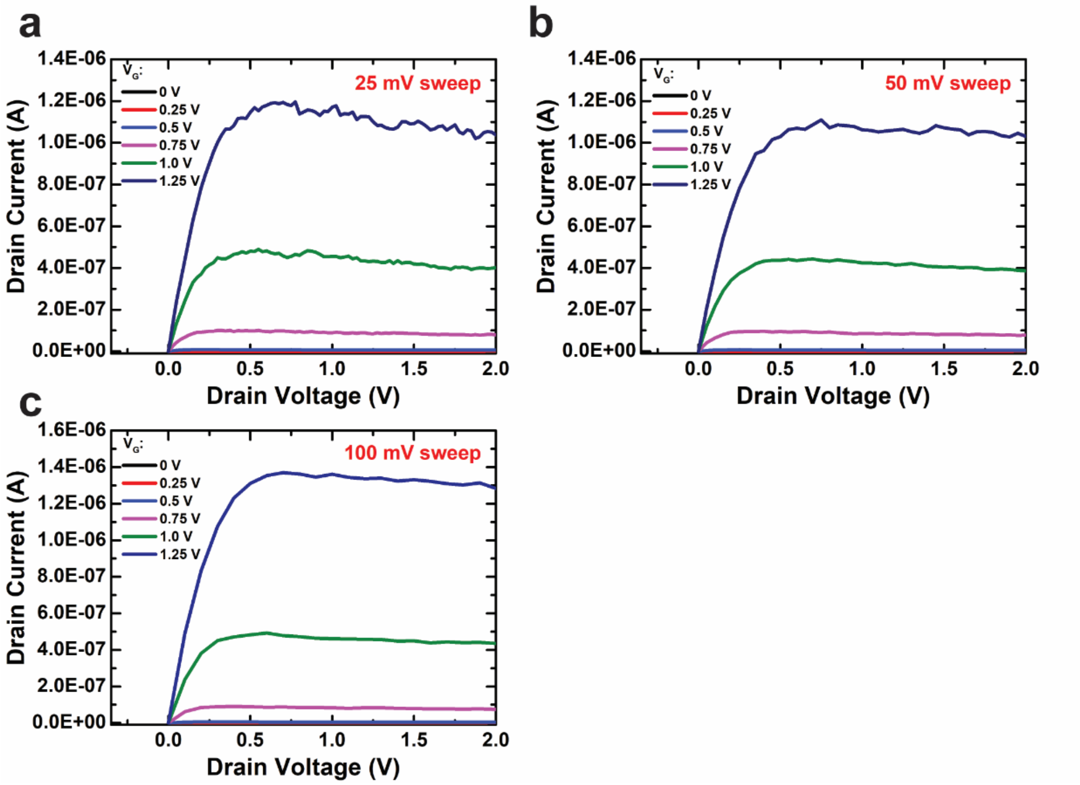
$$I_{GS} = 0.5{*}I_G$$
$$I_{GD} = 0.5{*}I_G$$

Therefore, the drain current without the contribution of the gate current in this region is determined from:

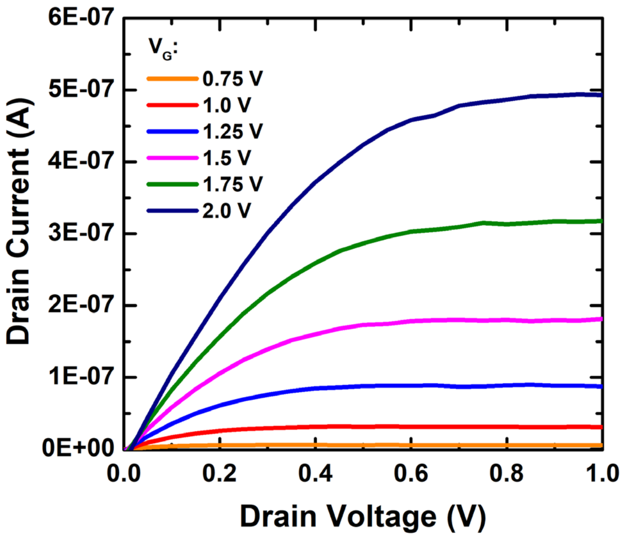
$$I_D = I_{D,measured} - 0.5{*}I_G$$



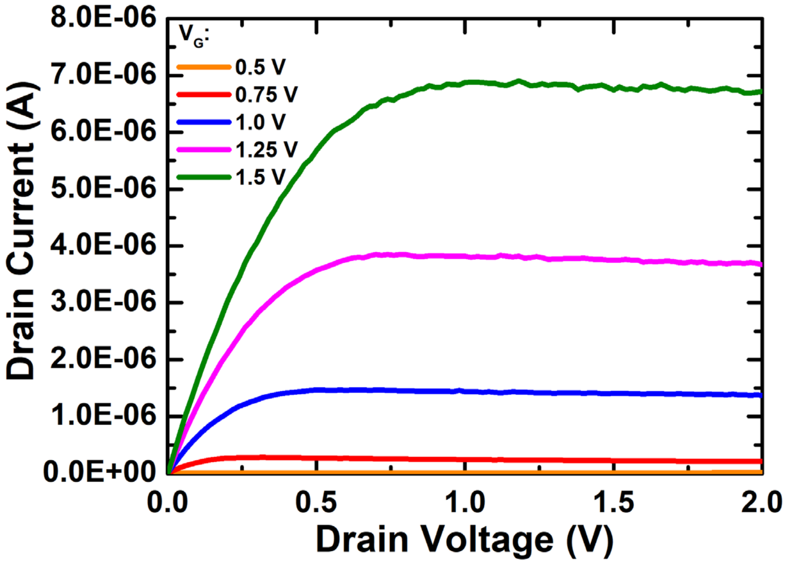
**Supplementary Figure 3.** Close up of dark condition $I_D$-$V_D$ at low drain voltages. The linear curves indicate ohmic-like contacts to monolayer $MoS_2$.



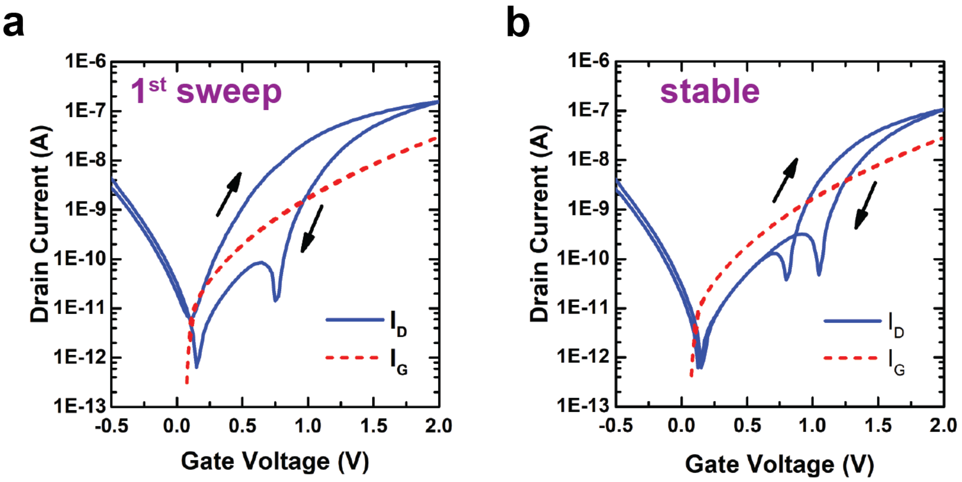
**Supplementary Figure 4.** Output characteristics of NCFG device with different drain voltage sweeps at (a) 25 mV, (b) 50 mV, and (c) 100 mV. This device measurement is from a different device from the result in the main article.



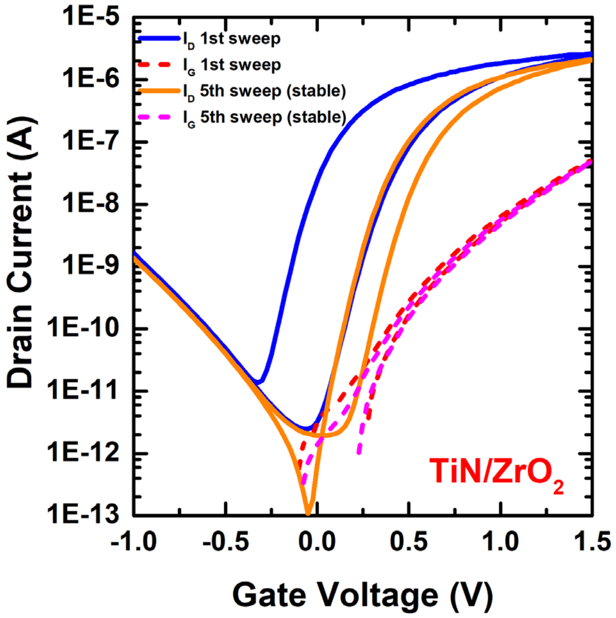
**Supplementary Figure 5.** Output characteristics of Si/$ZrO_2$ device under the dark condition.



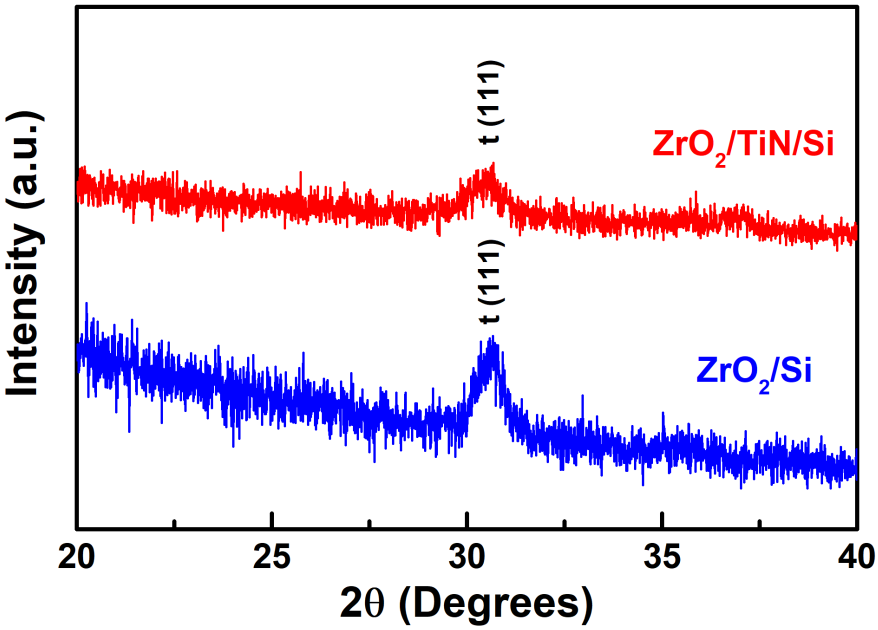
**Supplementary Figure 6.** Output characteristics of TiN-$ZrO_2$ device under the dark condition. The drain voltage sweep was at 20 mV.



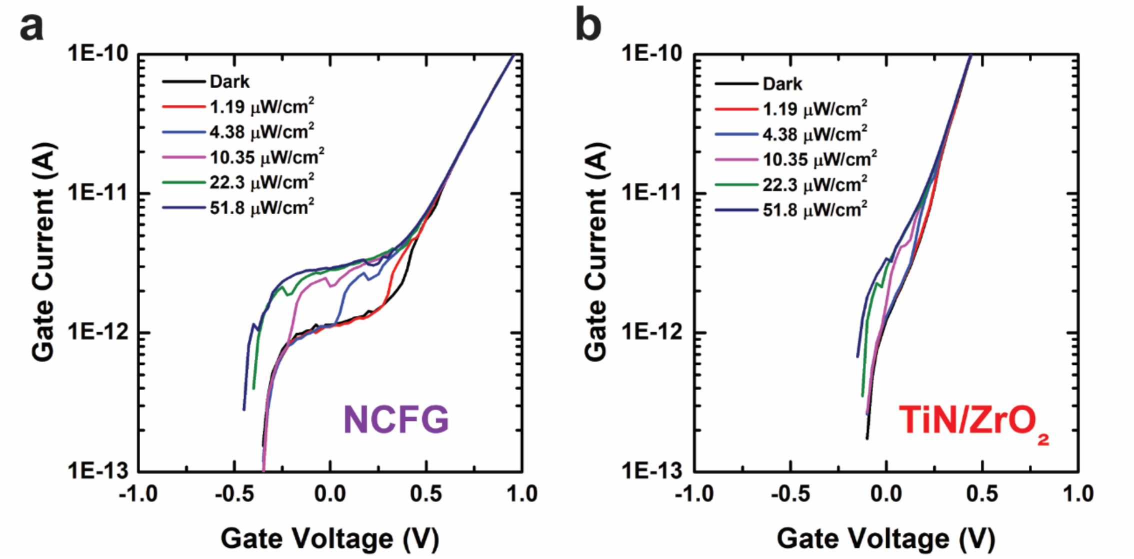
**Supplementary Figure 7.** Transfer characteristics of backgated device structure of Si/$ZrO_2$/$MoS_2$ with $V_{DS}$ = 150 mV. (a) After first $I_D$-$V_G$ sweep. (b) After a few $I_D$-$V_G$ sweeps, the transfer characteristics became stable; however, the $I_{on}/I_{off}$ ratio became lower.



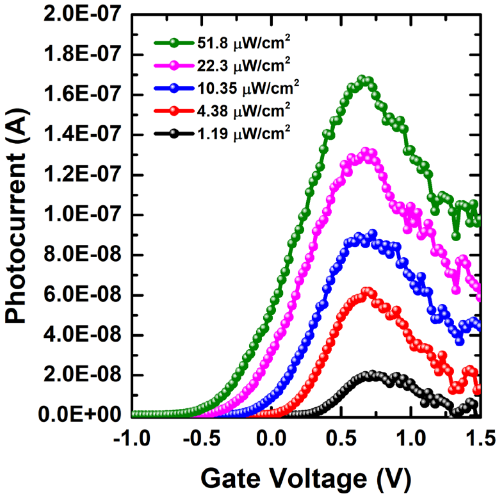
**Supplementary Figure 8.** Transfer characteristics of backgated device structure of Si/TiN/$ZrO_2$/$MoS_2$ including the first sweep and stable sweep.



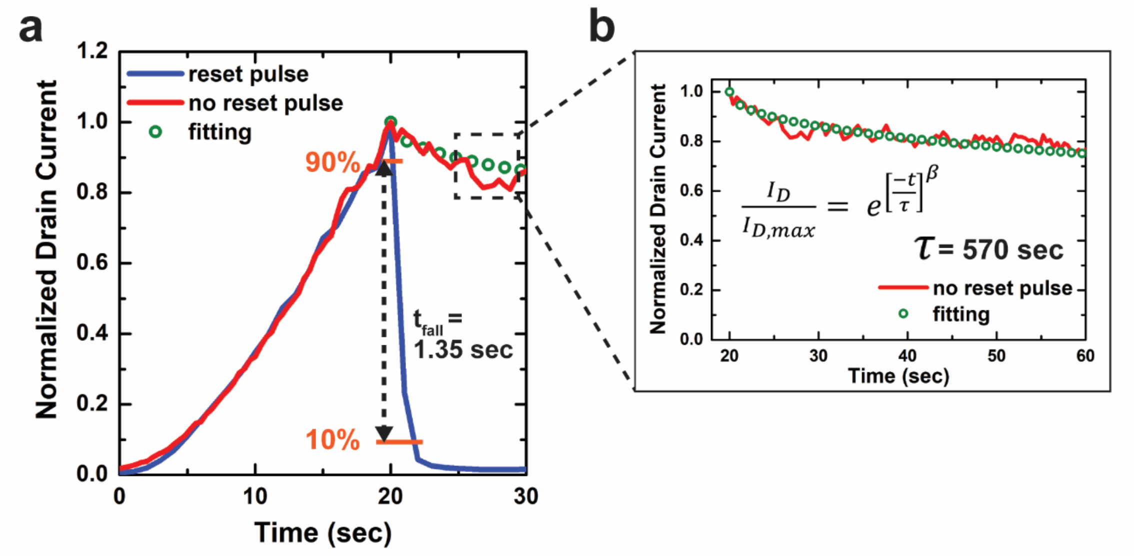
**Supplementary Figure 9.** XRD of $ZrO_2$ and TiN/$ZrO_2$ after ALD deposition at 300 °C with no post deposition annealing. Both films showed a small broad peak corresponding to the tetragonal (111) crystal phase at ~30.4° [2]; however, the $ZrO_2$ on Si showed a stronger peak intensity possibly indicating that this crystal growth is more preferable on a silicon interface rather than TiN at this deposition temperature. Overall, this result shows that the as-deposited ALD $ZrO_2$ thin film has at least one polycrystalline domain present.



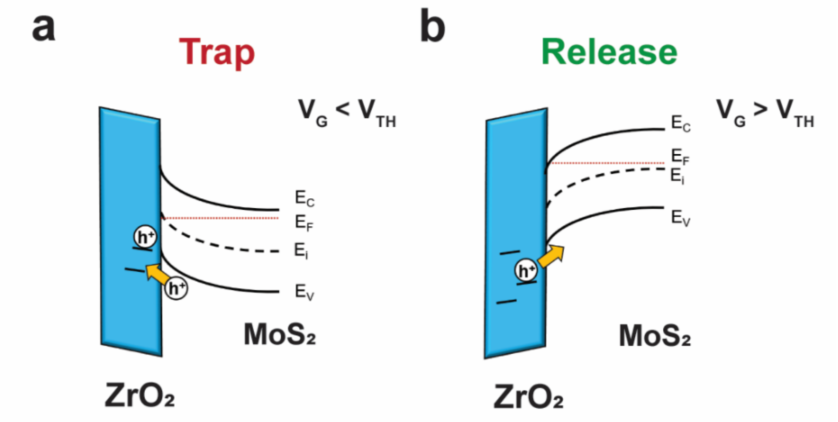
**Supplementary Figure 10.** Photoresponse of the gate current in (a) NCFG and (b) TiN-$ZrO_2$ device under green light illumination.



**Supplementary Figure 11.** Photocurrent as a function of the gate voltage at different optical power densities.



**Supplementary Figure 12.** Time response of the NCFG device under the application of a 20 second light pulse (optical power density of 10.35 μW/cm$^2$) with $V_G$ = -150 mV and $V_{DS}$ = 100 mV. (a) The red curve shows the intrinsic time response which displays the persistent photocurrent effect. The blue curve shows the improved fall time due to a 3 msec positive gate bias pulse. The green circle symbol line is the stretched exponential fitting to extract the time constant. (b) An extension of the persistent photocurrent decay and the stretched exponential fitting of the intrinsic time response. The extracted fitting parameters for $\beta$ and $\tau$ were 0.47 and 570 seconds respectively.



**Supplementary Figure 13.** $ZrO_2$ trap/release mechanism overview based on gate biasing. (a) Under depletion mode gate biasing, photogenerated holes get trapped into $ZrO_2$ occupying oxide trap levels. (b) When applying a positive gate bias pulse, trapped charges are released.

**References:**

[1] V.K. Singh, B. Mazhari, AIP Advances, 2011, 1, 042123.

[2] J.-K. An,N.-K. Chung, J.-T. Kim, S.-H. Hahm, G. Lee,S. B. Lee, T. Lee, I.-S. Park, and J.-Y. Yun, Materials 2018, 11, 386.