Supporting Information

Artificial Synaptic Transistor using α- In_2Se_3Van der Waals Ferroelectric Channel for Pattern Recognition

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Supporting Note 1

Sample preparation for Transmission Electron Microscopy (TEM) analysis

A 0.03g bulk sample of In_2Se_3 crystal was dissolved in 10 ml of Isopropyl alcohol (IPA) followed by ultrasonication at 8000 rpm for 8 hours. The resultant solution was further diluted in 30 ml IPA to get the desired concentration. The solution obtained was drop-casted onto a plasma cleaned PELCO carbon-supported copper grid and dried under an IR lamp for 12 hours. The resultant film was micro graphed under a 300 kV illumination on a FEI Titan Themis Transmission Electron Microscope.

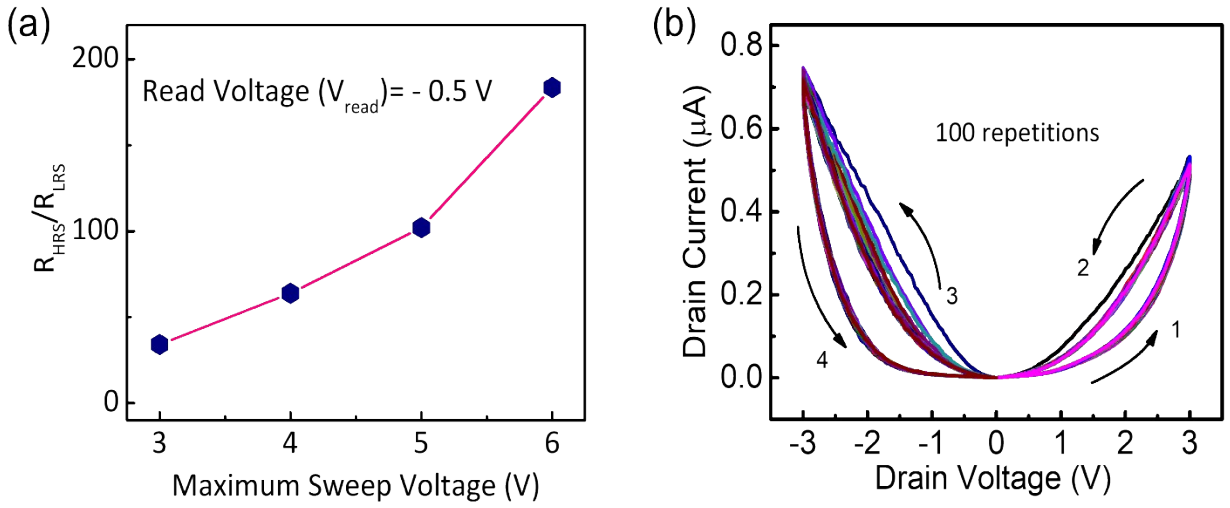

Figure S1. Extended data on electrical characteristics for two-terminal (metal-In_2Se_3-metal configuration geometry) measurements. (a) The resistance switching ratio for the maximum sweep voltage for (-3V to -6V). As the voltage applied to the drain terminal increases, it leads to a higher switching ratio between LRS to HRS. (b) Multiple sweep cycles measured for 100 sweep cycles.

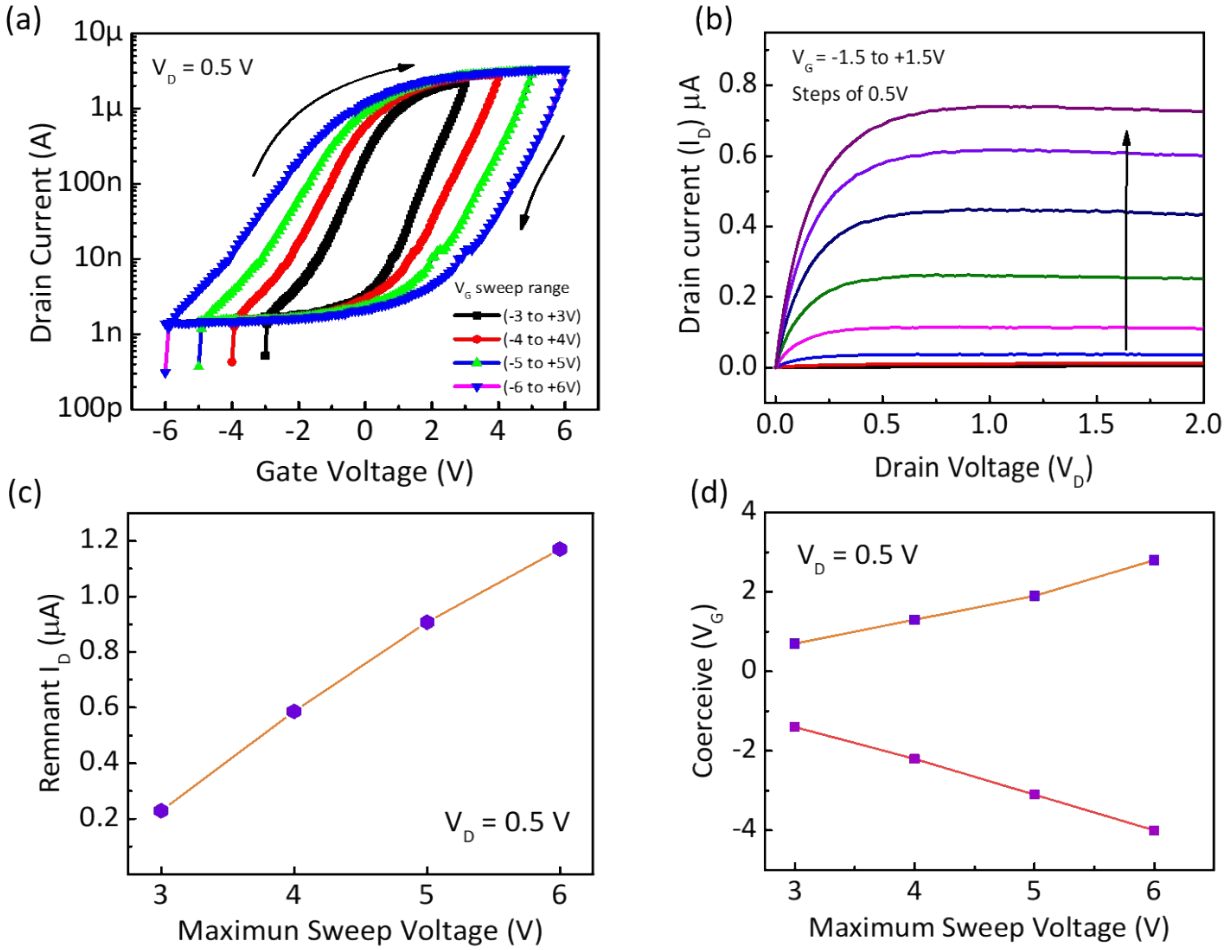

Figure S2. Extended electrical characteristics of α-In_2Se_3 based FeS-FET. (a) I_D-V_G curve for multiple gate sweep range from (±3V to ±6V). We note that increasing the voltage range results in an increased hysteresis window which can be attributed to more orderly polarization of the channel layers. (b) I_D-V_D characteristic curve at room temperature with channel length 2 microns and flake thickness 50 nm. The output characteristics were measured for the V_{ds} range of 0 to 2 V with a different V_G from -1.5 to 1.5 V, displaying a significant gate-modulated effect. (c) Remnant current as a function of gate voltage sweep from (3V to 6V). (d) Coercive V_G (at I_D = 10 nA/µm) as a function of maximum sweep V_G on the same device.

Low temperature measurement and Ferroelectricity:- Multiple authors have shown that the α-phase of In_2Se_3 is known to be ferroelectric at room temperature[2,3]. In general, the clockwise hysteresis in transfer characteristics of a FET is associated with charge trapping at the interface of oxide and semiconductor. To prove the ferroelectricity of the above devices under study, low temperature measurements were studied on devices with clockwise hysteresis loop. Since it is well known that charge trapping is associated with thermal activation and has strong temperature dependence, at low temperature the hysteresis window decreases[1]. The FET under study with 50 nm flake thickness show similar hysteresis window at room temperature and low temperature of (200 K and 300 K) which can be ascribed to its ferroelectricity.

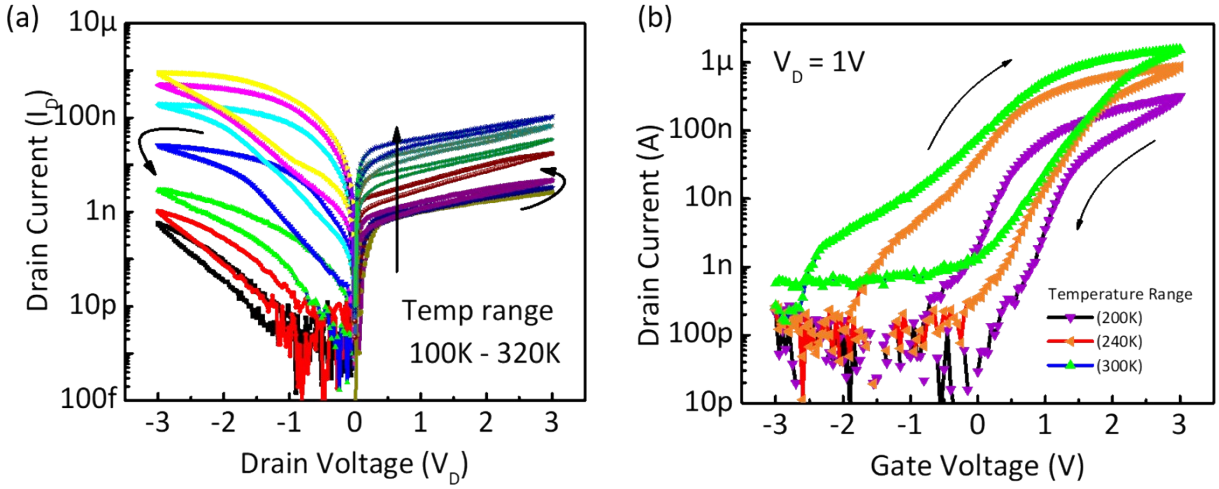

Figure S3. (a) Temperature dependence of the hysteresis loops for output characteristics for a planar α-In_2Se_3 memristor at V_G = 0V. (b) Temperature dependence of the hysteresis in the transfer characteristics at V_{ds} = 1V.

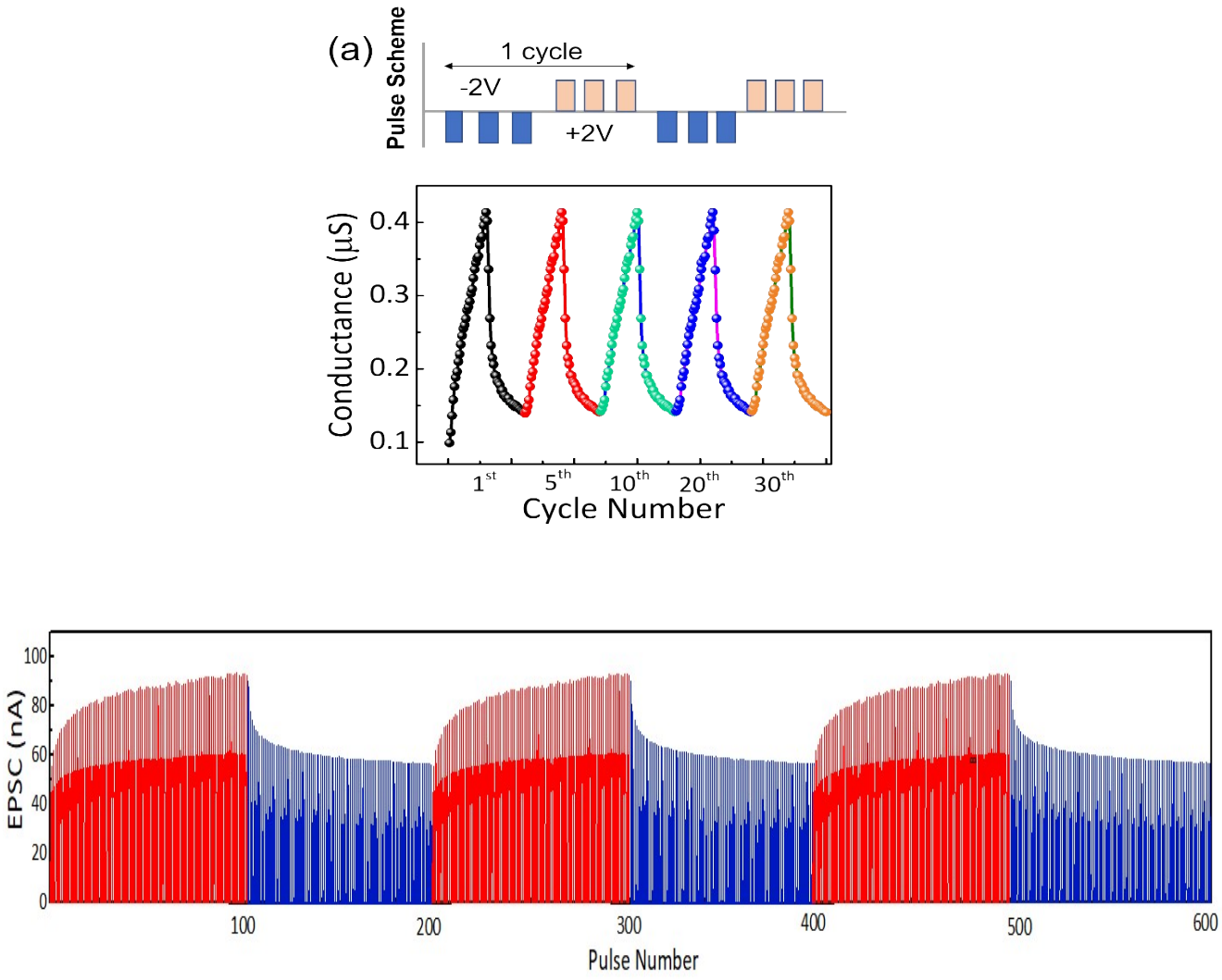

Figure S4. Top part shows the pulse scheme applied at the back-gate terminal of the In_2Se_3 synaptic transistor. (a) Endurance characteristics of the proposed FeS-FET for 30 potentiation and depression cycles at the gate terminal. (b) 100 excitatory and inhibitory pulses of amplitude -2V and +2V applied on the gate terminal respectively for 600 pulses.

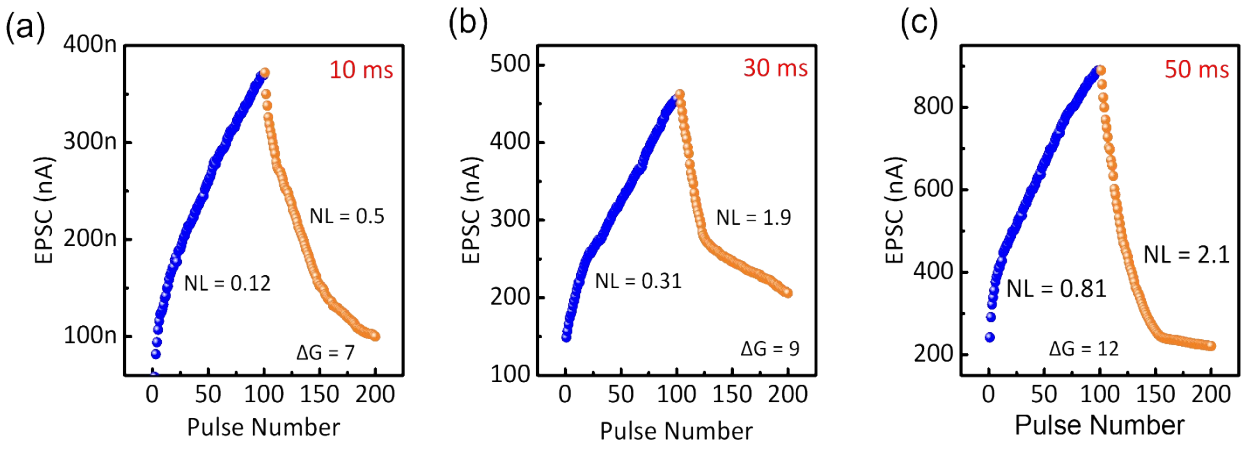

Figure S5. Potentiation and depression for 100 sequential pulses at different pulse widths: (a) 10 ms with NL_LTP (0.12) and NL_LTD (0.5) and ΔG (7). (b) 30ms with NL_LTP (0.31) and NL_LTD (1.9) and ΔG (9) (c) 50ms with NL_LTP (0.81) and NL_LTD (2.1) and ΔG (12) respectively.

Supplementary Note 2: Number of stable conductance states above threshold: -

In order to show we have achieved more than 64 states stable conductance states, we applied 100 excitatory pulses of (10 ms and 2V) on gate terminal as shown in figure (a). The value of conductance state at each pulse is increasing in linear fashion, with few conductance states being either overlapping or less than the previous pulse value. To avoid this overlap, we extracted the stable conductance states by setting threshold value for ΔG. The effective stable conductance states were extracted using (G_N -G_{N-1}) conductance weight values when the difference between G_1 and G_2 exceeds a certain threshold. Here G_1 and G_2 are conductance weight values from pulse1 and pulse2, respectively. A threshold of 0.2%, 0.3% and 0.5% was used to extract the stable weight values from 100 pulses. Figure (b) shows the extracted values of three different cases, corresponding to N_{states} = 10 (case-1), N_{states} = 20 (case-2) and N_{states} = 64 (case-3), to identify its impact on pattern recognition.

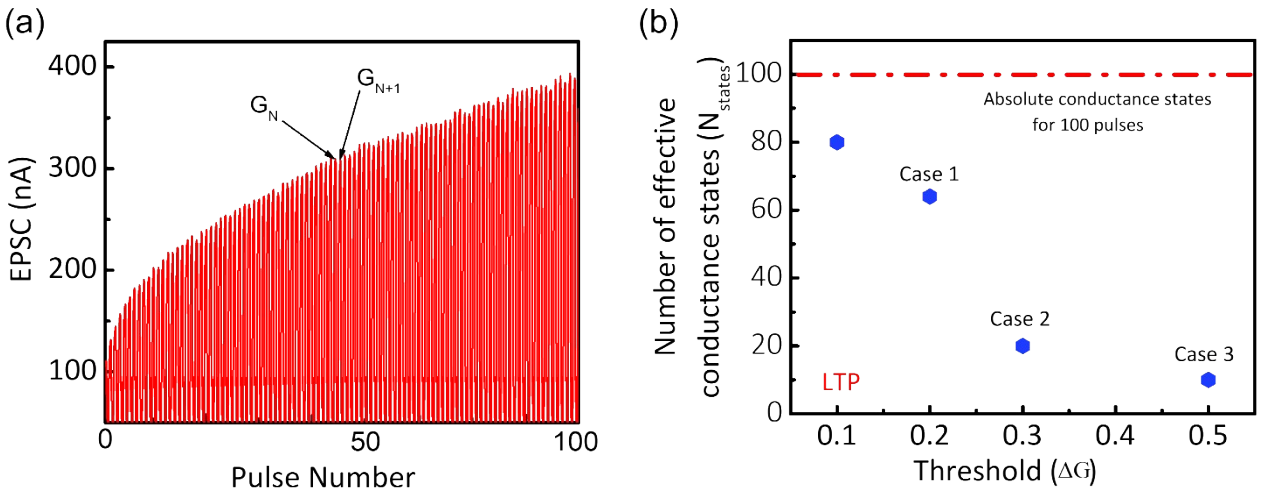

Figure S6. (a) Potentiation responses of the channel to 100 sequential pulses at V_{LTP} of -2V and 10 ms. The current values at individual pulse represents one conductance weight state. (b) Extracted stable conductance states value at different threshold voltages.

Supplementary Table 1. Extracted values of linear transfer coefficient ‘A’ and ‘B’ for different conductance states

Weight states	A_1	A_2	B_1	B_2
N_{states} = 10	2.681×10^6	7.304×10^6	-0.5473	-1.5083
N_{states} = 20	2.139×10^6	2.201×10^6	-0.6608	-2.4067
N_{states} = 64	6.557×10^6	2.444×10^6	-0.687	-2.5042

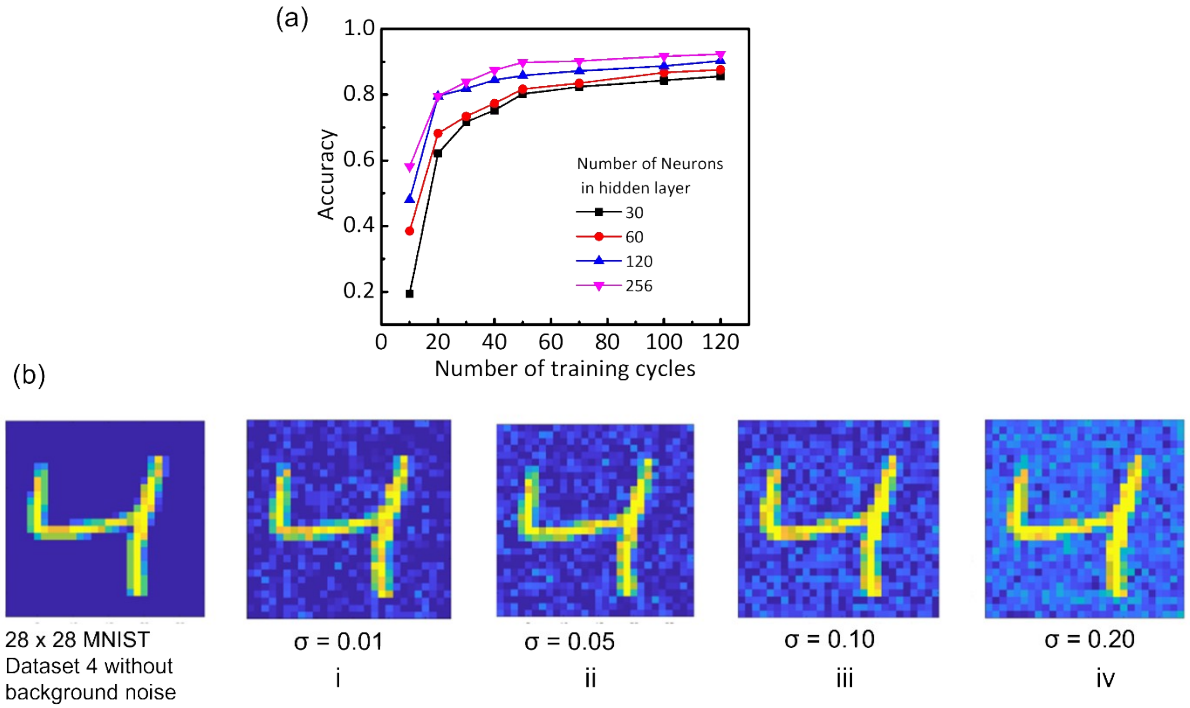

Figure S7. (a) Recognition accuracy for different numbers of hidden neurons (30, 60,120 and 256) as a function of training cycles. Increasing the number of neurons in the hidden layer increases the recognition accuracy with each epoch cycle. (b) (i-v) Numerical digit 4 represents different % of variance introduced as background noise pixels for calculating the classification accuracy. Introducing of background noise leads to difficulty in convergence state of conductance weight value, thus showing strong fault tolerant nature of the obtained conductance weights from the FeS-FET.

References: -

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