Electronic Supplementary Information (ESI)

Synaptic Transistors with Human Brain-Like fJ Energy Consumption via Double Oxide Semiconductors Engineering for Neuromorphic Electronics

Seong-In Cho,^a Jae Bum Jeon,^a Joo Hyung Kim,^a Seung Hee Lee,^a Wooseok Jeong,^a Jingyu Kim,^a Geunyoung Kim,^a Kyung Min Kim,^{*a} and Sang-Hee Ko Park ^{*a}

^a Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Dae-hak ro, Yuseong-gu 34141, Republic of Korea

E-mail: Kyung Min Kim: <u>km.kim@kaist.ac.kr</u>, Sang-Hee Ko Park: <u>shkp@kaist.ac.kr</u>

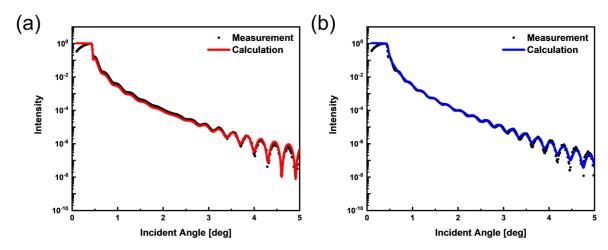


Fig. S1 XRR results of PEALD SiO₂ deposited at (a) 200 and (b) 300 °C.

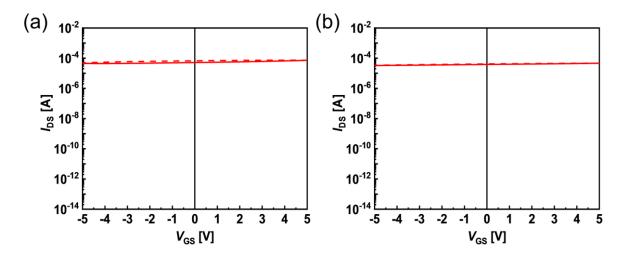


Fig. S2 Transfer curves of top-gate IZO TFTs with (a) 30 nm and (b) 60 nm of PEALD SiO₂ GI deposited at 200 °C without H barrier. ($V_{DS} = 0.1$ V) Solid lines represent forward sweeps and dashed lines represent back sweeps.

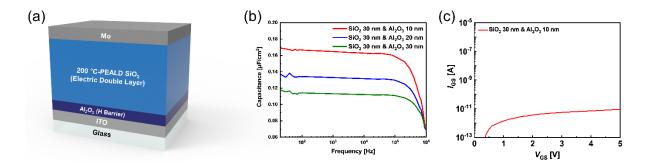


Fig. S3 (a) Schematic of MIM device with both a SiO₂ EDL and an Al₂O₃ H barrier. (b) Results of C-F measurements of these MIM devices. (c) Gate leakage current of synaptic transistor with 30-nm SiO₂ EDL and 10-nm Al₂O₃ GI.

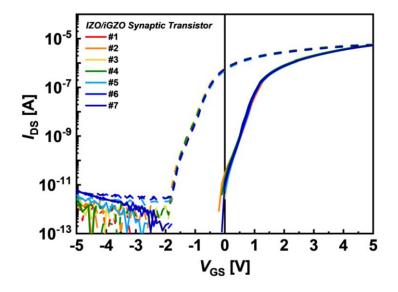


Fig. S4 Uniformity of transfer curves of IZO/IGZO synaptic transistors ($V_{DS} = 0.1V$). Solid lines represent forward sweeps and dashed lines represent back sweeps.

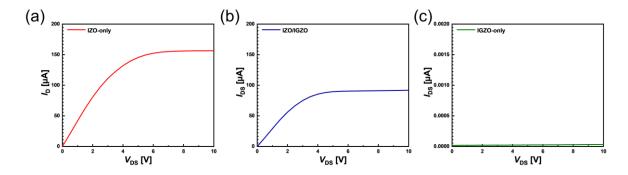


Fig. S5 Output curves of (a) IZO-only, (b) IZO/IGZO, and (c) IGZO-only synaptic transistor (V_{GS} = 3.5 V).

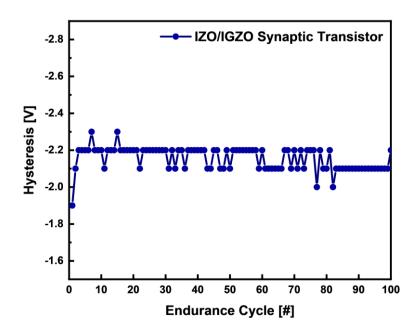


Fig. S6 Hysteresis window of IZO/IGZO synaptic transistor according to the number of endurance cycles.