Supplementary Information for:

Multi-functional Logic Circuits Composed of Ultra-thin Electrolyte-gated Transistor with Wafer-scale Integration

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1. Fabrication procedure of the top-gated EGTs

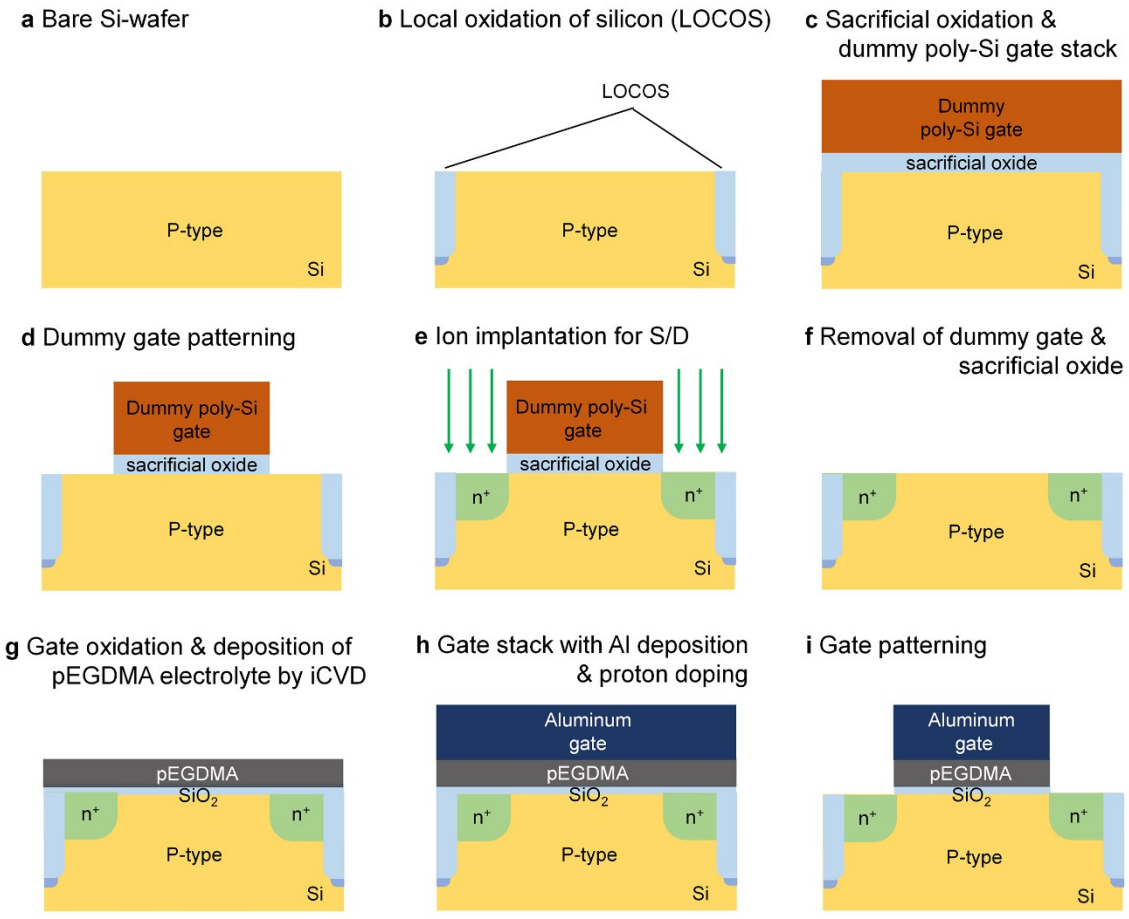

Figure S1. Process flow for the fabrication of the the top-gated EGTs using a gate-last process.

The fabrication procedure of the top-gated EGTs using a gate-last process is illustrated in **Figure S1**. A pEGDMA electrolyte is an all-solid-state film, and accordingly the EGTs were fabricated as a top-gate structure, which can allows individual access to each gate for various logic functions. The starting material for the EGTs is a p-type 4-inch bulk silicon wafer with a crystal orientation of (100) (**Figure S1 a**). Local oxidation of silicon (LOCOS) was ultilized for device-to-device isolation by wet oxidation. The thermally grown field-oxide thikness after the LOCOS was 1 μm (**Figure S1 b**). A sacrificial oxide and a dummy gate composed of poly-crystalline silicon (poly-Si) were sequentially stacked and patterned. The patterned

dummy gate was used as an implant stopper to avoid counter-doping of the p-type body during phosphorus (P) implantation for the n^+ heavily doped source and drain (S/D) (**Figure S1 c & d**). The ion implantation condition for the P doping is a dose of 5×10^{15} cm^{-2} and an energy of 50 keV (**Figure S1 e**). After removal of the disposable dummy gate and the sacrificial oxide, thermal gate oxidation was applied to form an interface layer (SiO_2) between the Si-channel and the pEGDMA electrolyte. Its thickness was 2 nm. Right after the gate oxidation, the pEGDMA was deposited using iCVD (**Figure S1 f & g**). Afterwards, aluminum for the gate electrode was deposited by DC magnetron sputter. Meanwhile, protons from moisture in the air were naturally introduced inside the sputtering chamber, then the chamber pressure was decreased down to 5 mTorr prior to the Al sputteing (**Figure S1 h**)[1]. The stacked aluminum gate, pEGDMA, and interface SiO_2 were sequentially patterned by aluminum etchant (APAL-1), O_2 plasma, and 2% of hydrofluoric acid (HF), respectively (**Figure S1 i**).

2. Measurement configuration of logic inverter, NAND, and NOR gates

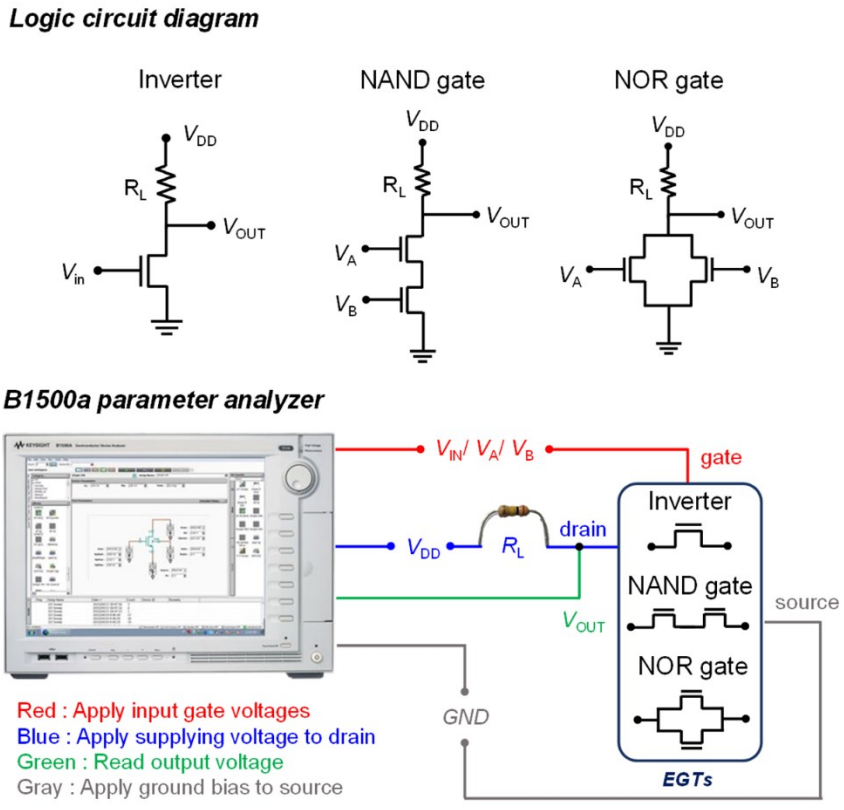

Figure S2. Details of the measurement setup used to characterize the logic circuits: inverter, NAND and NOR gates.

Figure S2 shows the measurement setup for the inverter, NAND, and NOR logic elements. They are composed of one or two fabricated EGTs. In the logic inverter, the gate of the EGT is connected to an input node with an applied voltage of V_{IN}, one end of the load resistor (R_D) is biased with V_{DD}, the other end of the load resistor is tied to the drain of the EGT which is an output node biased with V_{OUT}, and the source of the EGT is biased with ground (*GND*). On the other hand, the NAND and NOR gates use two EGTs, which are serially or parallelly connected with two input voltages (V_A, V_B), respectively. Detailed voltage nodes are depicted in **Figure S2**. V_{IN}, V_{DD} and *GND* were supplied from a B1500a semiconductor parameter analyzer. It can also measure V_{OUT} from the common drain electrode of each logic gate.

3. Voltage transfer curve (VTC) and maximum voltage gain (V_{GAIN}) according to load resistance (R_L)

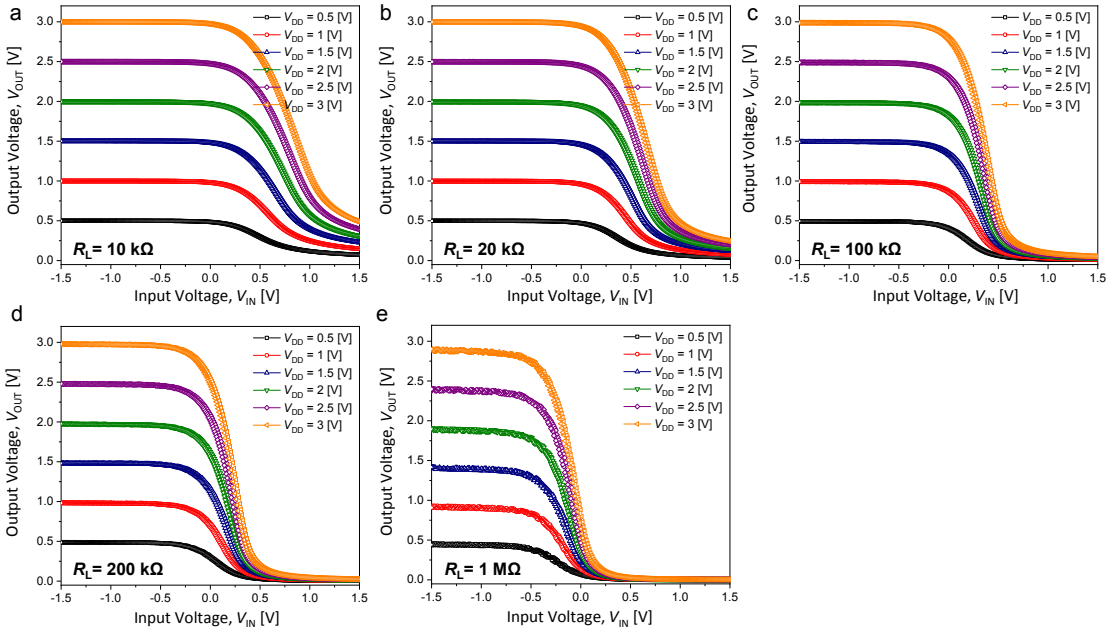

Figure S3. VTC according to various R_L from **(a)** 10 kΩ to **(e)** 1 MΩ.

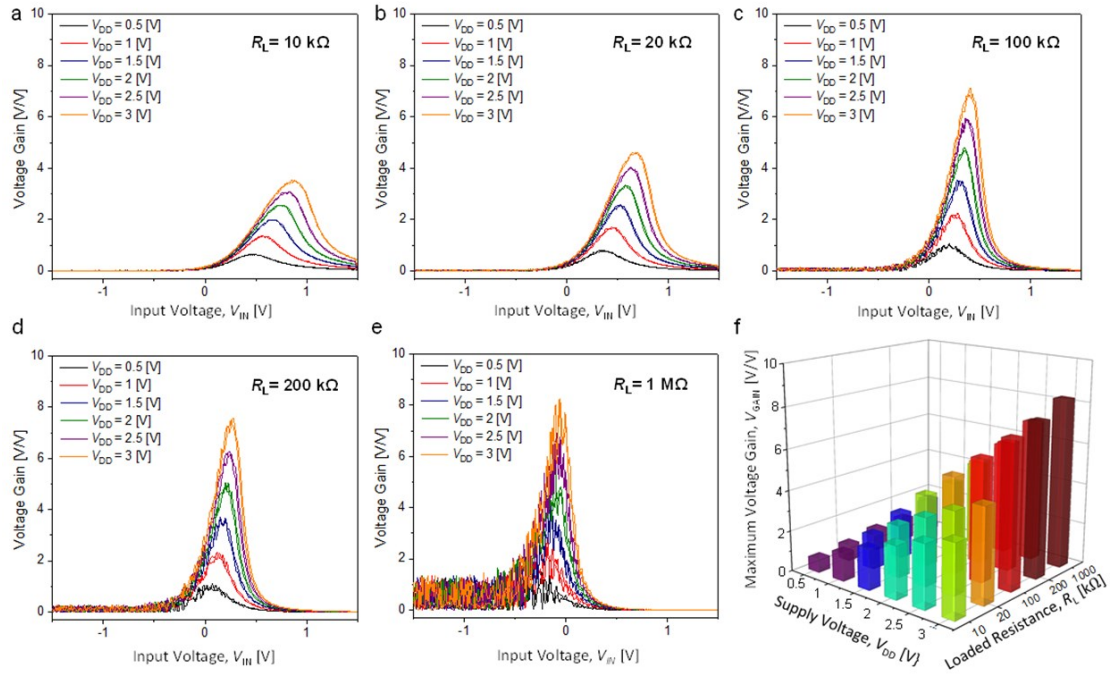

Figure S4. Plot of voltage gain (V_{GAIN}) according to various R_L from **(a)** 10 kΩ to (e) 1 MΩ. **(f)** Maximum V_{GAIN} versus V_{DD} and R_L. **f**

For the RLI, the voltage transfer curves (VTC) for various R_L are shown in **Figure S3**. Voltage gain (V_{GAIN}), defined as $V_{GAIN} = -\partial V_{OUT}/\partial V_{IN}$, is also plotted for various R_L in **Figure S4**. As the R_L is increased, the V_{GAIN} is increased. In the case of R_L =1MΩ, an oscillation was found in the VTC and the plot of V_{GAIN}, when V_{OUT} is high. This is because the high R_L becomes comparable to the channel resistance (R_{CH}) of the EGT in the off-state. This provoked the oscillation of I_{OFF} in the EGT, as well.

4. Dynamic output characteristics of the resistor-loaded inverter (RLI) from 1 Hz to 1 kHz

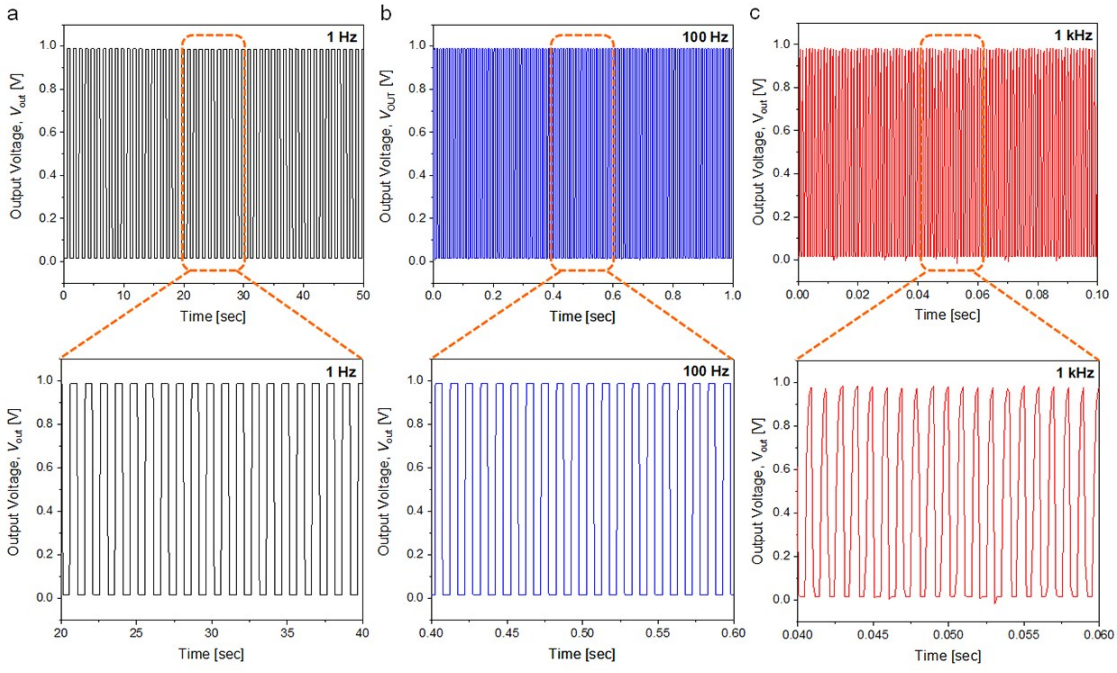

Figure S5. Dynamic output characteristics of the RLI with optimized load resistance (R_L=200 kΩ). Applied input frequency is from (a) 1 Hz to (c) 1 kHz.

Dynamic output voltage (V_{OUT}) characteristics of the RLI driven by the oscaillating rectangular-shaped V_{IN} from 1 V to -1 V with a frequency of 1 kHz, were plotted for elapased time in the upper row of

Figure S5. A close-up view of the oscillating V_{OUT} was also shown in a lower row in **Figure S5**. Note R_L=200 kΩ, which is connected to the drain of the fabricated EGT.

References

[1] X. Ma, J. Zhang, W. Cai, H. Wang, J. Wilson, Q. Wang, Q. Xin & A. Song., A Sputtered Silicon Oxide Electrolyte for High-Performance Thin-Film Transistors. *Sci. Rep.* **7**, 809 (2017).