Electronic Supplementary Materials

For

Fully-Printed Flexible Tin Oxide Thin-Film Transistors and Logic Circuits

Kun Liang,[a,b] Huihui Ren,[a,b] Dingwei Li,[a,b] Yan Wang,[b] Yingjie Tang,[b] Momo Zhao,[b,c] Hong Wang,[c] Wenbin Li,[b,d] and Bowen Zhu[b,d*]

a. Zhejiang University, Hangzhou 310027, China.
b. Key Laboratory of 3D Micro/Nano Fabrication and Characterization of Zhejiang Province, School of Engineering, Westlake University, Hangzhou 310024, China.
c. Key Laboratory of Wide Band Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an 710071, China.
d. Institute of Advanced Technology, Westlake Institute for Advanced Study, Hangzhou 310024, China.

*Email: zhubowen@westlake.edu.cn

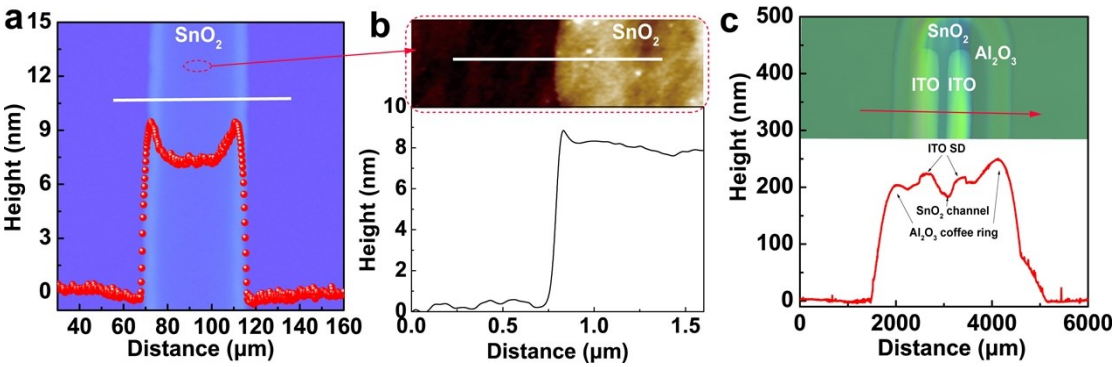

Fig. S1. Height profiles of printed SnO_2 films and TFTs. (a) Optical image and height profile of printed SnO_2 channel. The height was measured by a surface profilometer. (b) AFM image and corresponding height profile of printed SnO_2 film in the central area of the (a). (c) Stylus profilometer scan of the fully-printed SnO_2 TFT. The red arrow indicates scanning direction.

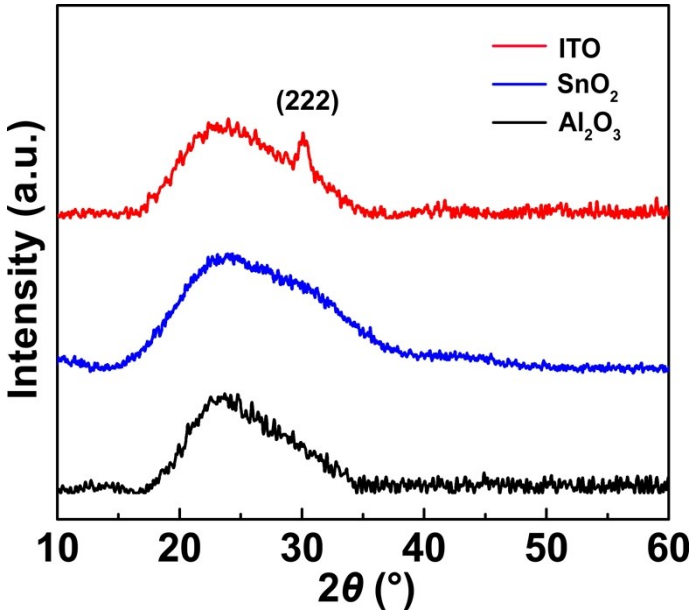

Fig. S2. XRD patterns of the ITO, SnO_2, and Al_2O_3 films on glass substrate. The diffraction peaks of the ITO film on the (222) crystal plane indicate its polycrystalline structure. No obvious diffraction peaks could be observed in SnO_2 and Al_2O_3 films. The samples were prepared by spin-coating of the same precursor ink solution and annealing condition as printed films.

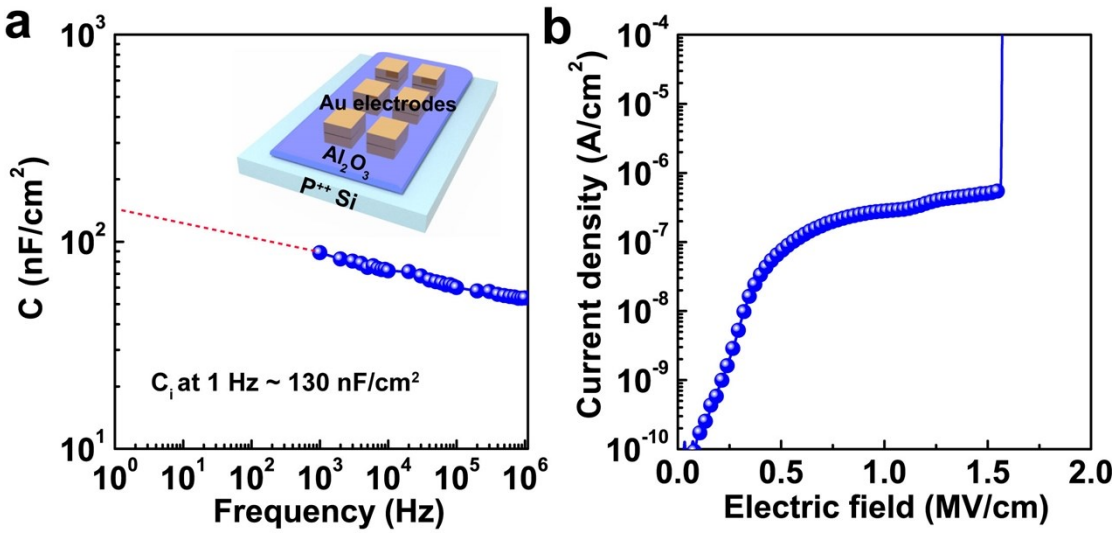

Fig. S3. Electrical properties of printed Al_2O_3 dielectric film. (a) Areal capacitance-frequency curve of printed Al_2O_3 film measured with a metal-insulator-metal (MIM) structure, with Au and highly doped Si (p^{++}) as the top and bottom electrodes, respectively. The areal capacitance value of the Al_2O_3 dielectric (C_i) was ~130 nF cm^{-2} extrapolated to 1 Hz. (b) Leakage current density of the MIM structure as a function of applied electric field.

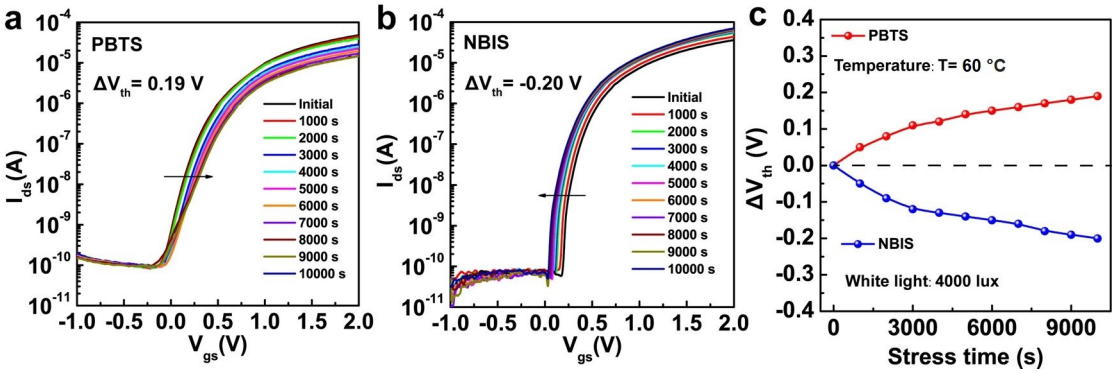

Fig. S4. Evolution of transfer curves of the fully printed SnO_2 TFTs as a function of (a) PBTS and (b) NBIS. (c) Threshold voltage shifts (ΔV_{th}) as a function of bias stress time. The PBTS test was carried out in air at 60 °C for 10000 s, and the applied gate bias was 1 V. The NBIS was performed in air at room temperature under white LED light illumination (4000 lux), and the applied gate bias was -1 V.

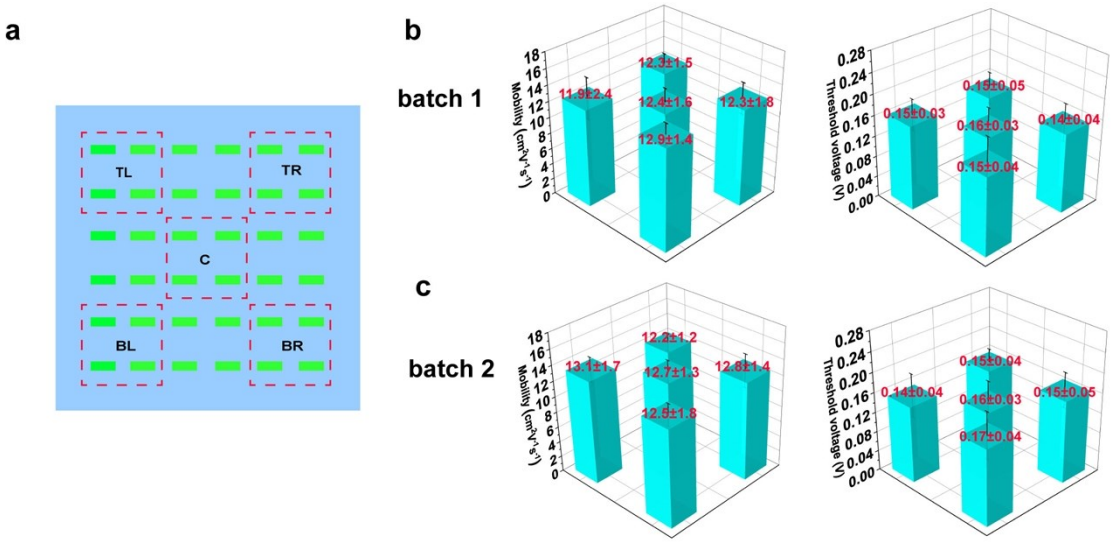

Fig. S5. Probabilistic histograms of the mobility (μ_{sat}) and V_{th} values of 80 printed devices from 4 sample substrates (fabricated from 2 batches, each batch contains 2 sample substrates). (a) Devices located at 5 different areas in each substrate were measured: top left (TL), top right (TR), bottom left (BL), bottom right (BR), and center area (C). 4 TFTs at each area were measured. In total, the parameters from 80 TFTs were collected (4 substrates × 5 area × 4 devices). (b-c) Average μ_{sat} and V_{th} values from two batches, showing high uniformity with deviations less than 10%.

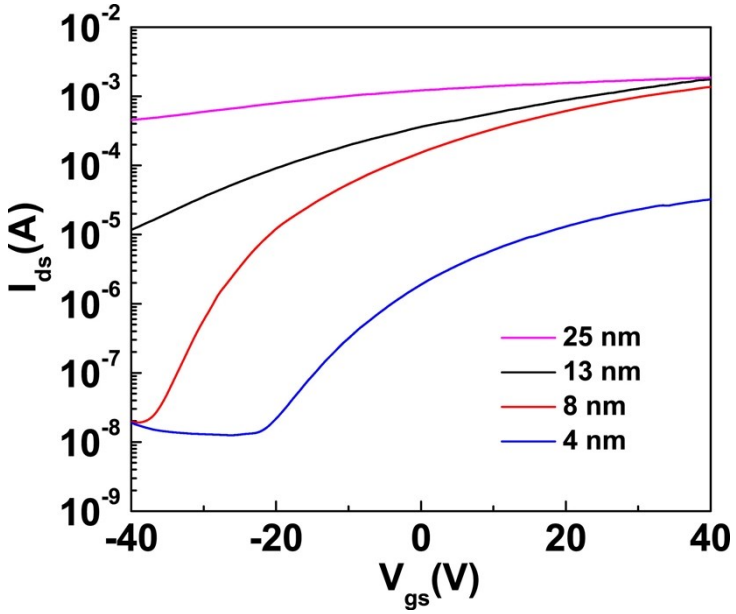

Fig. S6. Transfer curves of SnO_2 TFTs with different channel thicknesses fabricated on Si substrate with 100 nm thick SiO_2 gate dielectric.

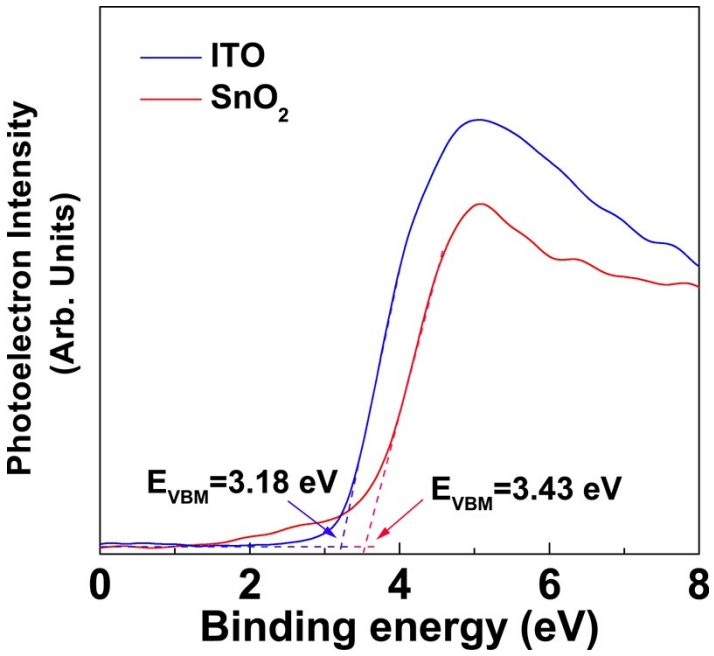

Fig. S7. Valence band spectra of ITO and SnO_2 films.

Table S1. Electrical properties of SnO_2 TFTs with SiO_2 gate dielectric.

SnO_2 thickness (nm)	μ_{sat} ($cm^2\ V^{-1}\ s^{-1}$)	V_{th} (V)	*SS* ($V\ dec^{-1}$)	I_{on}/I_{off}
4	0.3	-11.4	6.8	2.5×10^3
8	6.8	-20.2	4.4	9.2×10^4
13	/	/	/	/
25	/	/	/	/