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Supporting Information

Organic Synaptic Transistor with Integration of Memory and Neuromorphic Computing

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1. Electrical characteristics of the BPQDs blended devices.

To investigate the conventional memory performance, which is different from the demonstrated memory in synapse in our work, the transfer characteristics curves of the pristine and blended devices were measured by applying appropriate gate voltage pulse

for programming and erasing operation. **Figure S1** shows the positive and negative transfer characteristics curves shifts of devices by applying programming pulse (+20 v,1 s) and erasing pulse (-20 v,1 s) respectively. It should be noted that the memory window, which is defined as the difference ΔV_{TH} of threshold voltages between positive and negative transfer curve, has a negligible amount of 2.5 V for the pristine device. The increasing of memory window indicates that blending QDs can significantly enlarge the memory window of organic semiconductor channel. In addition, the threshold voltages of easing transfer curves for all blended devices shifted positive compared with pristine device. The positive shifts of easing transfer curves are ascribed to the trapped electronics in deep defects caused by blending BPQDs which cannot be released even applying the pulse (-20 v,1 s). Moreover, interestingly, 4 vol% BPQDs blended device not only can perform read operation at zero gate voltage but also has larger memory window than the other amount BPQDs blended devices, which indicates that appropriate amount of BPQDs is crucial for memory characteristics, as small amount of BPQDs could not provide enough charge trap sites, while excessive BPQDs lead to more deep defects due

to agglomeration of QDs. Figure S2 demonstrates the transfer and output characteristics curves of three types of BPQDs blended devices. The transfer curves of the organic channel blending with BPQDs exhibit p-type transistor behavior with a high ON/OFF ratio up to 10^3 even with low drain voltage of -1 V. The output curves show that the device has an excellent ohmic contact.

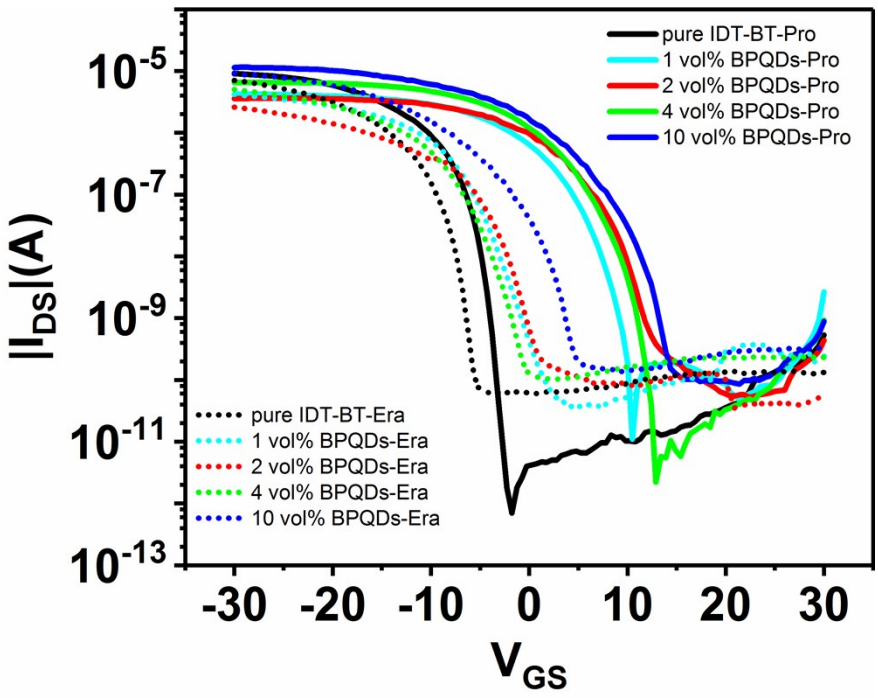

Figure S1. The transfer curves for the five types of BPQDs blended devices by applying writing and erasing pulses (±20 V, 1 s) with drain voltage at -20 V.

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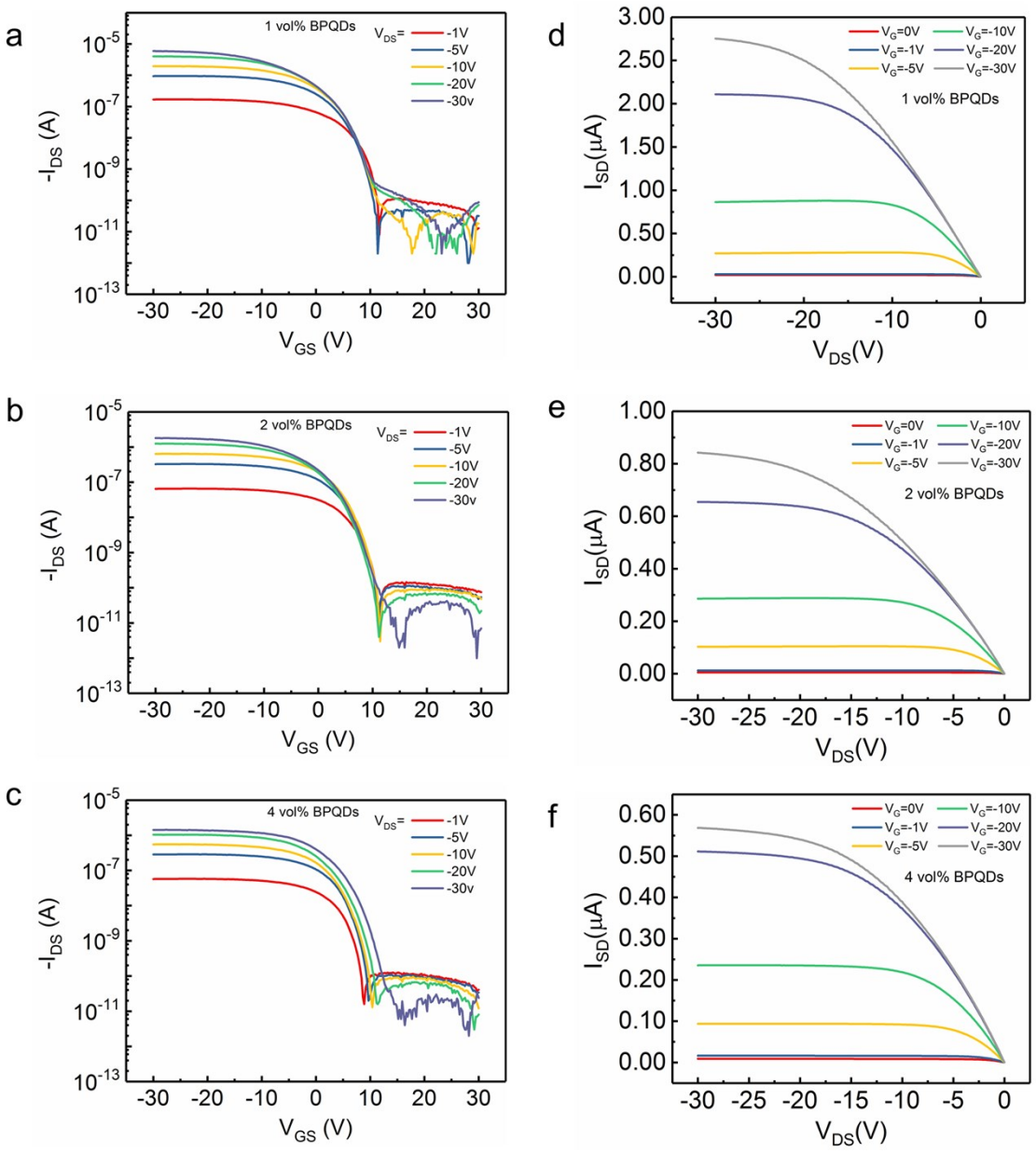

Figure S2. The electrical characteristics of the BPQDs blended devices. (a) (b) (c) Transfer curves of the 1 vol% (a), 2 vol% (b) and 4 vol% (c) BPQDs blended device with respect to different drain voltage. (d) (e) (f) Output characteristics of the 1 vol% (d), 2 vol% (e) and 4 vol% (f) BPQDs blended device with respect to different gate voltage.

2. The sudden enlargement of conventional memory window for the blended devices.

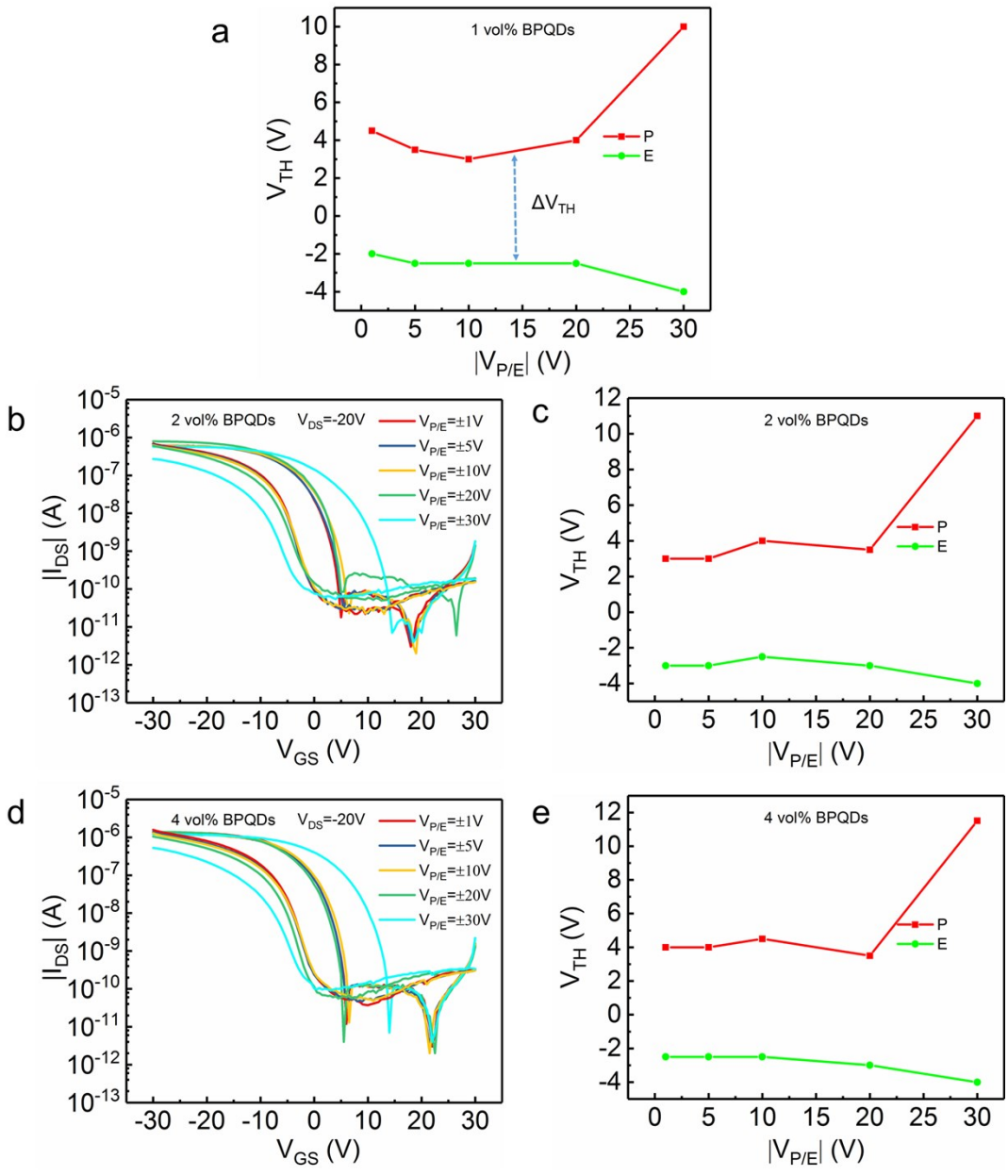

Figure S3. The dependence of threshold voltage on different programing /erasing impulse $V_{P/E}$ for the blended devices. (a) (c) (e) The conventional memory window variations of the 1 vol% (a), 2 vol% (c) and 4vol% (e) BPQDs blended devices as a function of impulse amplitude with duration time of 1 s. (b)(d) The transfer characteristic curves of the 2 vol% (b) and 4vol% (d) BPQDs blended devices on different programing

/erasing impulse amplitude with duration time of 1 s.

3. The respective dependence of conventional memory window on drain voltage and impulse time of gate voltage.

To investigate the programmable and erasable properties, the threshold voltage (V_{TH}) variation of transfer characteristic curves of the three types of BPQDs blended devices as a function of drain voltages, and gate voltages pulse time is investigated and the results are presented in **Figure S4 and Figure S5** respectively.

In order to further explore the effect of V_{DS} on the memory window, related electric measurements are performed and described in **Figure S4**. **Figure S4**a, b and c depict the transfer characteristic curves of the BPQDs blended device at V_{DS} from -1V to -30V with fixed $V_{P/E}$ pulse (±30 V, 1 s). Corresponding memory window variation of the device as a function of V_{DS} is shown in **Figure S4**d, e and f. With the increasing of V_{DS} from −1 to −30 V, the on and off currents both increase but the threshold voltage is almost unchanged, which suggests that V_{DS} has negligible effect on the memory window of the blended devices.

Figure S5 demonstrate the effect of $V_{P/E}$ pulse time on the memory window. **Figure**

S5a, b and c show the transfer characteristic curves of the blended device as a function of pulse time with fixed $V_{P/E}$ of ±30 V and V_{DS} of −30 V. The memory window variation of the blended device as a function of pulse time is presented in **Figure S5**d, e and f. The results indicate that the longer pulse time would induce more charge carriers which can be trapped into defects and be captured by BPQDs, resulting in an increase of memory windows. It is noteworthy that the threshold voltage of transfer curves shifted slowly with the increasing of programming pulse time from 0.05 s to 1 s, which indicates that both enough pulse amplitude and enough long pulse time are required for the charge capture of BPQDs.

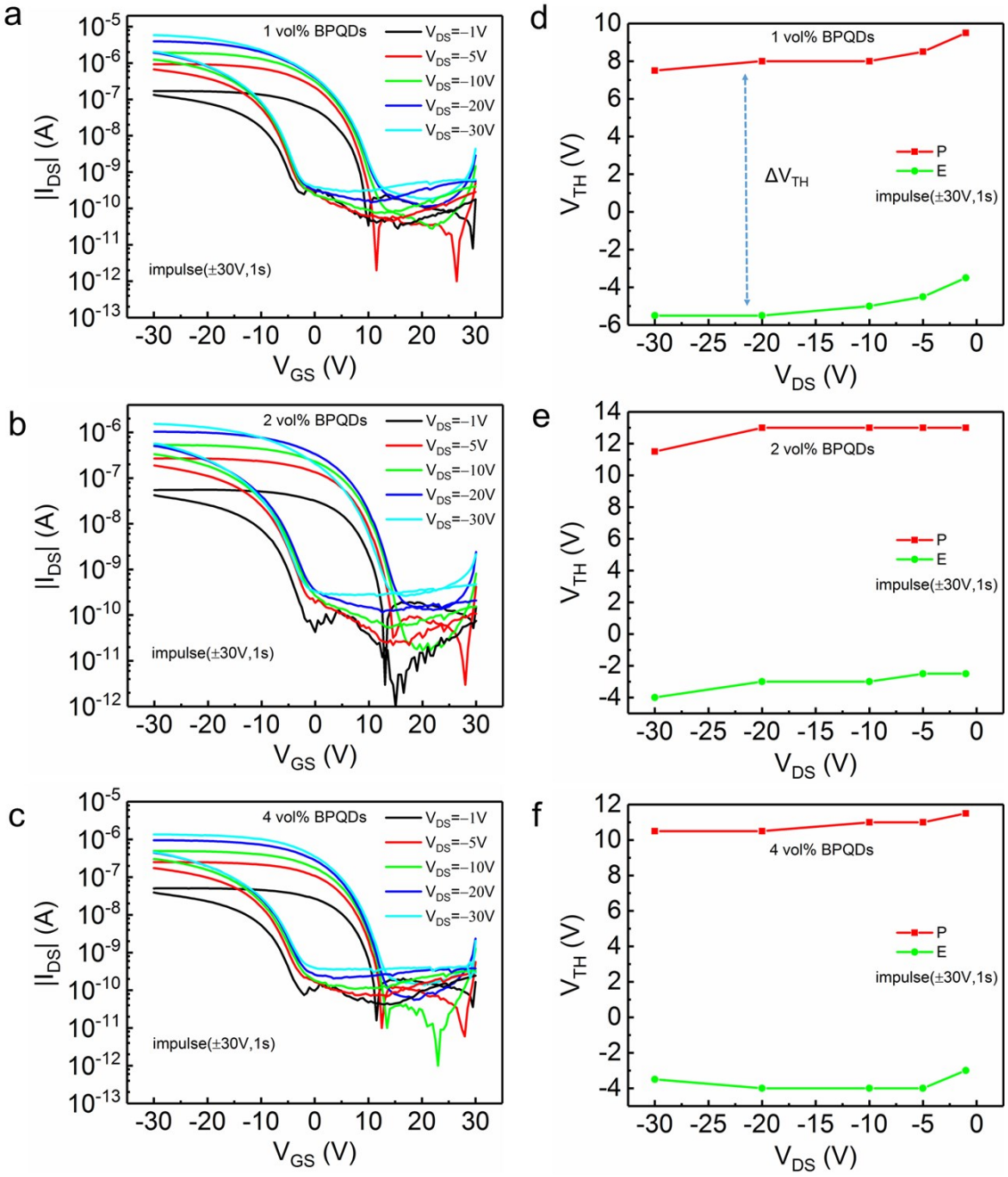

Figure S4. The dependence of conventional memory window on drain voltage. (a) (b) (c) The transfer characteristic curves of the 1 vol% (a), 2 vol% (b) and 4vol% (c) BPQDs blended devices with respect to different drain voltage. (d) (e) (f) Corresponding conventional memory window variations of the 1 vol% (d), 2 vol% (e) and 4vol% (f) BPQDs blended devices as a function of V_{DS}.

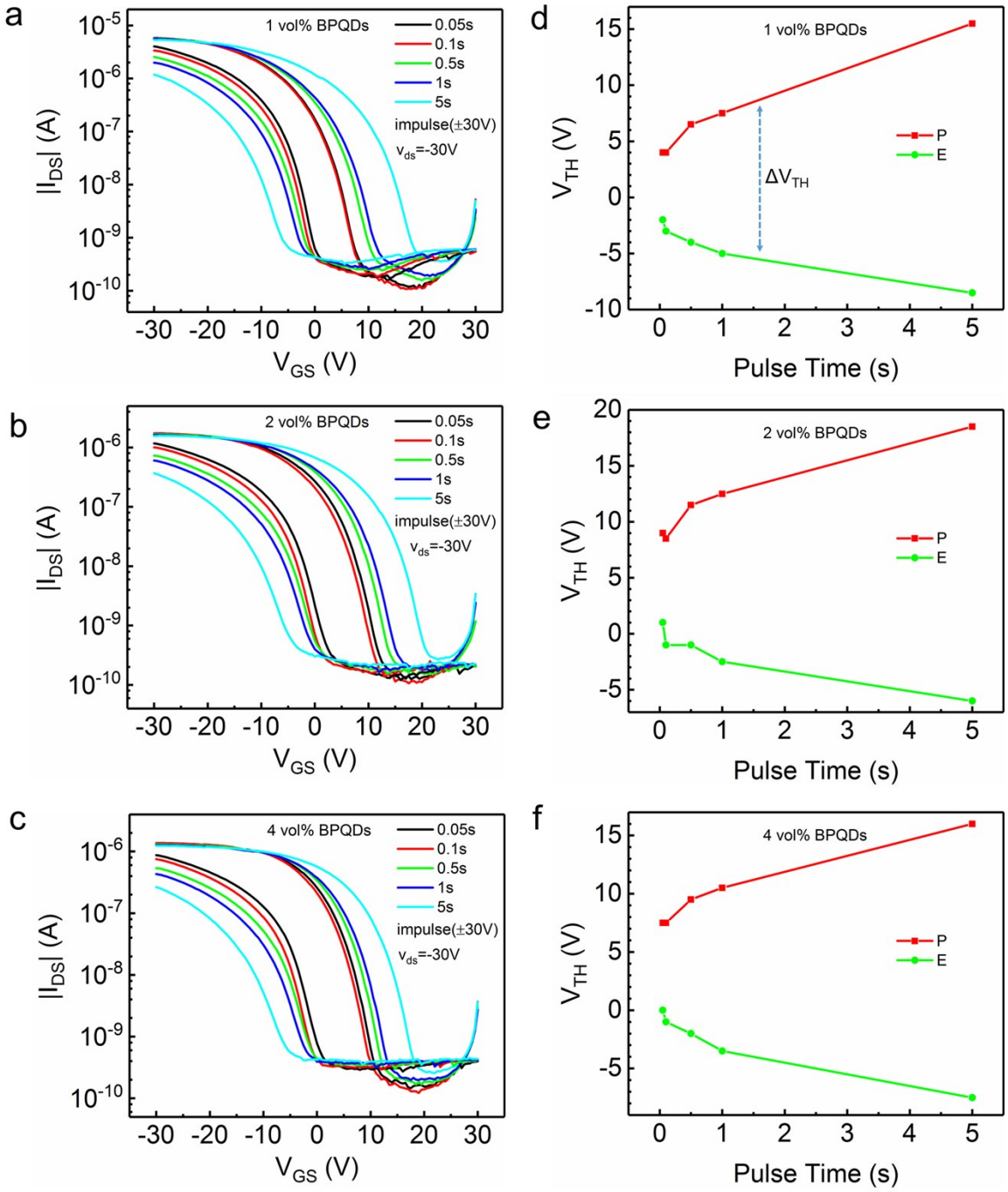

Figure S5. The dependence of conventional memory window on gate impulse duration. (a) (b) (c) The transfer characteristic curves of the 1 vol% (a), 2 vol% (b) and 4vol% (c) BPQDs blended devices with respect to different impulse duration. (d) (e) (f) Corresponding conventional memory window variations of the 1 vol% (d), 2 vol% (e) and 4vol% (f) BPQDs blended devices as a function of impulse time.

4. The asymmetry and principle in modulation for the synaptic transistor.

In order to investigate the difference of modulation to channel conductor for programming and erasing, the PSC triggered by 50 positive gate pulse (20 V, 0.5 s) with interval 0.1 s and 50 negative impulse (-10 V, 0.1 s) with interval 0.3 s is exhibited in **Figure S6**b. Obviously, linear modulation to channel conductor can be roughly observed with programming pulse number but the PSC tends to saturation quickly for erasing impulse. The asymmetry of modulation is mainly originated from the structure of device, which is described in **Figure S6**c. Due to the transmission channel close to the interface between dielectric layer and OSC, electrons at different heights will gradually sink to be trapped by defects with increasing of positive pulse number, while electrons trapped by defects in similar depth position will be most expelled simultaneously by the first negative pulse.

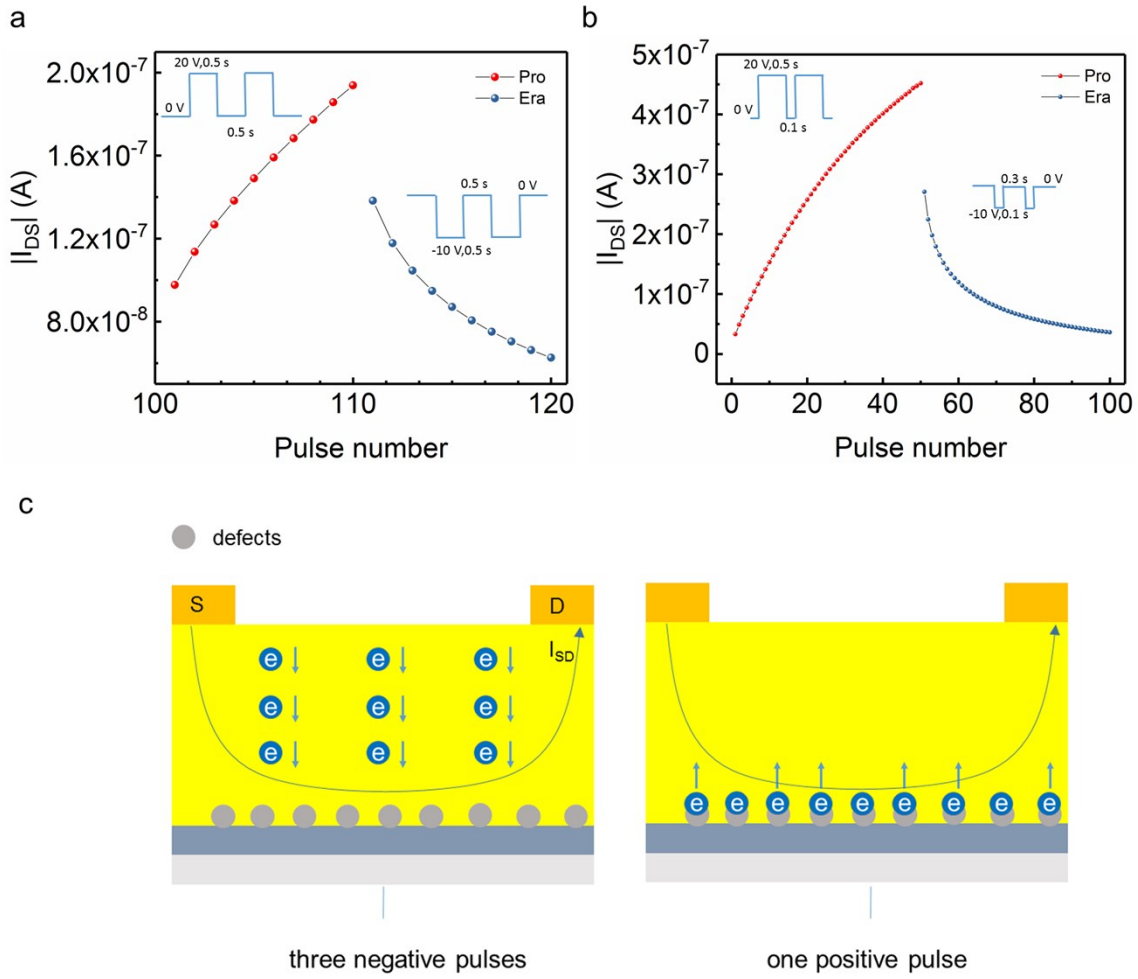

Figure S6. The asymmetry and principle in modulation for the blended device. (a) Enlarged image of one cycle in Figure 3e exhibiting successive potentiation and inhibition. (b) The similar asymmetry of modulation by different consecutive spikes with 50 positive gate pulse (20 V, 0.5 s) with interval 0.1 s and 50 negative impulse (-10 V, 0.1 s) with interval 0.3 s. (c) Schematic diagram to illuminate principle of asymmetry in modulation for the blended device.

5. The respective weight modulation of the synaptic transistor maintaining memory state "1" and "2" for pattern recognition.

To further illustrate the potential of the BPQDs blended transistor for in-memory computing, pattern recognition is implemented based on the experiment results of the potentiation and depression in **Figure S7** for each memory state respectively. **Figure S7**a and **S7**b present the conductance modulation of the synapse transistor in memory state "1" and in memory state "2" respectively. The drain current begins with 0.304 nA triggered by first positive gate pulse and rises to 16.7 nA by the 50th positive gate pulse in memory state "1" and the range of value is from 131 nA to 1220 nA in memory state "2". Obviously, modulation to channel conductor of state "1" shows more linear than memory state "2" due to the limitation of saturation current in channel. **Figure S7**c and **S7**d show the normalized figure of weight modulation in memory state "1" and "2" respectively.

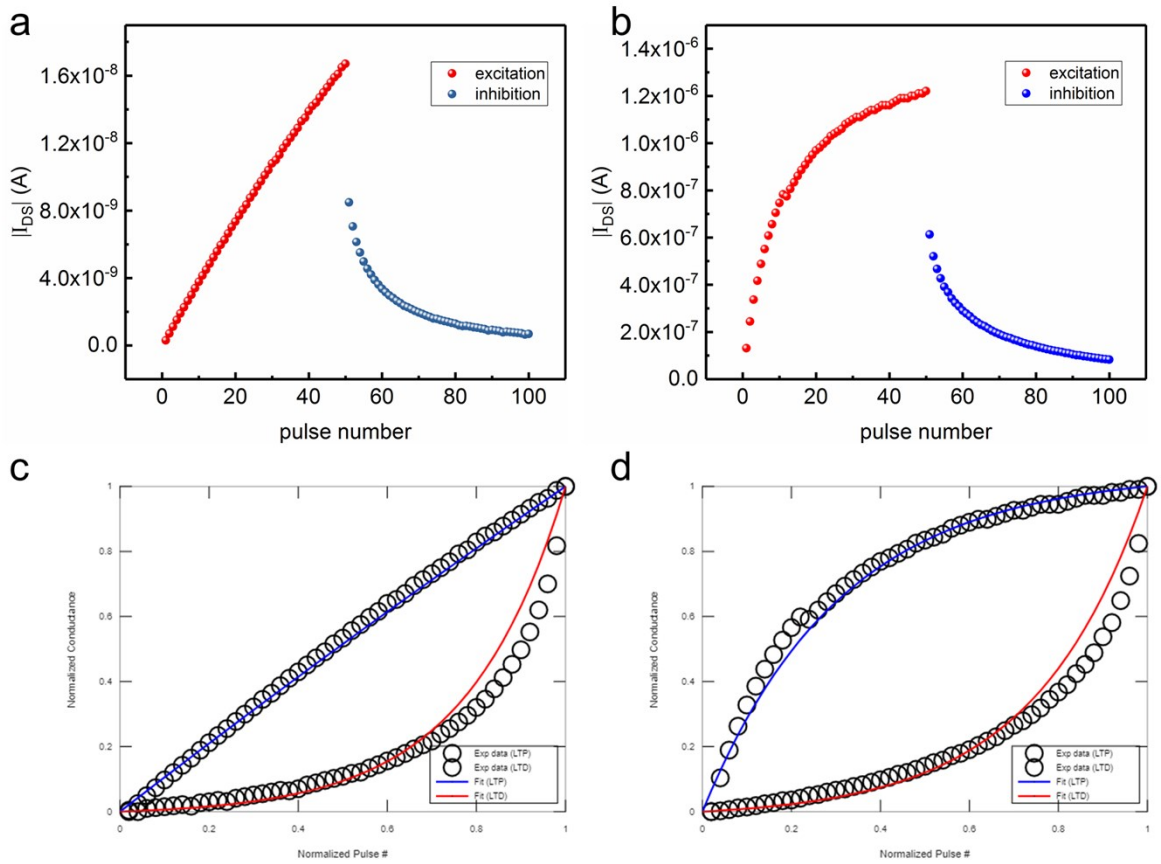

Figure S7. The respective weight modulation of the 1 vol% BPQDs blended device maintaining memory state "1" and "2" by consecutive spikes for pattern recognition. (a) The drain current modulated with 50 gate impulse (10 V,1 s) followed by (-1 V,1 s) in memory state "1". (b) The channel current stimulated by 50 gate impulse (30 V,1 s) followed by (-1 V,1 s) in memory state "2". (c) The normalized conductance as a function of normalized pulse number in memory state "1". (d) The normalized figure of weight modulation in memory state "2".

6. the aggregation phenomenon of BPQDs in the blended device..

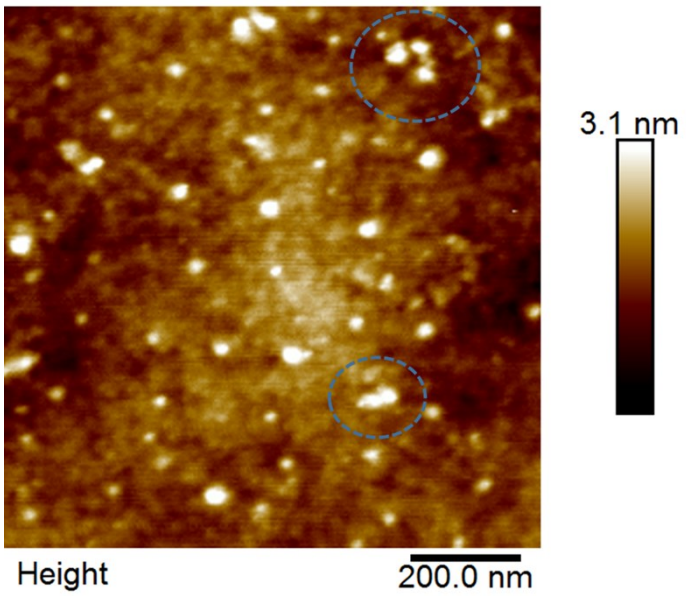

Figure S8. The AFM image of the 10vol% BPQDs blended device. The white points represent the BPQDs and the areas circled with blue dotted line indicate the aggregation of QDs.