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Supporting Information

Performance limit of Monolayer $MoSi_2N_4$ Transistors

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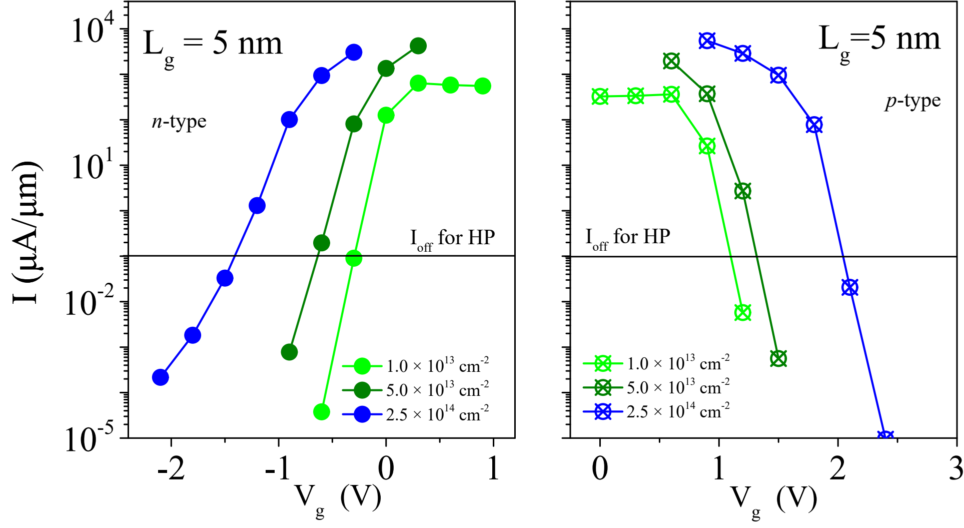

Figure S1. Transfer characteristics of *n*-type and *p*-type ML $MoSi_2N_4$ DG MOSFET with L_g = 5 nm and L_{ul} = 0 nm at different doping concentration.

Table S1. The I_{on}s of n/*p*-type ML $MoSi_2N_4$ DG MOSFET with L_g = 5 nm by different source and drain doping concentration of hole are listed below.

L_g	Hole/electron-doping（/cm^2）	I_{on} of *n*-type (μA/μm)	I_{on} of *p*-type (μA/μm)
5 nm	1.0×10^{13}	636	359
	5.0×10^{13}	1382	1343
	2.5×10^{14}	293	1322

From the test results, the I_{on}s of the 5 nm gate-length *n*-type and *p*-type ML $MoSi_2N_4$ DG MOSFET are the largest at the doping concentration of 5.0×10^{13} cm^{-2}. In terms of the maximum on-current, we choose 5.0×10^{13} cm^{-2} as the optimum doping concentration.

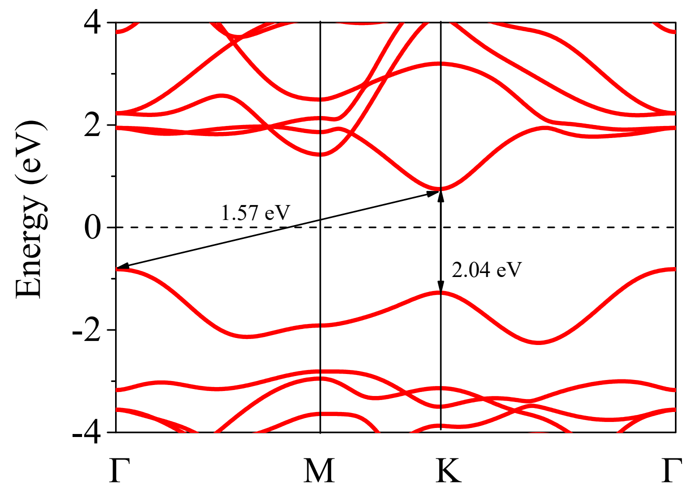

Figure S2. Band structure of monolayer $MoSi_2N_4$.

Table S2. Comparison of I_{on}, SS, delay time, and power dissipation in n/p-type ML $MoSi_2N_4$ DG MOSFET without and with NC layers.

	L_g (nm)	L_{ul} (nm)	I_{on} (μA/μm) for HP		I_{on} (μA/μm) for LP		SS (mV/dec)	
			Without NC	With NC	Without NC	With NC	Without NC	With NC
n-type	1	0	-	-	-	-	1044	-
		1	-	-	-	-	593	-
		2	59	753	-	-	209	138
		3	318	994	1	23	144	104
		4	490	1196	18	196	118	82
	3	0	120	3405	-	-	176	105
		1	470	2740	-	-	140	96
		2	800	2193	20	301	97	76
		3	1112	2288	163	831	80	68
	5	0	1382	4751	2	294	115	73
		1	1613	4325	114	1233	87	69
		2	1813	4516	77	3540	69	30
p-type	1	0	-	-	-	-	377	-
		1	114	1872	-	-	179	104
		2	290	1595	6	204	116	81
		3	393	1162	25	307	79	73
		4	362	783	46	259	59	44
	3	0	573	2644	4	850	113	68
		1	940	2941	67	1627	86	63
		2	959	2644	249	1002	63	51
		3	734	1463	252	523	47	40
	5	0	1343	2956	213	2439	71	51
		1	1690	2986	390	2004	46	38
		2	1244	2488	378	1065	52	45
ITRS	5.1		900		295			

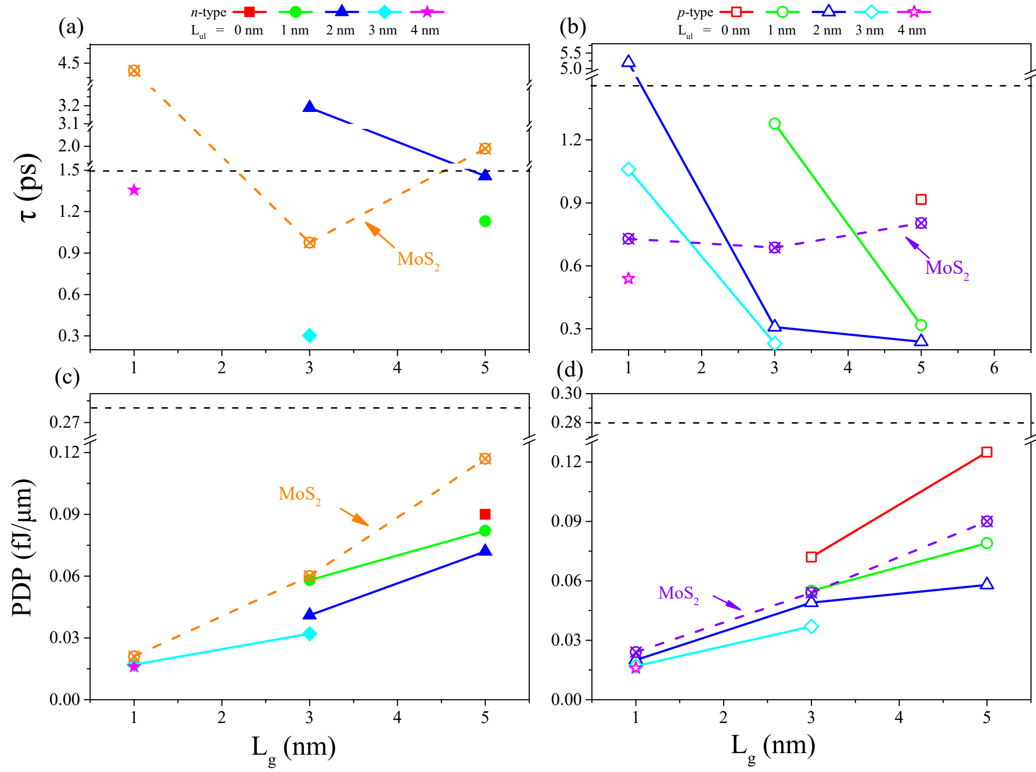

Figure S3. (a-b) Intrinsic delay time (τ) and (c-d) power dissipation (PDP) as a function of the gate length and underlap in DG ML $MoSi_2N_4$ MOSFETs with L_{ul} = 0, 1, 2, 3, and 4 nm for LP applications, respectively. The optimum τ and PDP of the *n*/*p* type DG ML MoS_2 counterpart for the LP device[1] are given by orange/purple dash line in each panel for the comparison, separately. Black dash lines are the ITRS LP requirements for τ and PDP in 2028, respectively.

Reference

1. Zhang, H.; Shi, B.; Xu, L.; Yan, J.; Zhao, W.; Zhang, Z.; Zhang, Z.; Lu, J., Sub-5 nm Monolayer MoS_2 Transistors toward Low-Power Devices. *ACS Appl. Electron. Mater.* **2021,** *3* (4), 1560-1571.