Supplementary information

Active Area Dependence of Optoelectronic

Characteristics of Perovskite LEDs

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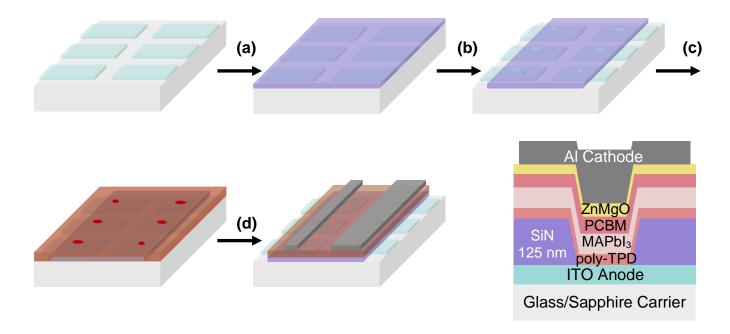


Figure S1. Simplified SiN fabrication flow of the bottom-emitting PeLED devices (dimensions not to scale). Each sample contains 12 devices of 6 different active areas, two of each area. (a) After a formation of sputtered ITO anode on a carrier substrate, pixel definition layer (≈ 125 nm SiN) is deposited via HDP CVD at a temperature of 350 °C. Circular structures and bottom contact pads are photolithographically defined by the development of the positive IX845G resist. The final pattern transfer is achieved by a Sf₆/O₂ dry etch process in Oxford Instruments Plasmalab System 100 ICP-RIE. This gas combination selectively etches SiN to ITO and produces sidewalls with positive slope angles (as confirmed by SEM, Figures 1 d and e). (c) PeLEDs are completed by a sequential spin-coating of poly-TPD (15 nm) hole transfer layer, MAPbI₃ (40 nm) emission layer, PCBM/ZnMgO (20 nm/20 nm) electron transfer bilayer. (d) In the last step, spin-coated material is mechanically removed to expose the anode, whereas the cathode is completed by vacuum evaporation of Al (120 nm). The excessive width of Al cathode leads to an adverse parasitic capacitor that contributes to RC product of the whole device. Herein, 1000 μm devices utilize 2 mm wide electrodes, whereas all the smaller sizes – 1 or 0.5 mm.

Table S2. Active area of PeLEDs used in this work.

Device	1000 μm	500 μm	300 μm	200 μm	100 μm	50 μm
Area [cm ²]	$7.85 \cdot 10^{-3}$	1.96·10 ⁻³	7.07·10 ⁻⁴	3.14·10 ⁻⁴	7.85·10 ⁻⁵	1.96·10 ⁻⁵
Scaling Factor	1	4	11.1	25	100	400

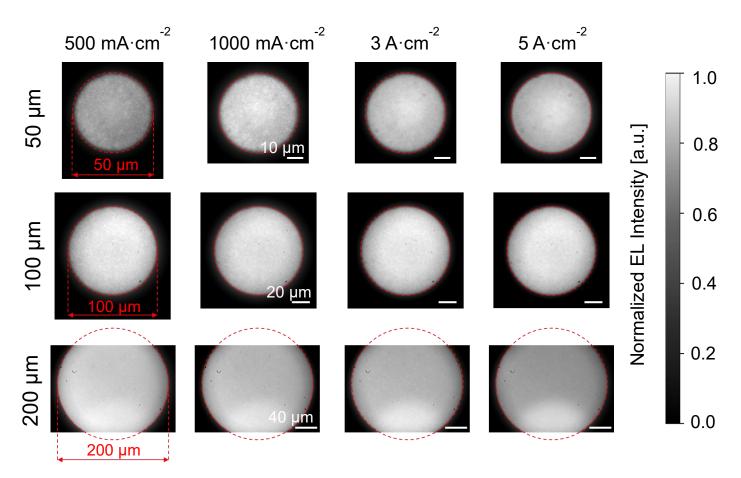


Figure S3. Spatial electroluminescence (EL) images at various current injection levels for 50 μ m, 100 μ m, and 200 μ m glass-based circular PeLEDs. Red border marks the edges of the devices as defined by a photolithographic design. Devices were driven in the quasi-DC mode. Electroluminescence is shown to be largely spatially uniform, with the effective electroluminescence area closely approaching the area set by photolithographic patterning. The imaging setup with a camera resolution of 4096 \times

2160 pixels with a 3.45 μm pixel size and the x44 magnification restricts the field of view to around 321 $\mu m \times 170 \ \mu m$.

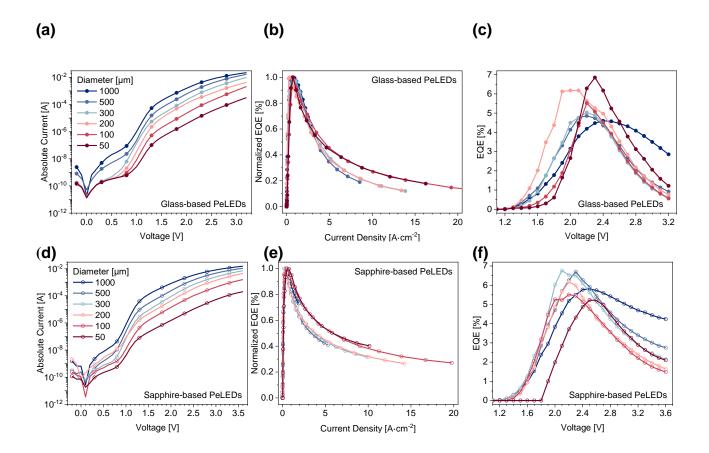


Figure S4. Active-area-dependent optoelectronic characteristics of glass (top row) and sapphire (bottom row) PeLEDs. (a), (d) *I-V* measurements. (b), (e) Normalized EQE-*J* characteristics. (c), (f) EQE-*V* plots.

In the ohmic region at 0.8 V and below, a lower limit for absolute PeLED current for the smallest devices (or the higher limit for the PeLED shunt resistance $R_{\rm shunt}$) is likely set by SiN capacitor and is equal to ≈ 600 pA and ≈ 580 pA at 0.8 V for glass- and sapphire-based PeLEDs, respectively.

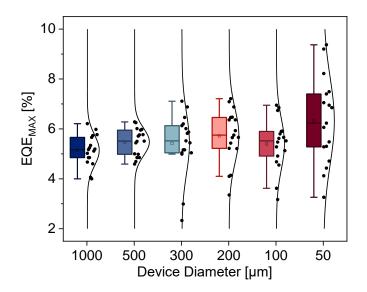


Figure S5. EQE_{MAX} statistical distribution of 102 devices of six different active areas, 17 of each area. Mean EQE is around 5.5 % and 6.3 % for 1000 μm and 50 μm PeLEDs, respectively. The smallest PeLEDs are subject to significant variability ($\sigma \approx 0.6$ % vs $\sigma \approx 1.7$ % for 1000 μm and 50 μm PeLEDs, respectively) with outliers reaching above 9 % EQE_{MAX}. Sapphire devices are not included in the statistics.

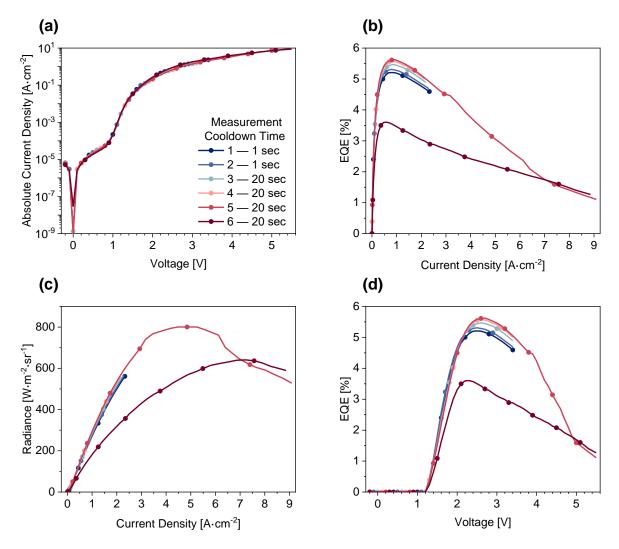


Figure S6. Electro-optical characteristics of 6 consecutive measurements for 1000 μ m glass-based PeLED recorded in a quasi-DC mode with 1 sec or 20 sec idle time between each acquisition. Measurements 1-4 are limited to 3.4 V (> 2 A·cm⁻²), whereas measurements 5 and 6 extend up to 5.5 V (> 8.8 A·cm⁻²). (a) *J-V* characteristics show very little variation among measurements. (b)-(d) EQE-*J*, Radiance-*J*, and EQE-*V* measurements show a stronger performance variation.

Maximum radiance operating point marks an irreversible degradation threshold that is strongly reflected in the recorded light signal, yet not in the electrical operation. Below this point, devices operate in a reproducible fashion with similar characteristics. However, we attribute PeLED

EQE/Radiance improvement from measurement 1 to 4 to stressing effects¹ and longer idle time that allows to effectively dissipate accumulated heat in-between each measurement.

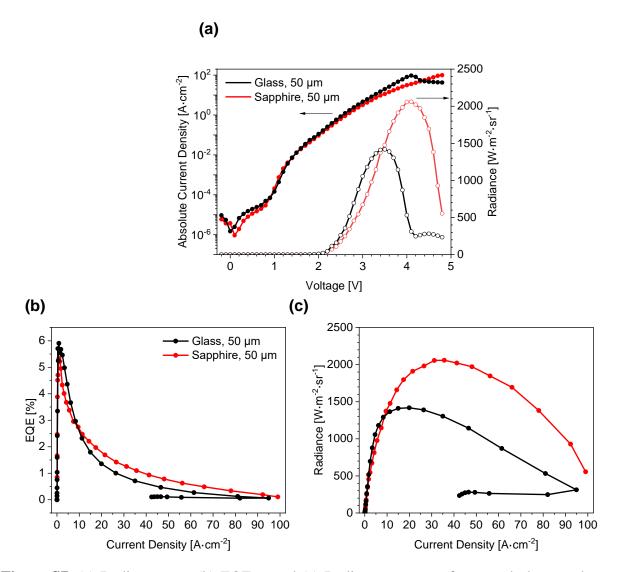


Figure S7. (a) Radiance-J-V, (b) EQE-J, and (c) Radiance-J curves for record glass- and sapphire-based 50 μ m PeLEDs measured in a quasi-DC regime at room temperature. A very steep EQE droop for both devices past the EQE_{MAX} up to 10 A·cm⁻² leads to more than 50 % EQE_{MAX} decrease, unaffected by heat generation. Overall, in the current density regime above 10 A·cm⁻², sapphire substrate provides a significant advantage and leads to a smaller EQE decrease even for a device with the smallest area used in this work. For the smallest devices fabricated atop sapphire, no irreversible degradation is observed below $\approx 30 \text{ A} \cdot \text{cm}^{-2}$.

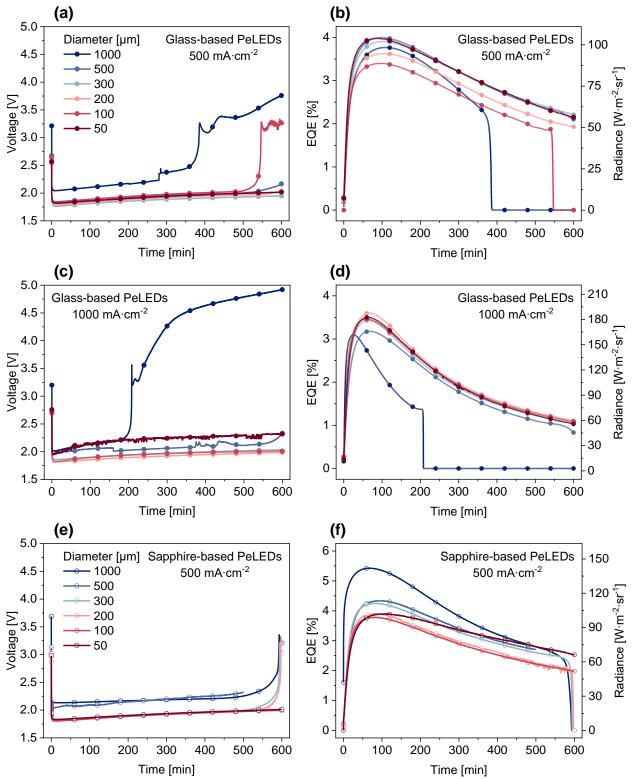


Figure S8. Voltage, EQE, and Radiance time evolution during constant-current lifetime measurement of glass-based PeLEDs at (a-b) 500 mA·cm⁻²; (c-d) 1000 mA·cm⁻²; and sapphire-based PeLEDs at (e-f) 500 mA·cm⁻². Most of the devices sustained continuous operation of 10

hours without hard breakdown. Voltage variation is caused by series resistance voltage contributions, stronger for larger devices, i.e., larger total applied currents. In strong contrast to a large $1000~\mu m$ glass-based PeLED, sapphire-based device of an equal area showed an almost identical T_{90} and T_{50} performance to the smaller devices.

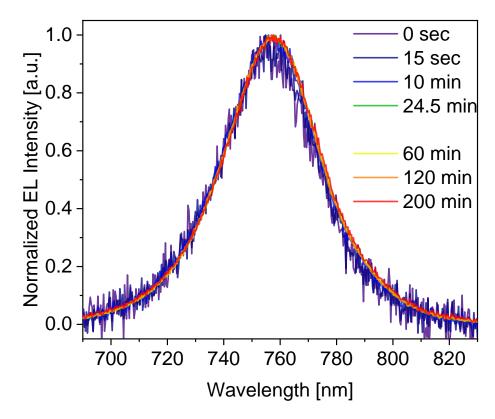


Figure S9. Electroluminescence (EL) intensity time evolution during constant-current lifetime measurement of 1000 μm glass-based PeLED at 1000 mA·cm⁻².

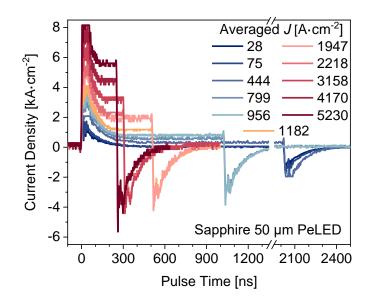


Figure S10. Typical transient current characteristics for our smallest sapphire PeLED, including the initial current spike, steady-state current relaxation, and a negative current spike.² The pulse times are 2000 ns, 1000 ns, 500 ns, 300 ns, and 250 ns. The steady-state value of current density is averaged over multiple data points during the pulse.

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