

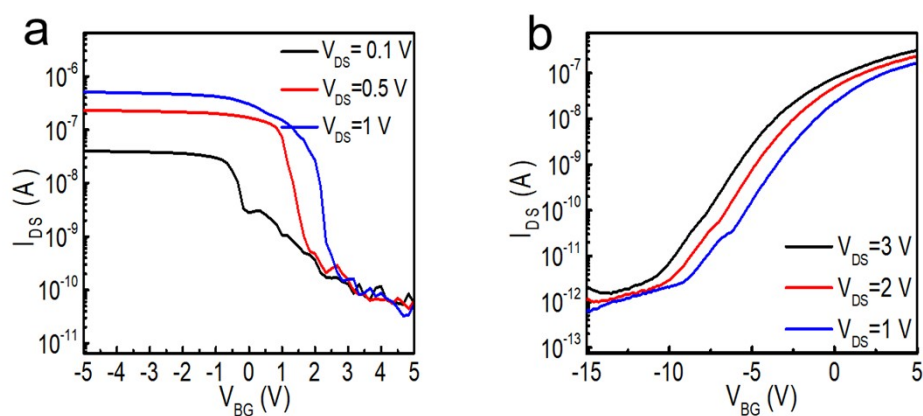
## Supporting Information

# Mixed-Dimensional WS<sub>2</sub>/GaSb Heterojunction for High-performance p-n Diode and Junction Field-Effect Transistor

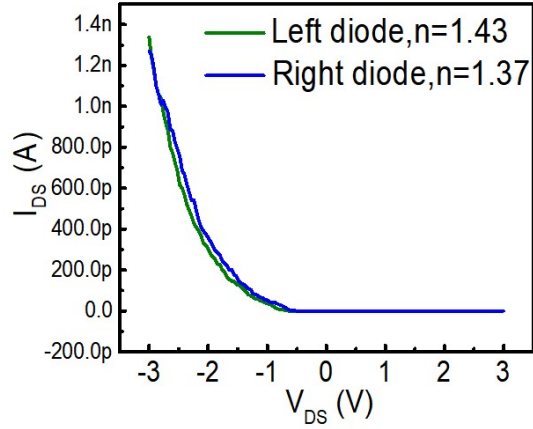
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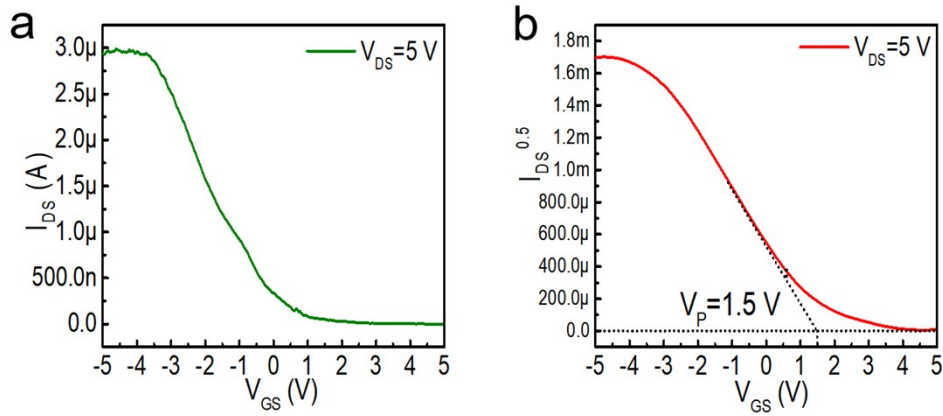
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**Fig. S1** Drain current-gate voltage ( $I_{DS}$ - $V_{GS}$ ) transfer curves of bottom-gate FETs with (a) GaSb nanowire and (b) WS<sub>2</sub> multilayer flakes on 285 nm-thick SiO<sub>2</sub> gate insulator/Si universal gate under different  $V_{DS}$ .



**Fig. S2** Linear scale current-voltage ( $I_{DS}$ - $V_{DS}$ ) curves of our p-n diodes formed by  $WS_2$  multilayer flakes on GaSb nanowire.



**Fig. S3** (a)  $I_{DS}$ - $V_{GS}$  curve of  $WS_2$ /GaSb JFET at  $V_{DS}=5$  V. (b)  $\sqrt{I_{DS}}$ - $V_{GS}$  curve of  $WS_2$ /GaSb JFET at  $V_{DS}=5$  V. The black dashed line linearly fits the curve of  $\sqrt{I_{DS}}$ - $V_{GS}$ , and its intersection with X axis gives the  $V_P$  (1.5 V).