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Supporting Information

Device Performance and Strain Effect of Sub-5 nm Monolayer InP Transistors

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Section I: Comparison between SG and DG ML InP MOSFETs

The transfer characteristics of the single-gated (SG) and double-gated (DG) *n*-type ML InP MOSFETs at L_g = 5 nm and UL = 0 nm with the doping concentration of 5 × 10^{12} cm^{-2} are calculated for comparison, as shown in Figure S1. The HP I_{on} of the SG ML InP MOSFET (575 μA/μm) is unable to reach the ITRS requirement (900 μA/μm). By contrast, the HP I_{on} of the DG ML InP MOSFET (1413 μA/μm) fulfills the ITRS demand and is two times larger than the SG counterpart. Besides, the DG ML InP MOSFET has a smaller SS than the SG ML InP MOSFET (117/150 mV/dec for the DG/SG ML InP MOSFET), which means better gate controllability. Therefore, the device performance of the DG ML InP MOSFET significantly surpasses the SG ML InP MOSFET. Experimentally, the DG ultra-thin GaAs FET shows higher I_{on}/I_{off} (10^6) and smaller SS (300 mV/dec) than the SG counterpart (10^5 for I_{on}/I_{off}, 400 mV/dec for SS) at the same channel length and drain voltage.[1] This result also proves the better device performance of the DG FET than the SG FET.

Compared with the single gate, the double gate covers more area of the channel, leading to better gate controllability and thus better device performance. This can also be illustrated by the natural length λ. As defined in the "Introduction" section, λ can be calculated by the formula $\lambda = \sqrt{\frac{t_{ch} t_{ox} \varepsilon_{ch}}{N \varepsilon_{ox}}}$, in which t_{ch} (t_{ox}), ε_{ch} (ε_{ox}), and N are the channel (gate oxide) thickness, channel (gate oxide) dielectric constant, and gate numbers, respectively. A better gate controllability generally requires a smaller λ. Compared with the SG FET, the DG FET possesses more gates, which means a larger N and thus a smaller λ. Therefore, the DG device has better gate controllability than the SG device.

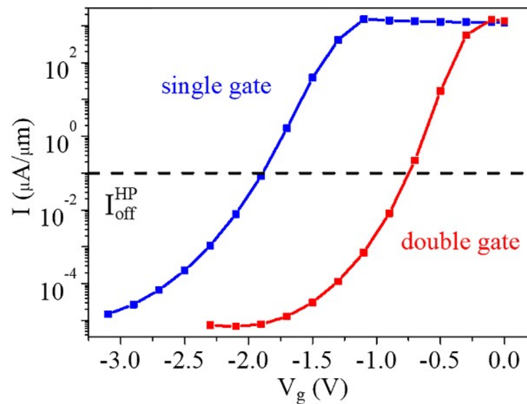

Figure S1. Comparison of the transfer characteristics between SG and DG *n*-type ML InP

MOSFETs at L_g = 5 nm and UL = 0 nm with the doping concentration of 5 × 10^{12} cm^{-2}.

Section II: Atomic Compensation Charge method

The electron density of the system:

$$\rho(\mathrm{r}) = \Delta\rho(\mathrm{r}) + \sum_{i}^{N_{atoms}} \rho_i^{atom}(\mathrm{r}) \tag{1}$$

Where $\Delta\rho(\mathrm{r})$ is the electron difference density, and $\sum_{i}^{N_{atoms}} \rho_i^{atom}(\mathrm{r})$ is the sum of the densities associated with the individual atom. Based on the following two formulas, the integral of $\Delta\rho(\mathrm{r})$ and $\sum_{i}^{N_{atoms}} \rho_i^{atom}(\mathrm{r})$ can lead to N and $\tilde{N}$, respectively.

$$\int \sum_{i}^{N_{atoms}} \rho_i^{atom}(\mathrm{r}) = N \tag{2}$$

$$\int \Delta\rho(\mathrm{r}) = \tilde{N} \tag{3}$$

in which N and $\tilde{N}$ are the total number of electrons and extra electrons, respectively. Using the atomic compensation charge method, $\tilde{N}$ is set to zero, and the extra charge is introduced by modifying N. The density of the i-th atom is rescaled by a factor:

$$c_i = \frac{\tilde{n}_i + n_i}{n_i} \tag{4}$$

Where n_i is the number of valence electrons, and $\tilde{n}_i$ is the extra compensation charge associated with the isolated i-th atom. The individual values of $\tilde{n}_i$, and therefore the individual coefficients c_i, can be set arbitrarily from atom to atom, even within the same chemical species. For sake of comparison, we assume here that $\tilde{n}_i$ and c_i are the same for all the atoms. In this case, the integral of the total density can be expressed as a sum over the individual densities:

$$\int \rho(\mathrm{r})\mathrm{dr} = \sum_{i}^{N_{atoms}} \int c_i \cdot \rho_i^{atom}(\mathrm{r})\mathrm{dr} \tag{5}$$

Section III: Comparison between *n*-type and *p*-type ML InP MOSFETs

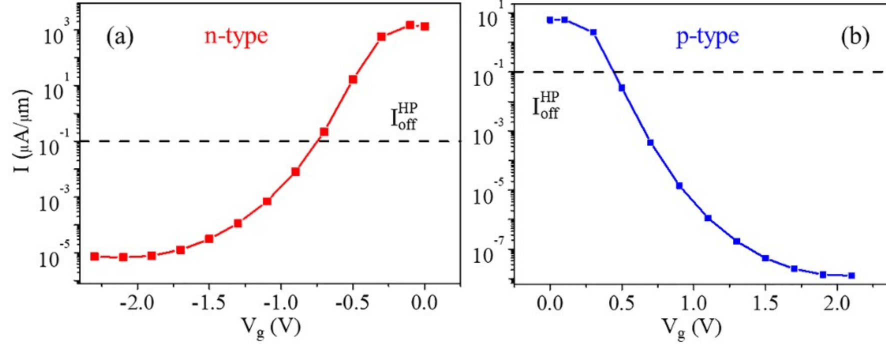

Figure S2. Transfer characteristics of the (a) *n*-type and (b) *p*-type ML InP MOSFETs at L_g = 5 nm and UL = 0 nm with the doping concentration of 5 × 10^{12} cm^{-2}.

Section IV: Illustration of Electron Transport Mechanism

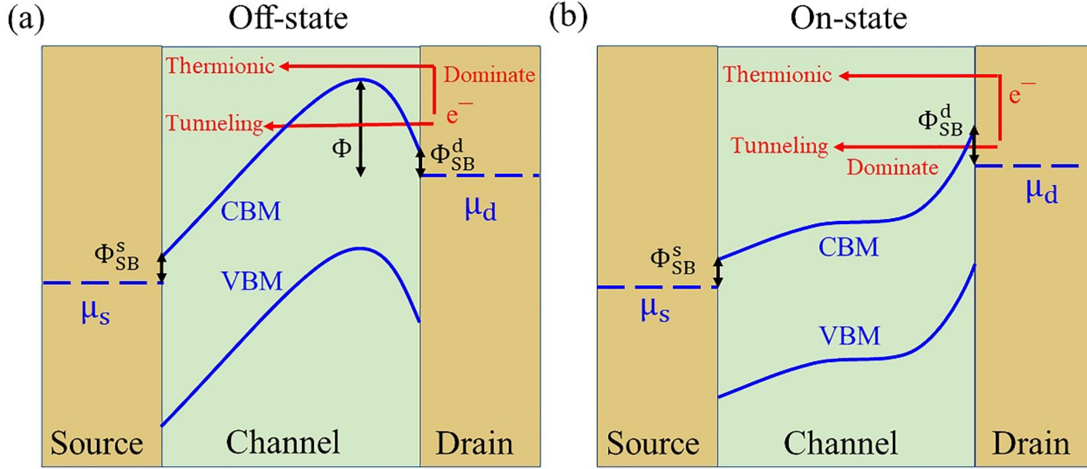

Figure S3. Schematic diagram of the electron transport mechanism at (a) off-state and (b) on-state. The thermionic emission and tunneling emission are the dominant mechanisms for the off-state and on-state, respectively. Φ is the electron barrier height, and Φ_{SB}^{s} (Φ_{SB}^{d}) is the Schottky barrier height at the source (drain)-channel interface. μ_s (μ_d) and CBM (VBM) are the source (drain) electrochemical potential and conduction band minimum (valance band maximum), respectively.

References

1. J.-P. Shim, S. K. Kim, H. Kim, G. Ju, H. Lim, S. Kim, H.-j. Kim, Double-gated ultra-thin-body

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