Supporting Information

Ambipolar to Unipolar Irreversible Switching in Nanosheets Transistors: The Role of Ferrocene in Fullerene/Ferrocene Nanosheets

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Experimental details

The C_{60}/Fc nanosheets were prepared by the method reported previously.[1]

The structure and morphology of the obtained nanosheets were characterized using scanning TEM (STEM; JEOL JEM-2100F, 200 kV), field emission SEM (FE-SEM; JEOL JSM-6700F, 5 kV). PYSA was performed with RIKEN KEIKI AC-3 equipped with a monochromated D2 lamp.

Fabrication of FET devices

The FET devices were fabricated by dropping of solutions of C_{60}/Fc nanosheets on prepatterned substrates. The prepatterned substrates (heavily doped Si wafers as gate electrodes with 300 nm-thick thermally oxidized SiO_2 layer as gate dielectric, Gold source and drain electrodes with channel widths of 10,000μm and lengths in the range of 2-10μm) were prepared at NIMS NAMIKI Foundry. Electrical transport properties were measured inside the glove box by using a semiconductor analyzer (Agilent B2902A, Agilent E5272A).

Theoretical calculations

Density of state (DOS) and projected DOS (PDOS) calculations for C_{60}/Fc nanosheets and fcc-C_{60} were performed using density functional theory (DFT) with the Perdew–Burke–Ernzerhof (PBE) functional[2] and PAW pseudopotentials[3, 4]. The *k*-point was set at 4 × 4 × 4. All the calculations were performed using the Vienna *Ab initio* Simulation Package (VASP) 5.4.4 program.[5, 6]

References

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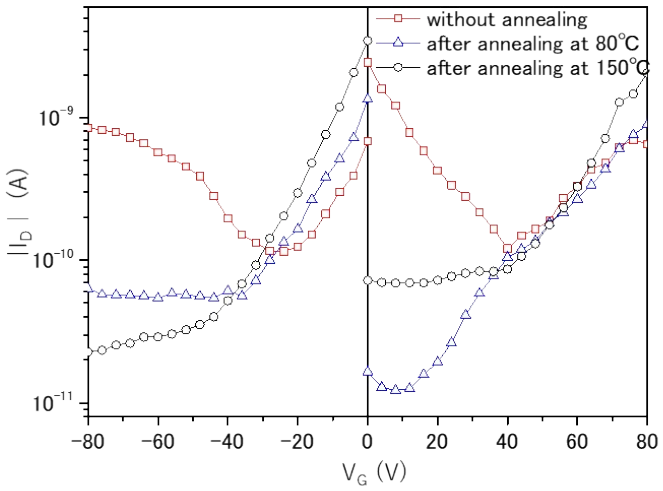

Figure S1. Transfer (I_D-V_G) characteristics of C_{60}/Fc nanosheets in the dark after annealing.

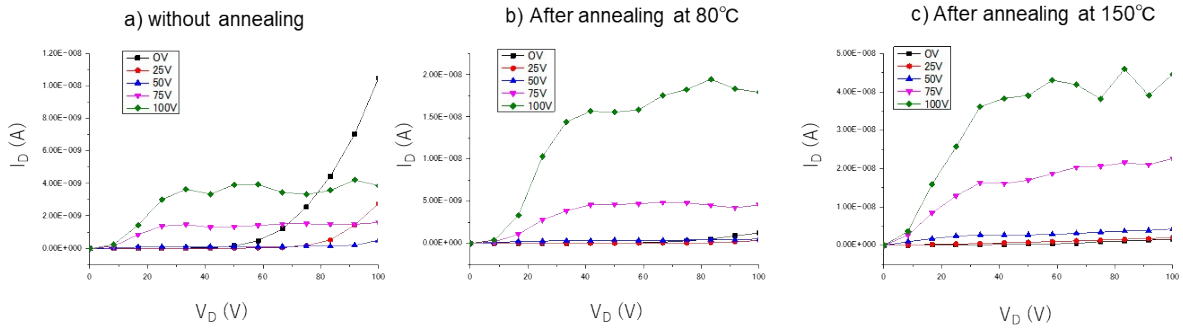

Figure S2. Typical output characteristics of C_{60}/Fc nanosheets based FETs a)without annealing, b) after annealing at 80°C, and c) after annealing at 150°C.

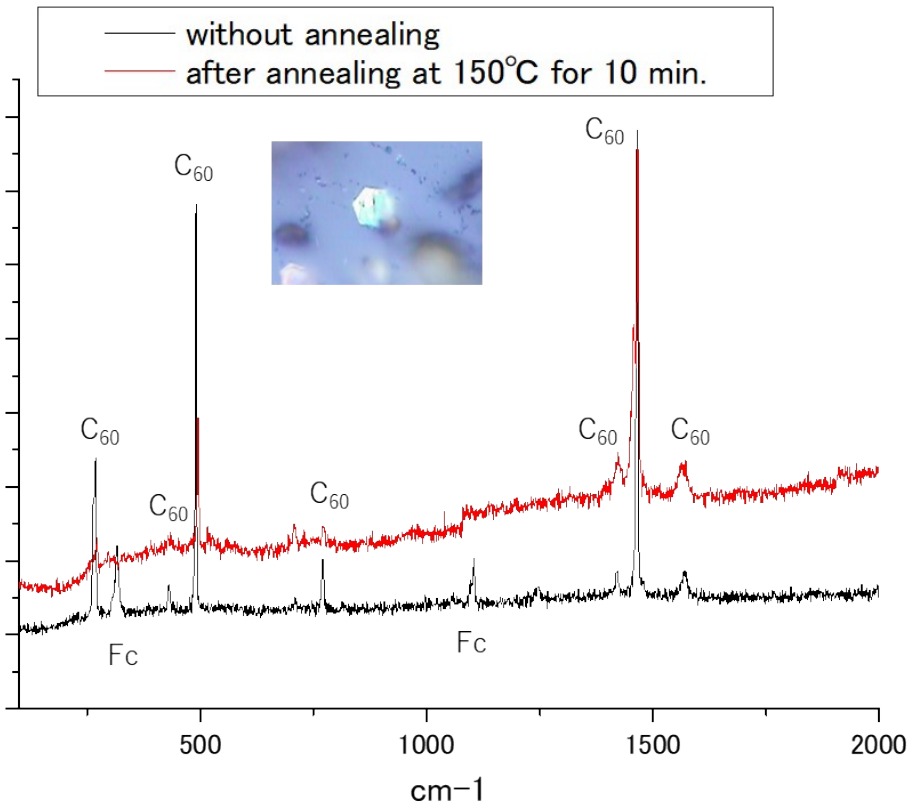

Figure S3. Raman spectra of C_{60}/Fc nanosheet without annealing (black line) and after annealing at 150℃ for 10 min (red line). Inset: optical microscope image of C_{60}/Fc nanosheet.