Electronic Supplementary Information (ESI)

Facile fabrication of ferroelectric poly(vinylidene fluoride) thin films with pure γ phase

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Experimental Section

Materials and chemicals

Poly(vinylidene fluoride) (PVDF) (weight-average molecular weight $M_w = 5.34 \times 10^5$ g/mol, vendor data) and poly(methyl methacrylate) (PMMA) [M_w of 4.76×10^4 g/mol and a polydispersity index (PDI) of 1.9] were purchased from MilliporeSigma and used directly without any treatment. The analytical grade N,N-dimethylformamide (DMF) and chloroform were purchased from Beijing Chemical Reagent Co. Ltd. The PVDF powder was dissolved in DMF at 100 °C for 8 h, while chloroform was used to dissolve PMMA powder at 50 °C for 8 h. The two kinds of solutions were conducted on a hot plate under magnetic stirring. The Si substrate was successively rinsed with detergent, deionized water, and isopropyl alcohol, and dried at room temperature in flowing nitrogen of 0.02 MPa before use. Solution of PVDF (4 g, 7.49 μmol) in DMF (50 mL) was spin-coated onto a Si wafer or Al electrode covered glass substrate at 80 °C and then dried in a vacuum oven at 90 °C for 12 h, yielding uniform PVDF thin films with thicknesses of *ca.* 420 nm (measured by a Dektak profilometer). The uniform PVDF thin films were heated at 5 °C/min in open air on the Linkam hot stage to different annealing temperatures (T_as) for 1 min and then cooled at 5 °C/min down to 25 °C, in order to regulate the content of electroactive γ phase.

Fabrication of ferroelectric devices

The metal-film-metal capacitor was fabricated as follows: (1) A bottom Al electrode with thickness of 80 nm was thermally evaporated on a glass substrate in vacuum. (2) A uniform PVDF film was spin-coated onto the Al electrode covered glass substrate and then treated using the same temperature program as described in main text. (3) A top Al electrode was thermally evaporated on PVDF film in vacuum, overlapping the bottom electrode and creating an area of 3.06 mm² for electrical measurement.

The OFeFET device was fabricated by following steps: (1) A uniform PVDF film was first spin-coated onto an ITO substrate and then treated using the same temperature program described in the main text. (2) After the treatment of the PVDF thin film, a thin layer PMMA with thickness of *ca.* 30 nm, as the dielectric layer in the FET devices, was spin-coated from its 8 wt% chloroform solution onto the PVDF film, and subsequently dried in a vacuum oven at 70 °C for 12 h. (3) Organic semiconductor pentacene was vacuum deposited on the dielectric bilayer of PVDF/PMMA to form the conducting channel of the FET device. (4) Source-drain gold electrodes with thickness of *ca.* 80 nm were evaporated on the PMMA surface.

Sample Characterizations

The surface morphology of the samples was monitored by a Dimension Icon AFM from Bruker Nano with scan rate from 0.5 to 1.0 Hz. Both height and phase images of the samples were recorded simultaneously in the tapping mode using silicon cantilever tips (TESP) with a resonance frequency of 300 kHz and a spring constant of 40 N/m. For in-situ AFM measurements, a hot stage connected with Bruker Thermal Applications Controller was equipped for controlling the sample temperature. The PVDF thin film spin-coated on Si substrate was heated and cooled at 5 °C/min, and the AFM images were scanned after stabilizing at the settled temperatures.

Thermal analysis was performed on a Q2000 TA Instrumental DSC equipment in a nitrogen atmosphere. The crystallinity of γ phase ($X_{c\gamma}$) was calculated by the equation:

$$X_{c\gamma} (\%) = \left(\Delta H_{m(\gamma)} / \Delta H_m^0 \right) \times 100\%$$

where $\Delta H_{m(\gamma)}$ is the melting enthalpy of γ phase in the spin-coated PVDF film; ΔH_m^0 is the melting enthalpy of a 100% crystalline PVDF and taken as 103.4 J/g in this study.[1] $\Delta H_{m(\gamma)}$ were obtained by multi-peak fitting the DSC curve.

Two-dimensional (2D) WAXD experiments were performed with a X-ray wavelength of 1.54 Å at beamline 1W1A of the Beijing Synchrotron Radiation Facility, Beijing, China. The

relative scattering intensity was recorded with a Mar165 CCD detector. FTIR transmission spectra scanned at the room temperature were recorded by a Spectrum 100 FTIR spectrometer (PerkinElmer) with averaging 16 scans and a resolution of 4 cm^{-1}. Double-sided polished silicon wafer was used as the substrate for the FTIR measurements of spin-coated PVDF thin films. The PVDF thin films during the thermal treatment were monitored by in-situ transmission IR, equipped with a T95 Linkam stage linked to T95-PE and LNP95 controllers. The rate for heating and cooling steps was 5 °C/min, and the FTIR spectrum at each temperature was captured by averaging 8 scans in mercury cadmium telluride (MCT) mode during the temperature-changing process. The characteristic bands at 764 cm^{-1} for α-PVDF and 840 cm^{-1} for γ-PVDF were used to determine the content of electroactive phase in different samples. To eliminate the influence of sample on the absorption intensity, the 877 cm^{-1} band was chosen as an internal standard for normalizing the spectra. The fraction of γ phase in films was calculated by: [2]

$$F_\gamma = A_\gamma / [(K_\gamma / K_\alpha) * A_\alpha + A_\gamma]$$

where A_α and A_γ represent the absorbance intensities of the bands at 764 and 840 cm^{-1}, while the K_α and K_γ are the absorption coefficients of those bands with the values of 6.1×10^4 and 7.7×10^4 cm^2 mol^{-1}, respectively.

The capacitor with the Al/PVDF/Al sandwich structure was then characterized with a Radiant Ferroelectric Tester Premier II-100 V in the ambient atmosphere. By using a sinusoidal bipolar waveform at the frequency of 1 Hz, the polarization-electric field (P-E) hysteresis loops were measured during voltage sweeping at various electric fields. The OFeFET device was evaluated with Keithley 4200 SCS analyzer in the ambient atmosphere.
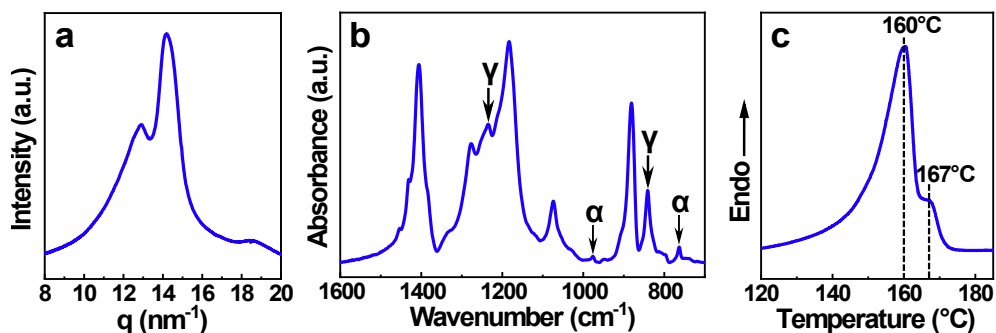
Fig. S1 (a) WAXD profile, (b) FTIR transmission spectrum and (c) DSC heating curve of as-prepared spin-coated PVDF thin films.
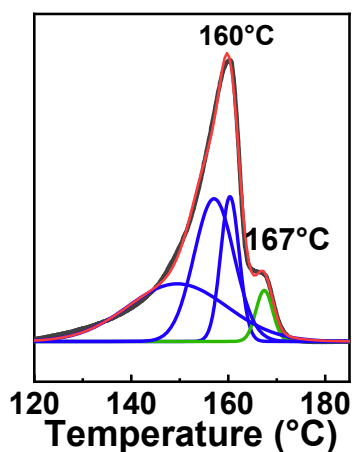

Fig. S2 Multi-peak fitting result of the DSC heating curve (in Fig. S1c) of the spin-coated PVDF thin film.
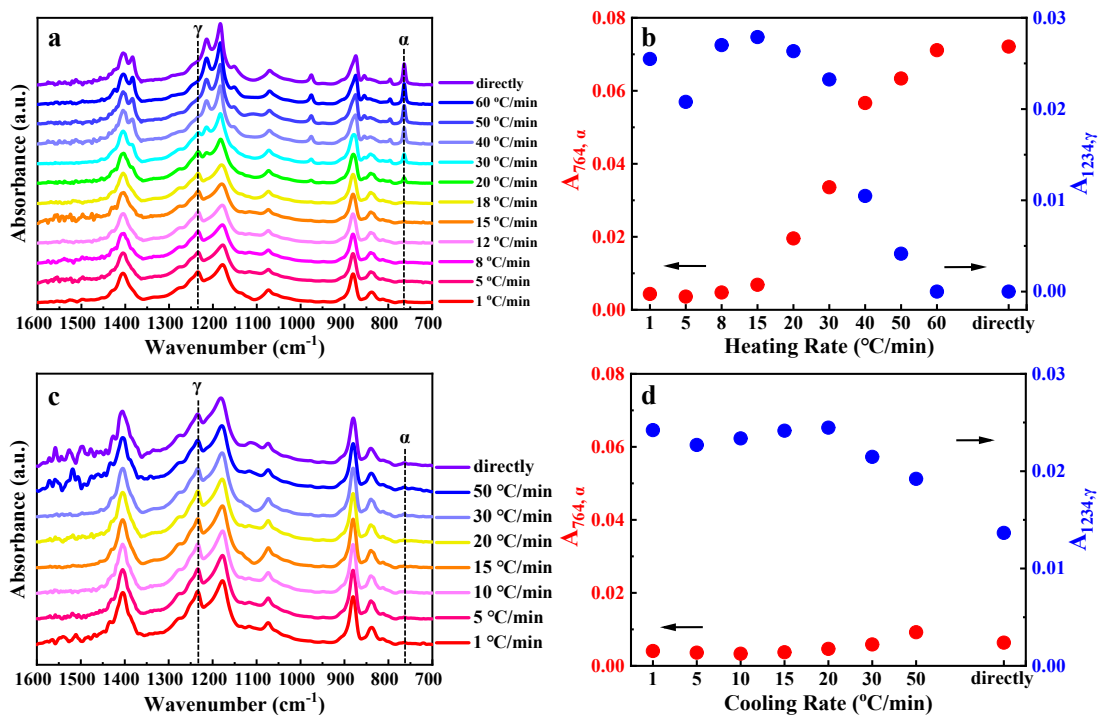

Fig. S3 FTIR spectra scanned at the room temperature for the spin-coated PVDF films annealed

at 166 °C with (a) a cooling rate of 5 °C/min and different heating rates and (c) a heating rate

of 5 °C/min and different cooling rates. Absorbance intensity of peaks characteristic of α and γ crystals plotted with (b) the heating rate and (d) the cooling rate. The term "directly" means "move the sample from one temperature to another temperature directly".
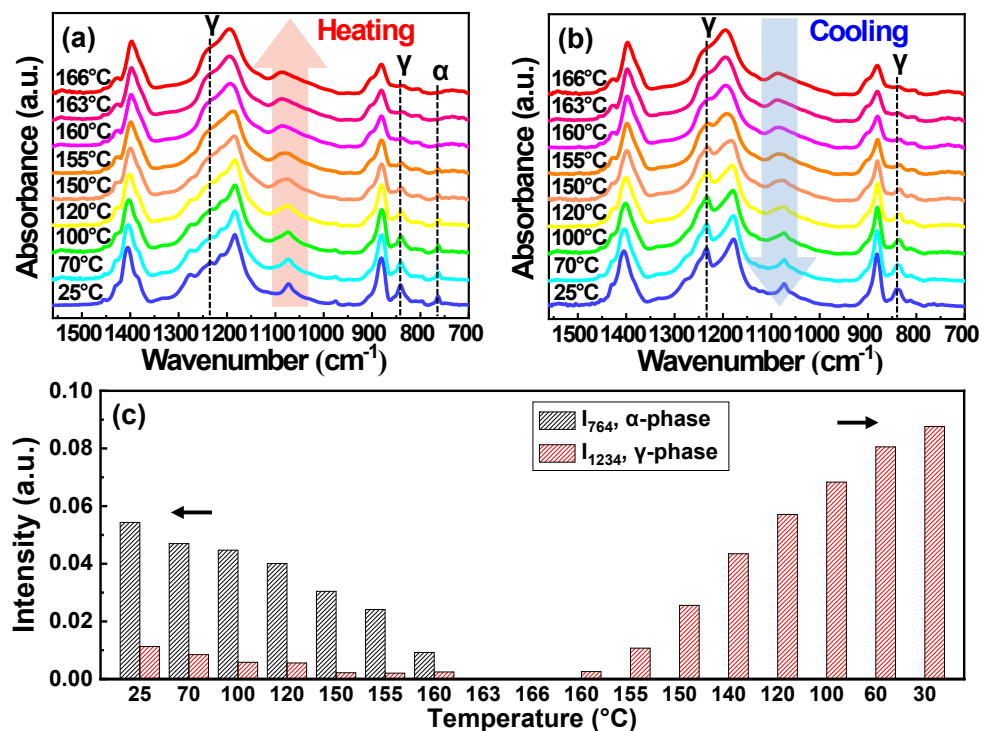

Fig. S4 In-situ FTIR spectra of the PVDF sample obtained during (a) heating process and (b) subsequent cooling process. (c) The variations in intensity of peaks located at 764 cm^{-1} and 840 cm^{-1} versus the temperature in the whole annealing process.
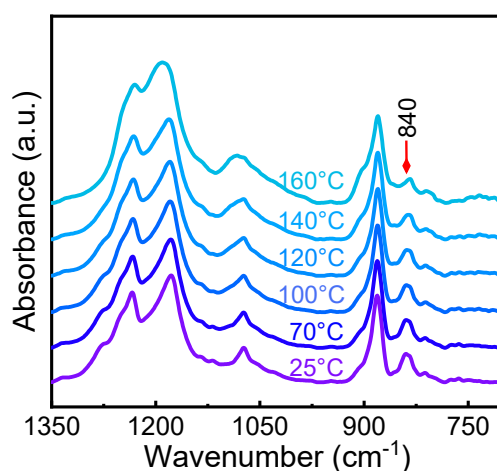

Fig. S5 In-situ heating FTIR spectra of pure γ-PVDF film, scanned at the indicated temperatures. Before the measurement, the PVDF film has been thermally annealed at 166 °C and cooled down to the room temperature.
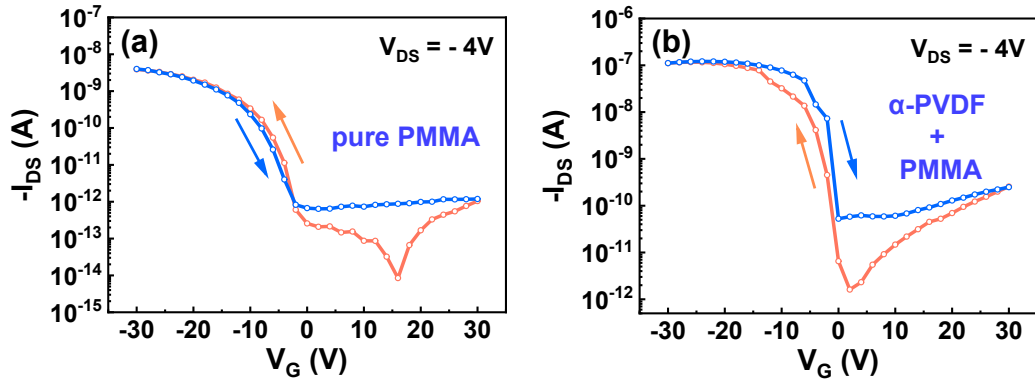
Fig. S6 The transfer curves of the FET devices based on (a) pure PMMA and (b) α-PVDF/PMMA bilayer with PEN as the active layer and ITO as the gate electrode. The α-PVDF layer was prepared by melt recrystallization, wherein the spin-coated PVDF film was melt at 200 °C for 10 min and slowly cooled to the room temperature.

The transfer curve of the PMMA device shows no obvious hysteresis loop, shown in Fig. S6a, which is expected due to the lack of ferroelectricity of PMMA. There is an extremely subtle clockwise loop of α-PVDF/PMMA bilayer device, see Fig. S6b, which exhibits a poor performance with an I_{on}/I_{off} value of only 8.1. Theoretically, α-PVDF is nonpolar, and its FET device should not exhibit any current hysteresis at zero gate bias voltage.[3] The subtle hysteresis loop of α-PVDF/PMMA bilayer device observed here might be attributed to partial polarization of the nonpolar α phase into the polar δ phase during the sweep of gate bias voltage.
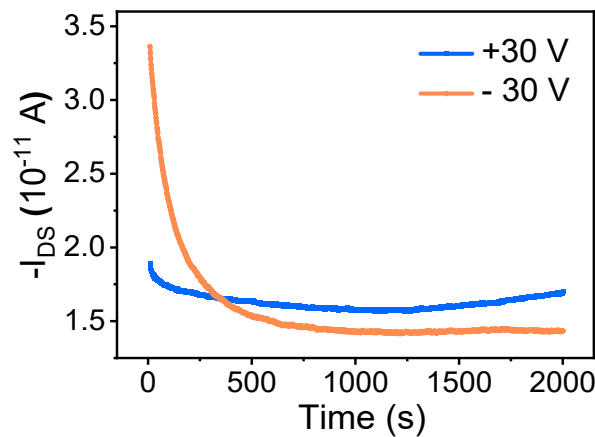

Fig. S7 Data retention characteristics of FET device based on α-PVDF/PMMA bilayer, measured at $V_G = 0$ V and $V_{DS} = -4$ V after programming -30 V and +30 V gate pulse voltage for the on and off drain current, respectively.

Data retention characteristics of α-PVDF/PMMA bilayer FET was performed at zero gate voltage with a fixed V_{DS} of -4V after programming -30 V and +30 V gate pulse voltage for the on and off drain current, respectively. It is seen that the initial I_{on}/I_{off} value at 0 s is less than 8.1 (Fig. S7), I_{on} then decreases rapidly with retention time until the existence of an intersection with I_{off} at approximately 330 s. All those current reduction phenomena reveal unstable of partial polarization of α-PVDF, resulting in nearly zero remnant polarization and a small I_{on}/I_{off} value when the gate bias returns to zero.

References

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