SI: Low temperature (Zn,Sn)O deposition for reducing interface open-circuit voltage deficit to achieve highly efficient Se-free Cu(In,Ga)S_2 solar cells

Mohit Sood*[a], Damilola Adeleye[a], Sudhanshu Shukla[a], Tobias Törndahl[b], Adam Hultqvist[b], Susanne Siebentritt[a]
(E-mail address: mohit.sood@uni.lu)

[a]*Laboratory for Photovoltaics, Department of Physics and Materials Science, University of Luxembourg, Belvaux, L-4422, Luxembourg.*
[b]*Solar Cell Technology, Department of Materials Science and Engineering, Uppsala University, Uppsala, 751 21, Sweden.*

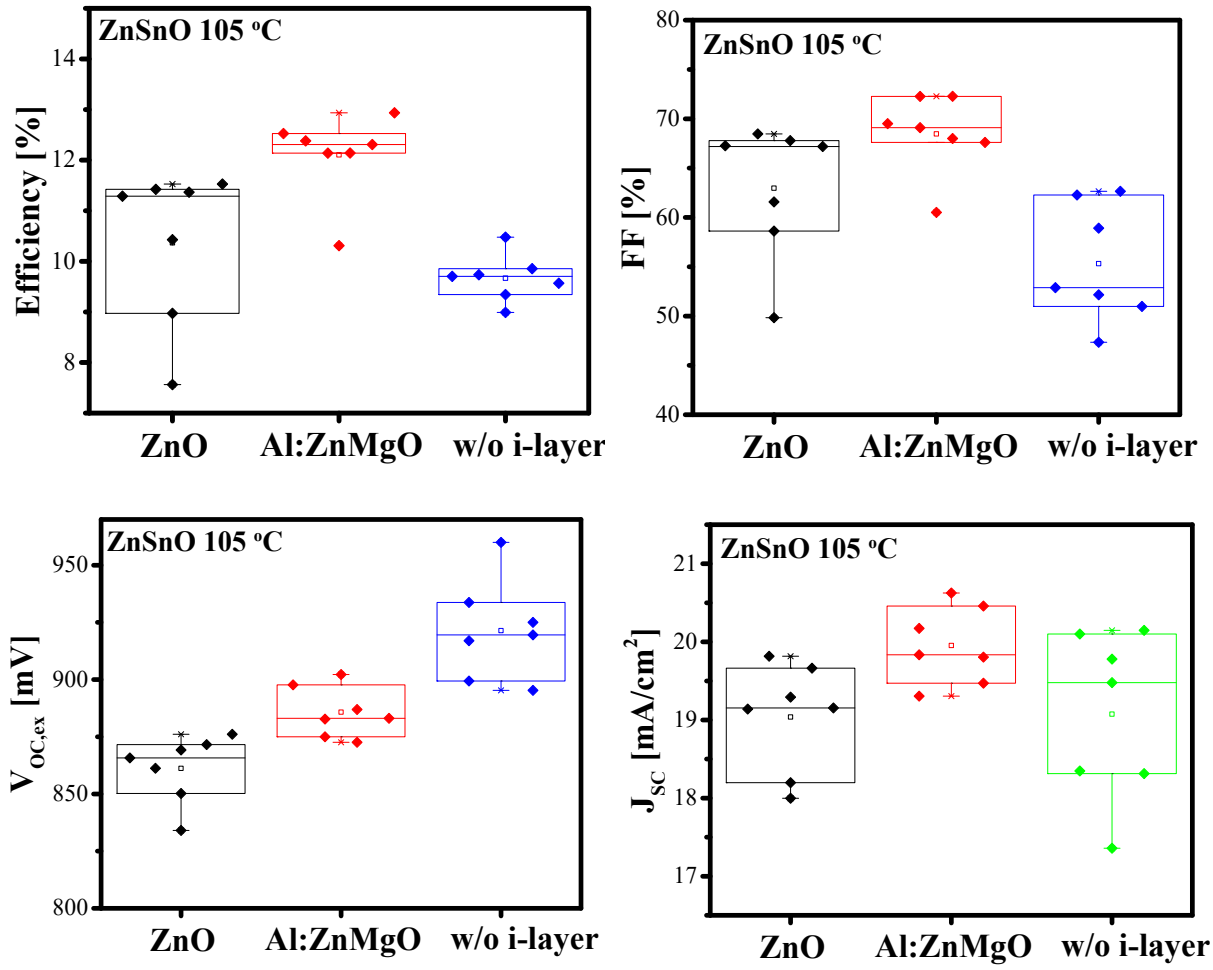

Figure S1: Box plot showing the distribution of J-V characteristics of Cu(In,Ga)S_2 devices using B1 with different i-layer combinations.

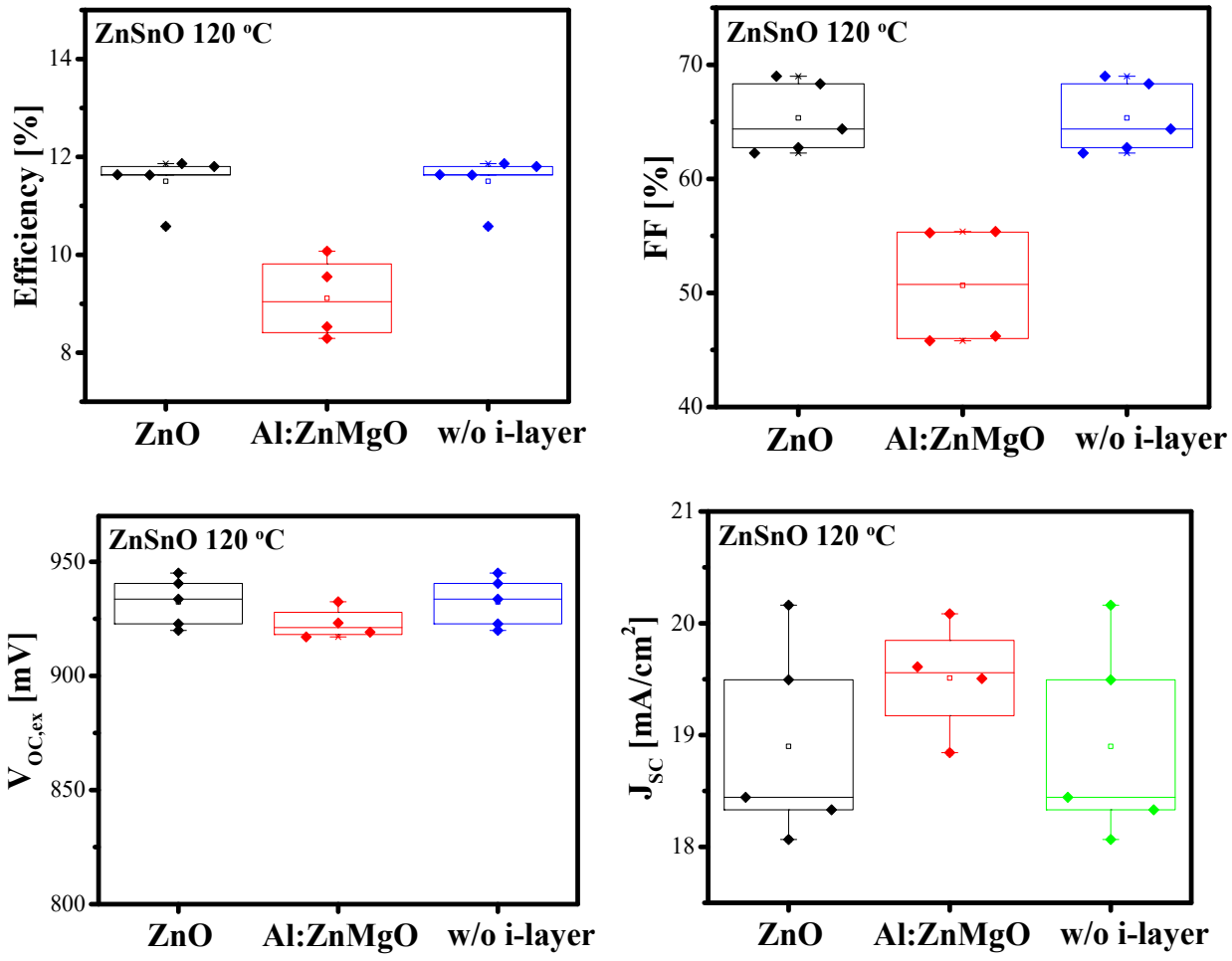

Figure S2: Box plot showing the distribution of J-V characteristics of Cu(In,Ga)S_2 devices using B2 with different i-layer combinations.

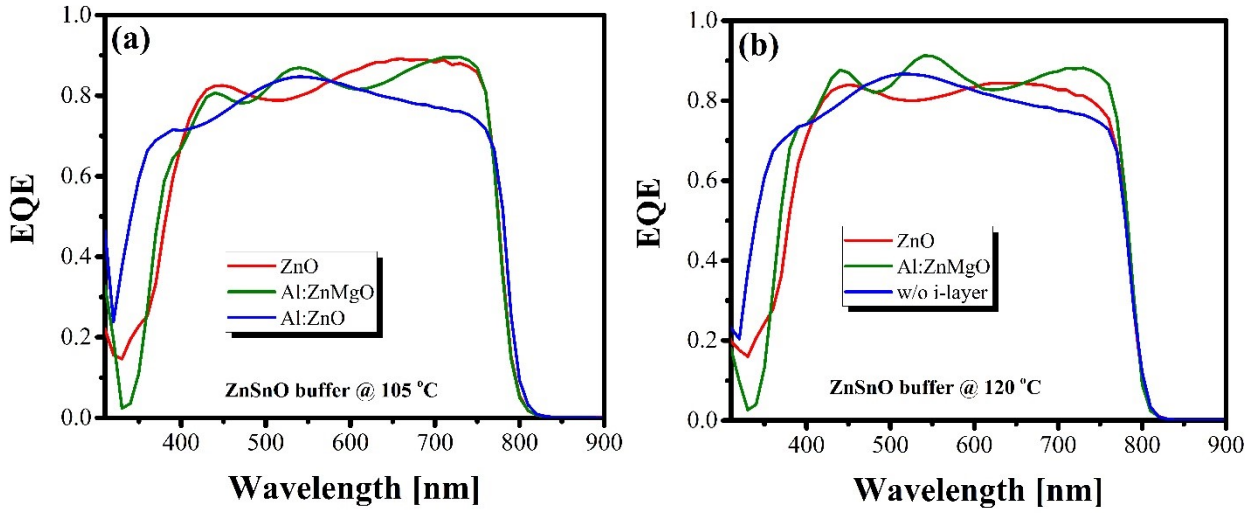

Figure S3: External quantum efficiency plot of (a) B1 device (b) B2 devices with different i-layer combinations.

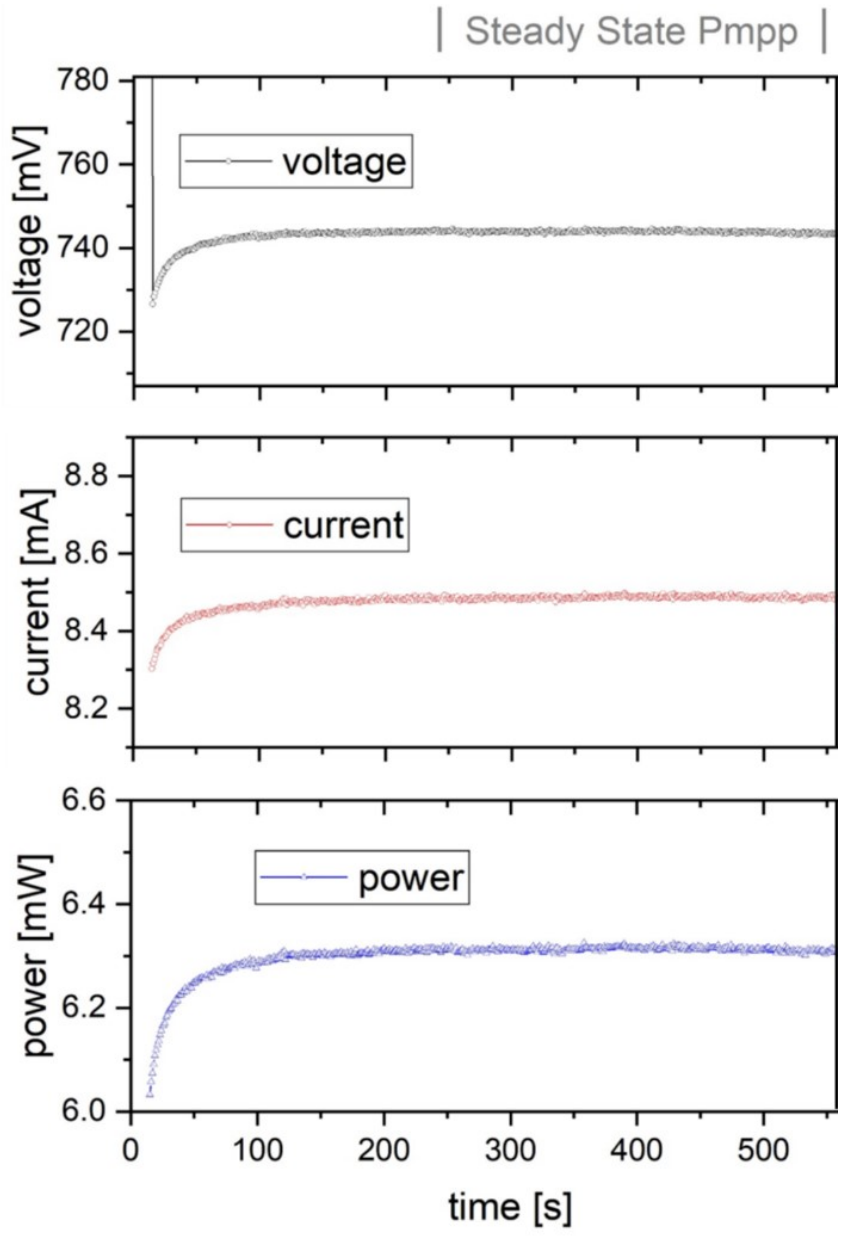

Figure S4: Transient curve of voltage (top), current (middle) and power (bottom) at maximum power point for the device under 100 mW/cm^2 illumination.

In-house measurements of the certified device

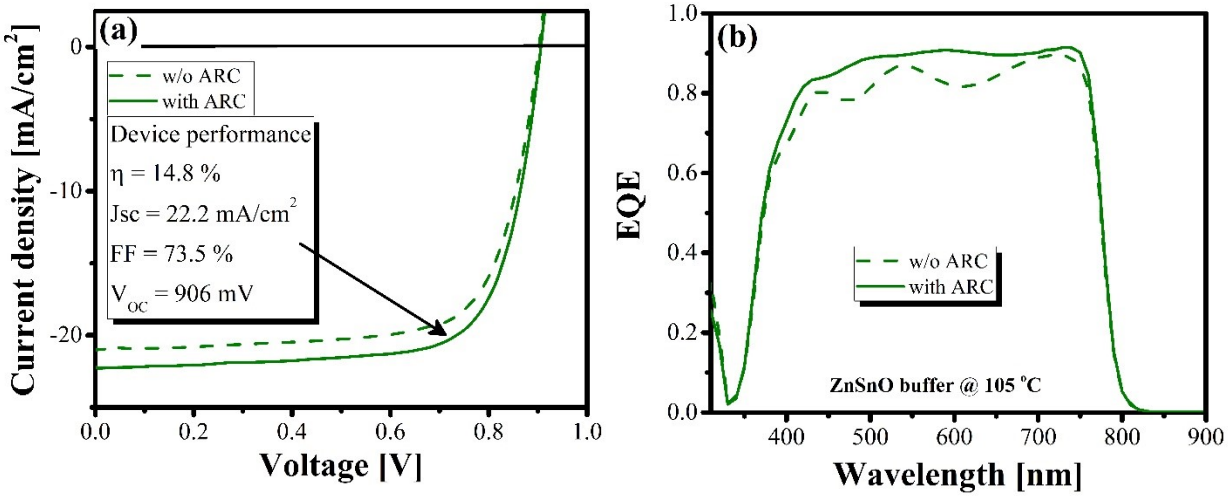

Figure S5: (a) I-V curve and (b) EQE curve of the Cu(In,Ga)S_2 device having a PCE of 14.8 % prepared with $Zn_{0.8}Sn_{0.2}O$ buffer layer deposited at 105 °C with sputtered Al:ZnMgO i-layer with and without an anti-reflective coating of MgF_2.