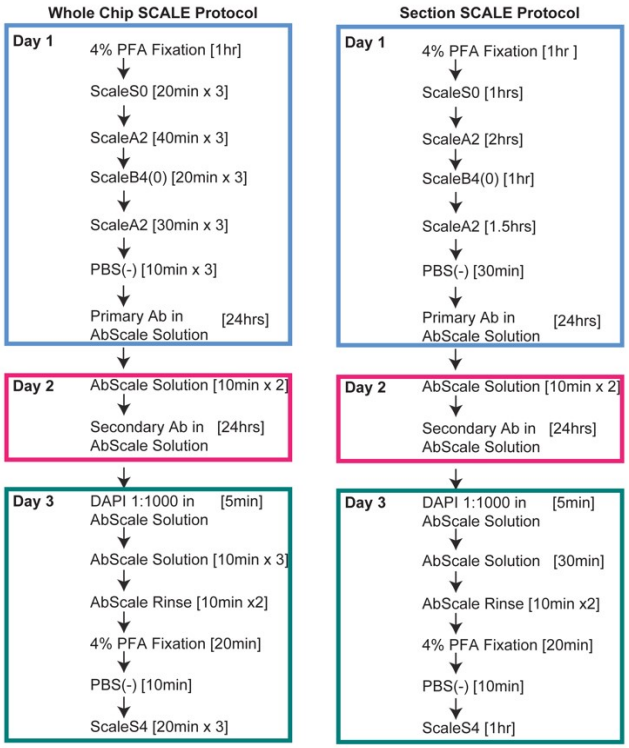
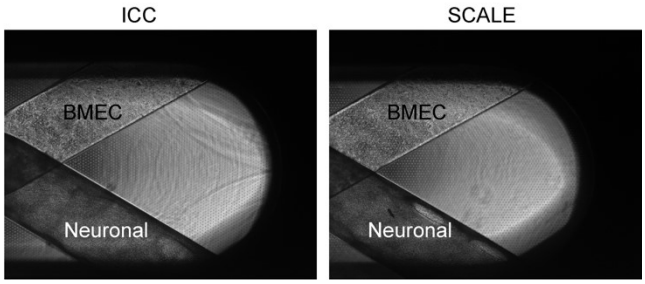
Electronic Supplementary Material (ESI) for Lab on a Chip.


**Supplemental Figure 1**: Flow diagrams depicting the timing of whole chip SCALE and section SCALE.




**Supplemental Figure 2**: Representative phase contrast imaging of d28 chips taken prior to staining or clearing applications. BMEC channel is shown at the top and neuronal channel is indicated at the bottom.