Supporting information

The Floating Body Effect of WSe2 Transistor With Volatile Memory Performance

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Experimental Section:

Chemicals: The tungsten diselenide (WSe_2) single crystal was purchased from a company named *HQ Graphene* and was mechanically exfoliated to multilayers flakes for the fabrication of dual-gate filed effect transistor. The single cast silicon oxide wafer was bought from Suzhou Crystal Silicon Electronic & Technology Co., Ltd and served as the bottom gate along with back dielectric layer. In addition, photoresist and corresponding stripping liquid, N-methylpyrrolidone (NMP), were both acquired from Suzhou Ruicai Semiconductor Co., Ltd. Especially, all the chemicals mentioned above were utilized directly without any further purification.

Device fabrication process: Initially, highly doped P-type silicon substrate coating with 300 nm silicon dioxide was served as the bottom-gate electrode and bottom dielectric layer, respectively. The multilayers WSe_2 nanosheets were obtained from monocrystal bulk material through Scotch-tape micromechanical cleavage technique and then directly transferred to the substrate by sticking the tape tightly to the substrate surface. Afterwards, the symmetric drain-source (D/S) electrodes (Cr/Au 5 nm/40 nm) were

patterned on top of the MLs WSe_2 by photolithography using photoresist materials and deposited via thermal evaporation as well as lift-off steps. In particular, the chromium electrode was only served as an adhesion layer. Subsequently, a layer of comprehensive and uniform coverage of 30 nm Al_2O_3 was deposited by atomic layer deposition (ALD) at the temperature of 200 Celsius degree, which serves as the top-gate insulating material. Finally, a top-gate electrode approximately located in the center of channel was fabricated in the same way as D/S electrode.

Structural and electrical characterization: The topography of the device and interface phase shift were characterized by means of atomic force microscopy (AFM) on a Bruker Dimension Fastscan AFM. For the surface morphology, a normal tip with back-coated reflective Al layer (Bruker: SCANASYST-AIR; k: 0.4 N/m; f_0: 70 kHz) was employed to investigate the height profile of the nanoflakes and the morphology of the dual-gate device on a ScanAsyst mode. With regard to the detection of the signal of phase change, proportional to the square of electric potential difference, a platinum-iridium coated conductive probe (Bruker: SCM-PIC-V2; k: 0.1 N/m; f_0: 10 kHz) was utilized operated in the function of electrostatic force microscopy (EFM) based on tapping mode. In particular, the dominant parameters for it are as follows: drive amplitude 1162 mV, amplitude setpoint 320 mV, drive frequency 61.5 KHz, scan rate 0.8 Hz, and lift height 80 nm. Besides, top-gate voltage bias is added to the sample by setting tip bias as +3 V and -3 V respectively. In the meantime, drain bias during writing operation is also applied through connecting to a signal generator with the value of 2 V. The electrical performance of the MLs WSe_2 based devices as common dual-gate transistor and 1T capacitor-less DRAM cell were characterized by the combination of Keysight B2902 along with Keithley 4200A-SCS parameter analyzer in the ambient atmosphere at room temperature. In addition, the drain and top-gate electrodes are connected with SMU-1 and SMU-2 of B2902 respectively, while the top-gate is connected with the SMU-1 from 4200. And the source electrode was connected to the mutual ground.

Simulation Methods: The structural optimizations and electronic structure calculations are performed based on density functional theory (DFT) as implemented in the Vienna Ab Initio Simulation Package (VASP) code[1], based on the projector augmented wave (PAW) method with a cutoff energy of 600 eV[2]. All of

configurations of WSe_2 models were fully optimized[1]. The generalized gradient form (GGA) of the exchange-correlation functional (Perdew-Burke-Ernzerhof 96, PBE) was adopted[3, 4]. A revised Perdew-Burke-Ernzerhof generalized gradient approximation (PBEsol)[5, 6] was used for the exchange-correlation. PBEsol functional has been introduced to improve the equilibrium properties of solids[7]. Valence-core interactions were described by projector-augmented-wave (PAW) pseudopotentials[8]. The Brillouin zone sampling is carried out using the (3 × 3 × 1) Monkhorst-Pack grids for surface and Gamma for the structure[2]. The convergence tolerance of energy is 1×10^{-5} eV, maximum force is 0.002 eV $Å^{-1}$, and maximum displacement is 0.002 $Å^2$.

The fundamental mechanism of floating body effect appearing in the conventional SOI-technology based transistor:

For a conventional SOI-MOSFET cell, because of the unavailable contact with the substrate, the channel body constitutes a capacitor against the insulated substrate. In this situation, the floating body effect originating from the holes generated by avalanche effect will induce the change of body potential resulting from the historical operations of voltage biasing and the corresponding carrier generation/recombination processes. In particular for the partially-depleted (PD) SOI transistor whose body thickness is relatively thick (guaranteeing the presence of intermediate neutral region), the threshold voltage during the transfer characteristic curve is dominated by the floating body effect. When applying a large positive drain voltage and negative top-gate bias, the electrons within the front-channel will obtain adequate energy under giant electric field closed to the drain edge and to produce a large number of electron-hole pairs. In this situation, the induced electrons swiftly reach the drain region while the remanent holes migrate towards the floating body, contributing to the gradual accumulation of holes. Moreover, the aggregated holes in the floating body will enhance the body-emitter voltage, which consequently reduce the threshold voltage. As a result, it is reasonable for us to utilize such variation of threshold voltage induced by floating body effect to realize hysteresis.

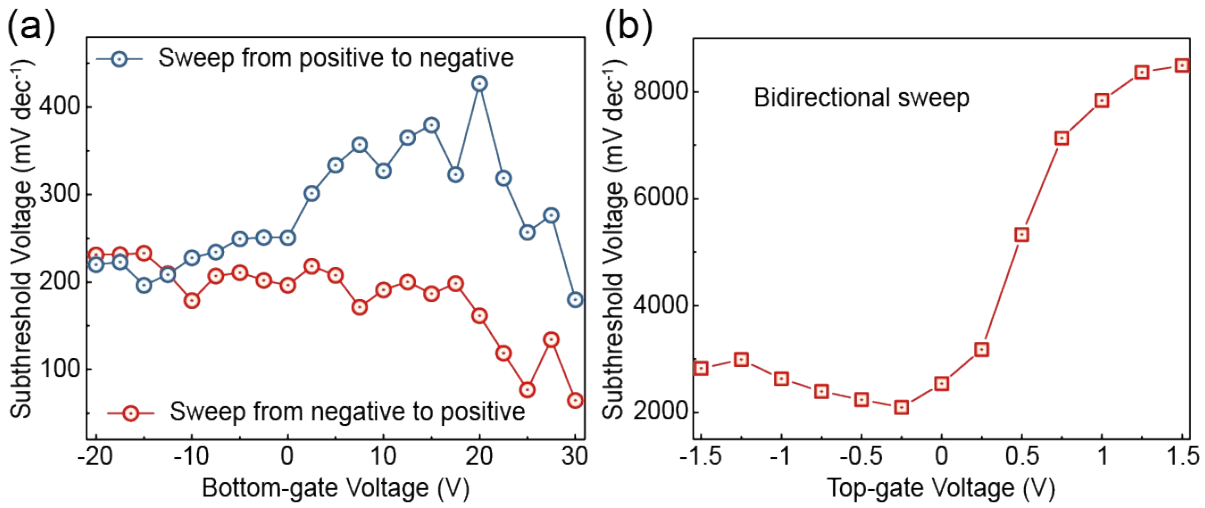

Fig. S1 The extraction of the variation of subthreshold swing (SS) with regard to different V_{bg} and V_{tg} from the static transfer characteristic curves of (a) top-gate and (b) bottom-gate respectively under bidirectional voltage scan. The two individual change tendencies of SS with the increment of BG biases are ascribed to the distinct shift of threshold voltage existing in a two-way sweep cycle applied on TG electrode.

Especially, the estimation of SS is based on the following Equation:

$$SS = \frac{V_{th} - V_{off}}{\log_{10} I_{th} - \log_{10} I_{off}}$$

where V_{th} represents the threshold voltage and I_{th} is defined as the corresponding current, I_{off} is objectively set as the value of 10^{-10} A and V_{off} denotes corresponding gate bias.

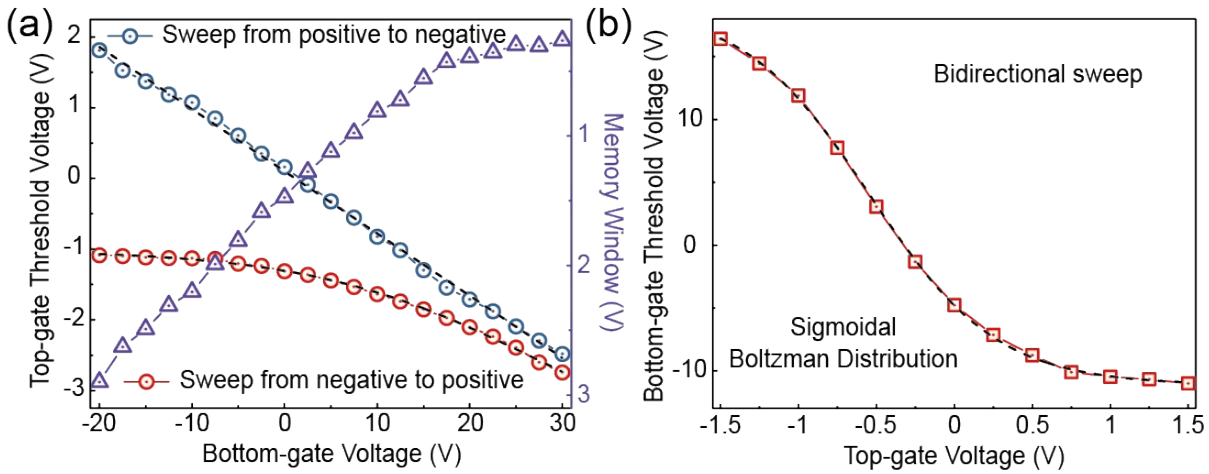

Fig. S2 The extraction of the variation of threshold Voltage (V_{th}) as a function of contrary gate biases from the transfer characteristic curves of (a) top-gate and (b) bottom-gate respectively during bidirectional voltage sweep.

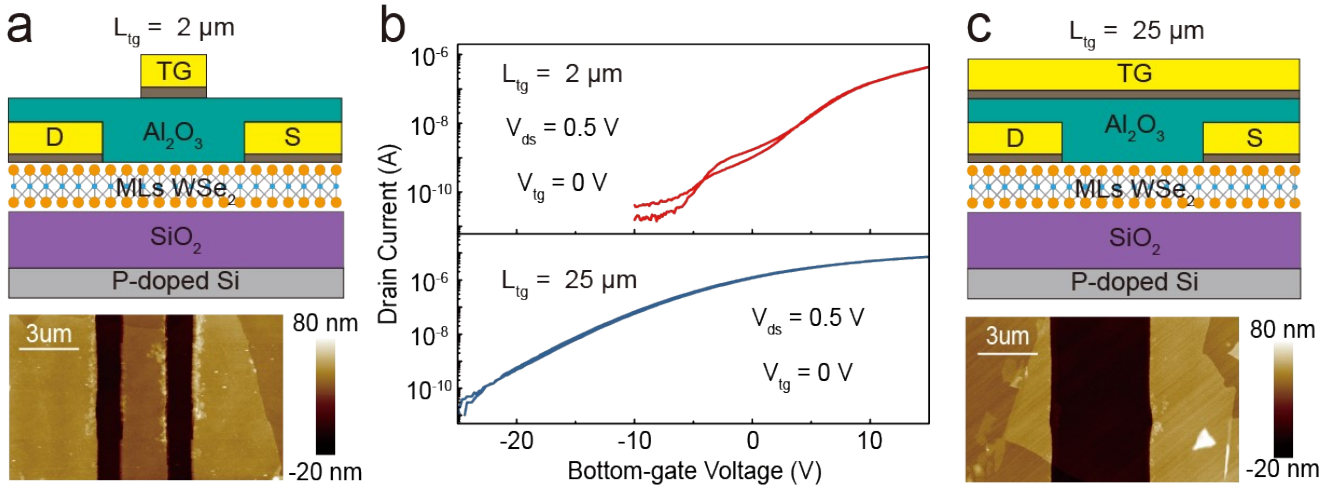

Fig. S3 The schematic of cross-sectional structure along with the morphology images by AFM measurements for two control dual-gate transistor devices with different top-gate lengths of (a) 2 μm and (c) 25 μm. (b) The corresponding static transfer characteristic curves for two control devices under the operation of bottom-gate. Noting that, similar to the prototypical device, neither of them exhibit obvious hysteresis.

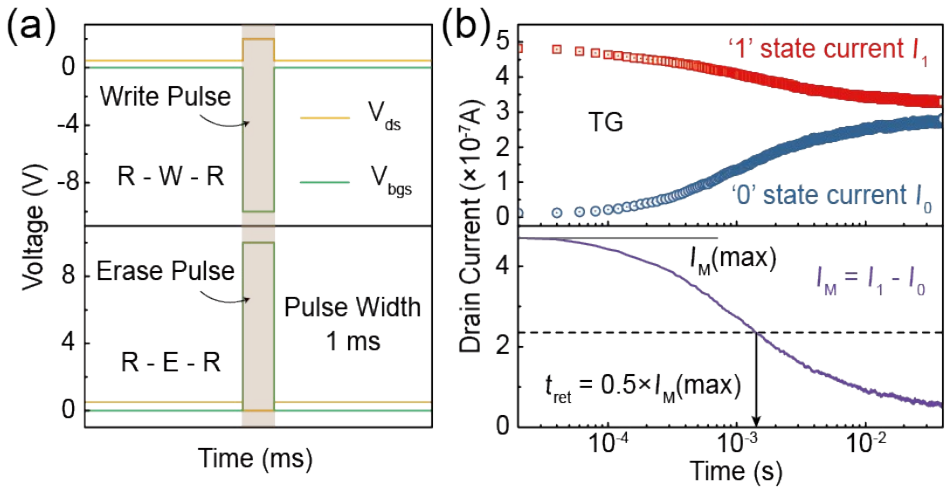

Fig. S4 (a) Upper Panel: the evolution of readout current instantly after both writing and erasing operation, corresponding to the state '1' and '0' respectively. Bottom panel: The sense margin between two distinct states to estimate the retention capability. (b) The voltage setting of single programming (writing/erasing) operation pulse along with persistent read operation on the bottom-gate terminal.

It should be distinguished that the evidently unequal degradation for state '0' and state '1' represent different variations of the amount of pristine body holes with regard to time in dissimilar effects. The decay of state '1' is attributed to the gradual recombination of non-equilibrium carriers that excess holes fleetly vanished in the boundary of homojunction, inducing the decrease of drain current. While the rebound of the population of minority carriers, which is primarily resulted from parasitic injection through gate induced drain leakage (GIDL) as well as indirect recombination (also known as Shockley-Read-Hall), interferes with the lifetime of state '0'. These effects disturbing the quantity of existing holes are eventually responsible for volatile performance of capacitor-less DRAM cells.

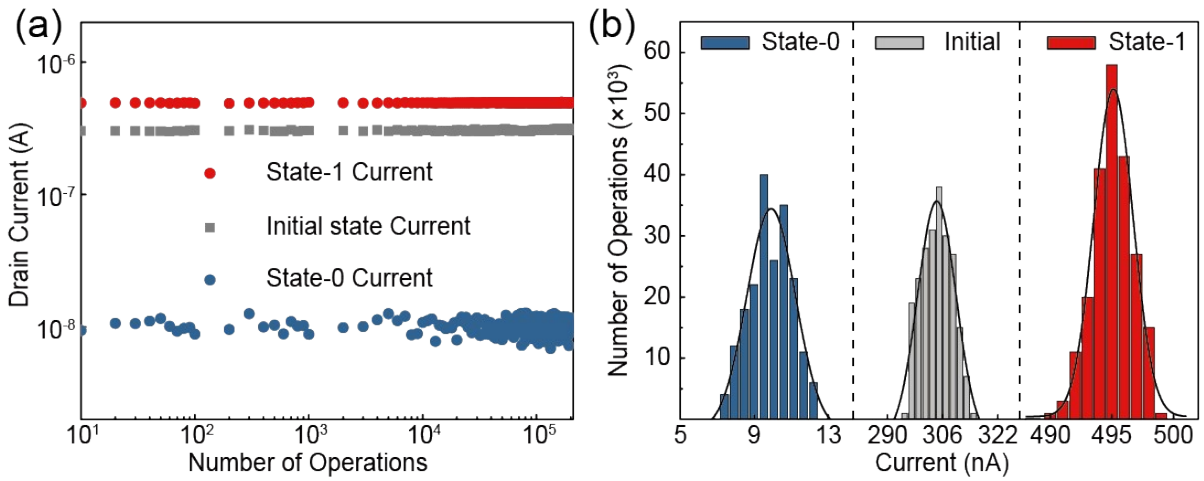

Fig. S5 (a) The characterization of endurance test and (b) corresponding Gaussian-shaped histograms distribution for initial state, state '0' and state '1'.

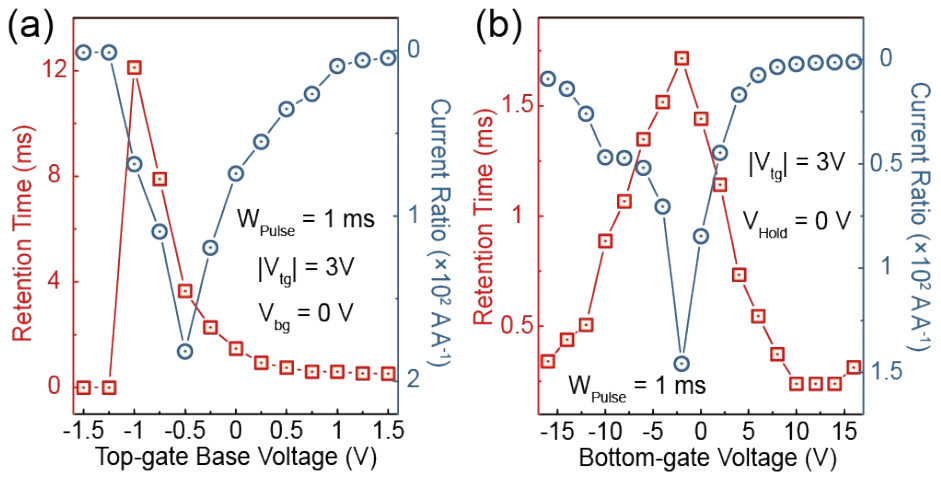

Fig. S6 The calculated values of retention time and current ratio after each programming (W/E) operation, which are extracted from the evolution of sense margin under diverse amplitude of (a) top-gate base voltage and persistent (b) bottom-gate voltage.

With the conversion of TG pulse base voltage from negative to positive, the retention time gradually drops since the potential well which prohibits the thermal recombination of holes is impacted by degrees and eventually falls into invalid with the stepwise increase of hold bias (Fig. S6a). With regard to the impact on current ratio, V_{tg} exhibits a non-monotonic modulation that a small negative bias can lead to a higher current proportion. Moreover, in consideration of capacitive effect between two channel interface, V_{bg} can also regulate the volatile memory characteristics by regulating the body potential.[9] As displayed in Fig. S6b, the retention characteristic exhibits an intricate nonmonotonic change with regard to the increment of bottom-gate voltage. For large positive V_{bg}, the restrained injection of holes by B2B tunneling within the front channel and shallow potential well for hole conservation degrade the retention time of state '1'. While if V_{bg} is sufficiently negative, the bottom channel interface would be thoroughly depleted, so that both W/E operations fail to induce the effective modulation of electron population within the back channel. The bottom-gate bias could modulate the ON/OFF ratio as well. On account of the complete depletion or abundant accumulation of back interface of body at tremendously positive or negative V_{bg}, the current ratio drops towards one (means no distinct memory behavior) in spite of the variation of hole population in the floating body after programming operation.

Order	Gate Operating Voltage	Switching Speed	power consumption	retention time	Endurance	Body Thickness	Body Materials	Source
1	-1 V	20 μs	~ 7 pJ	~ 2 ms	10^9 cycles	~ 20 nm	InGaAs	Ref[10]
2	-2.4 V	~ 10 μs	~ 0.24 pJ	~ 1 ms	——	70 nm	doped silicon	Ref[11]
3	-6 V	1 ms	——	~ 100 ms	——	40 nm	doped silicon	Ref[12]
4	-1.7 V	1 μs	~ 34 pJ	~ 20 ms	——	36 nm	doped silicon	Ref[13]
5	-1.75 V	~ 3 μs	~ 9 pJ	~ 20 ms	10^6 cycles	22 nm	doped silicon	Ref[14]
6	-10 V	10 ms	——	few ms	——	20 nm	doped silicon	Ref[15]
7	-1.6 V	50 ns	~ 0.2 fJ	~ 33 ms	——	10 nm	doped silicon	Ref[16]
8	-1 V	50 ns	——	~ 10 ms	——	30 nm	undoped silicon	Ref[17]
9	0 V	10 ns	——	few ms	——	20 nm	doped silicon	Ref[18]
10	0.5 V	40 ns	——	~ 1 ms	——	14 nm	doped silicon	Ref[19]
11	1 V	200 μs	~ 50 fJ	1 s	——	7 nm	MLs MoS_2	Ref[20]
12	3 V	10 ms	~ 80 fJ	1.26 s	——	3 nm	MLs MoS_2	Ref[21]
13	-3 V	50 μs	~ 60 fJ	~ 1 ms	10^5 cycles	~ 8 nm	MLs WSe_2	This Work

Table 1 A rough comparison of dynamic memory performance between this work (2D WSe_2 1T0C DRAM) and others based on SOI-MOSFET technology.

Compared with contemporary 1T0C DRAM unit cell based on the conventional SOI CMOS technology, the switching speed in our 2D WSe_2 1T0C DRAM unit cell is less competitive with part of them, which is partly attributed to the intrinsic restrictions in the accuracy of the test instrument and the performance of the built-in pulse generator. Nevertheless, the dynamic memory performance of our device can be further optimized in the future research work through adjusting the thickness of 2D channel dielectric layer or

varying the selections of different sorts of 2D semiconducting materials. In addition, the switching speed of our work is faster than the other two 2D DRAM cells with different architectures (2T or 1T1C), and the absence of additional gain cell allows it to improve the integration level in the large-scale integrated circuit. Therefore, this benchmark table review is able to guide us to further investigate the floating body effect on the 2D 1T0C DRAM system as well as optimize their performance for prospective roadmap in future research in depth.

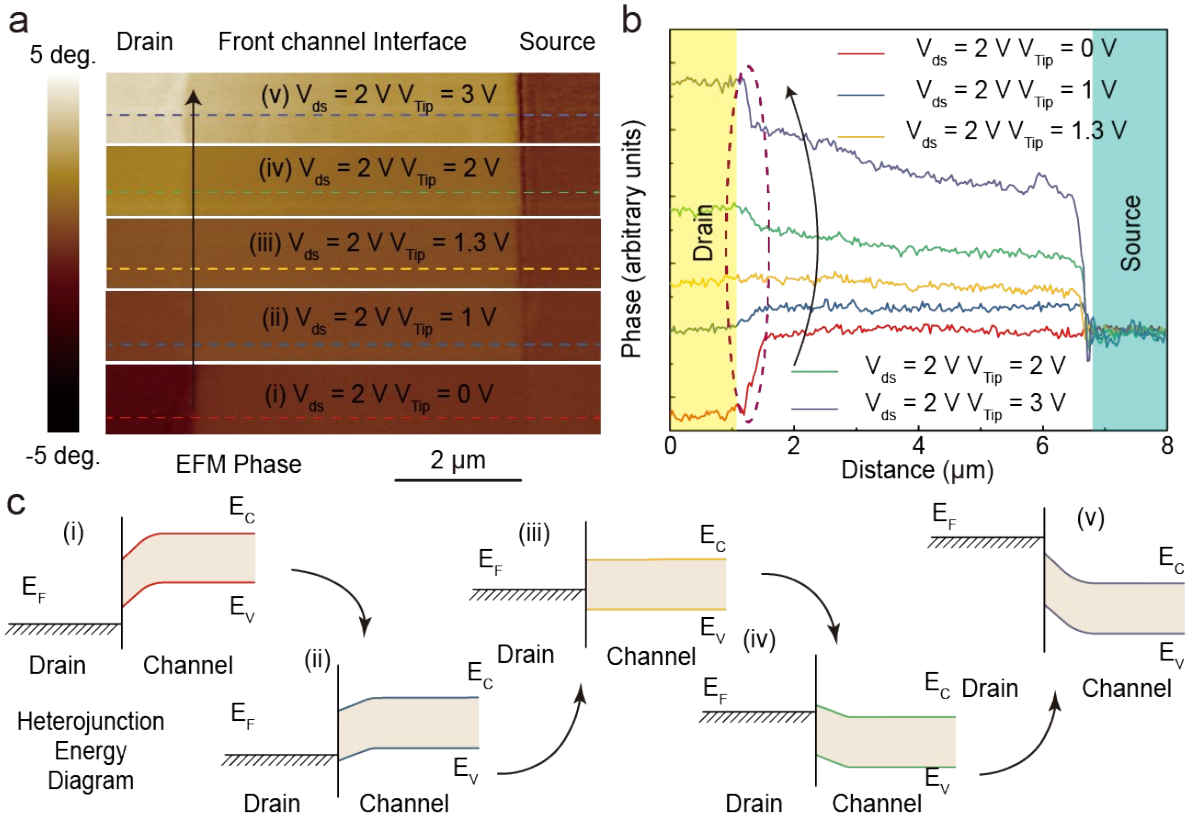

Fig. S7 The evolution of (a) 2D mapping of phase lag under various positive tip voltage biases and (b) the corresponding line profiles. (c) The relative changes of the energy band of 2D WSe_2 front channel compared to the drain electrode with the variation of plus tip voltage biases.

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