Supplementary Information for

Imidazole-based artificial synapses for neuromorphic computing: Cluster-type conductive filament via controllable nanocluster nucleation

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1. Characterization of the Polymeric Thin Film

We fabricated five different polymeric films that were copolymerised with V3D3 and VI monomers by controlling the flow rate of the monomers during iCVD. The monomer contents were analysed using an XPS survey. As shown in Fig. S1a, V3D3 contains three silicon atoms with no nitrogen, and VI contains two nitrogen atoms and no silicon atoms. Thus, the V3D3 and VI contents can be calculated using the atomic percentages of silicon and nitrogen. The equation used is as follows:

$$VI\ contents\ (\%) = 100 \times \frac{Atomic\ \%\ of\ N\ \div 2}{Atomic\ \%\ of\ N\ \div 2 + Atomic\ \%\ of\ Si\ \div 3}$$

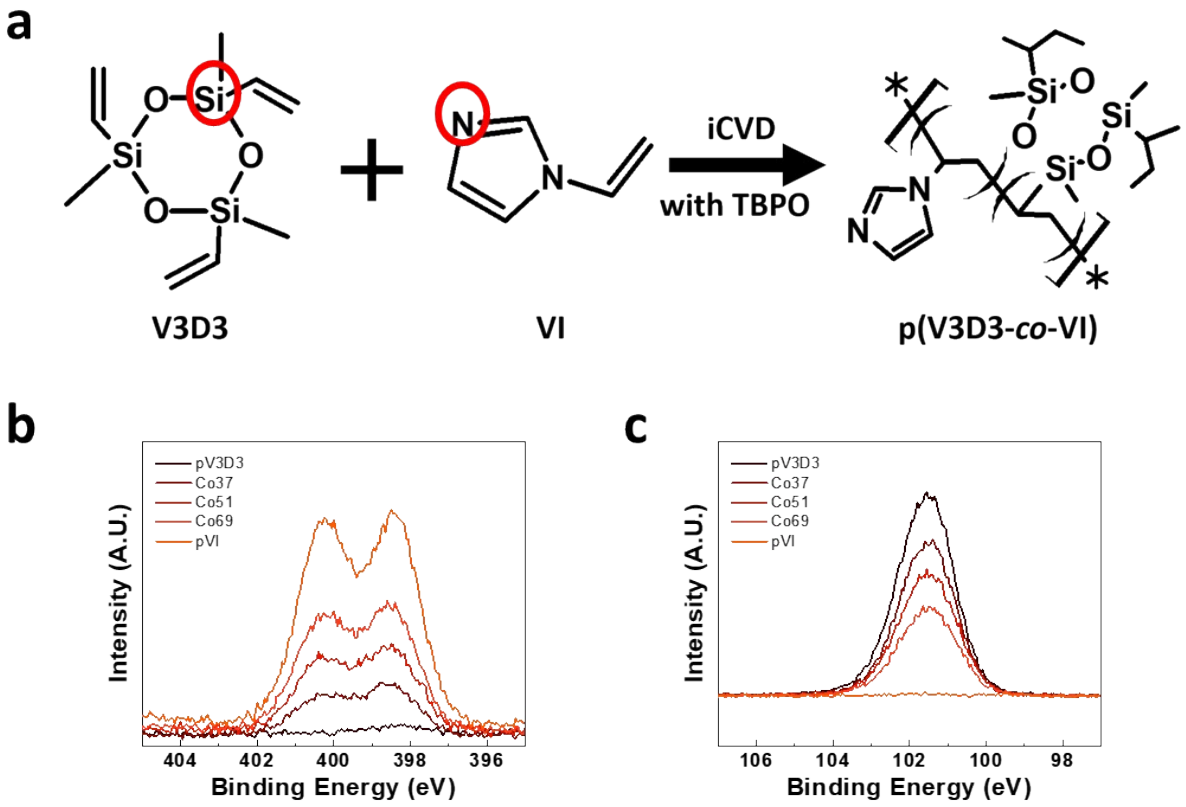

Fig. S1: Analysis of the composition ratio of copolymer thin films. (a) Synthetic scheme for the copolymer film. XPS analysis: high-resolution scans of (b) N1s and (c) Si2p of five polymeric films.

As the flow rate of VI increased, the N and Si content tended to increase and decrease, respectively. However, as the flow rate of V3D3 increased, the N and Si content tended to decrease and increase, respectively. Table S1 shows the content of each monomer, calculated by using the above equation. In this study, a p(V3D3-*co*-VI) memristor used a Co37 thin film, which is considered to have optimal VI content.

	pV3D3	Copolymer 1	Copolymer 2	Copolymer 3	pVI
Si (%)	21.0	14.9	12.7	8.6	
N (%)	0	5.97	8.8	12.6	20.4
VI Contents (%)	0	37.5	51.6	68.6	100

Table S1: A Summary of atomic percentages and VI contents of the five polymeric films.

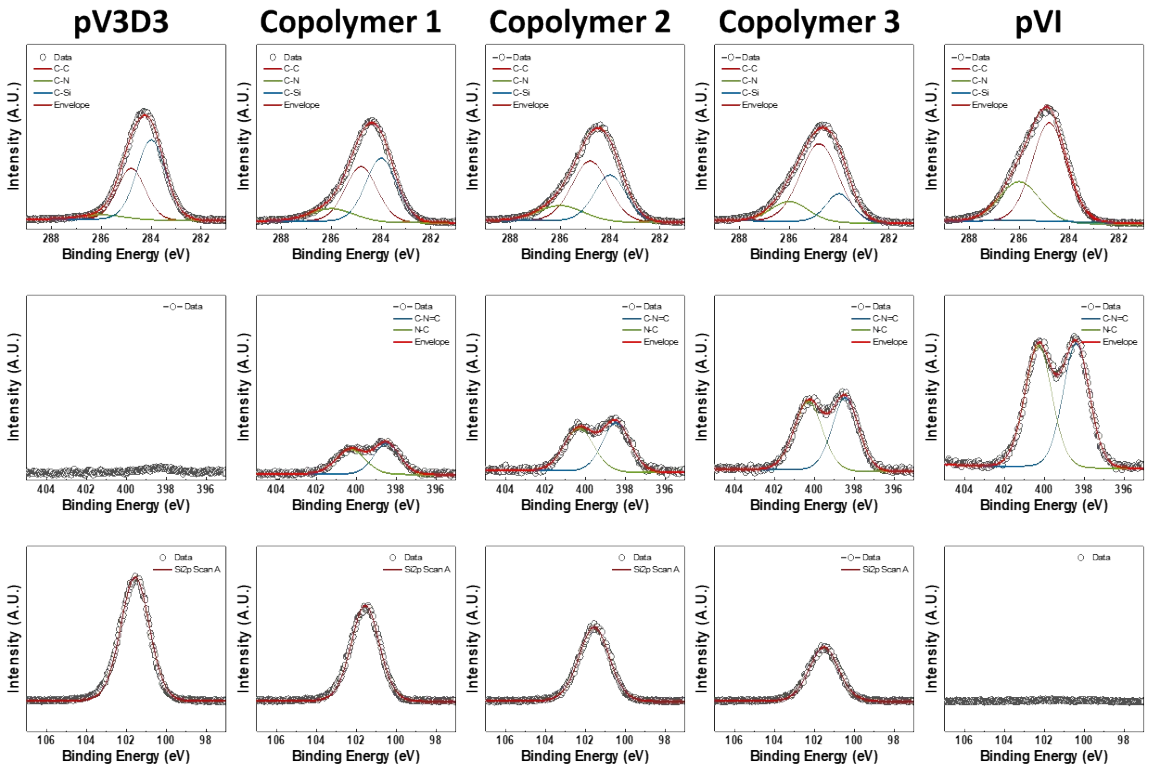

Fig. S2: XPS analysis of the polymeric films. High-resolution scans of C1s (top), N1s (middle), and Si2 (bottom). pV3D3, pVI, and three copolymer films are investigated, and the estimated VI contents of copolymers 1–3 were 37.5%, 51.6%, and 68.6%, respectively.

2. Long-Term Retention of the p(V3D3-*co*-VI) Memristor

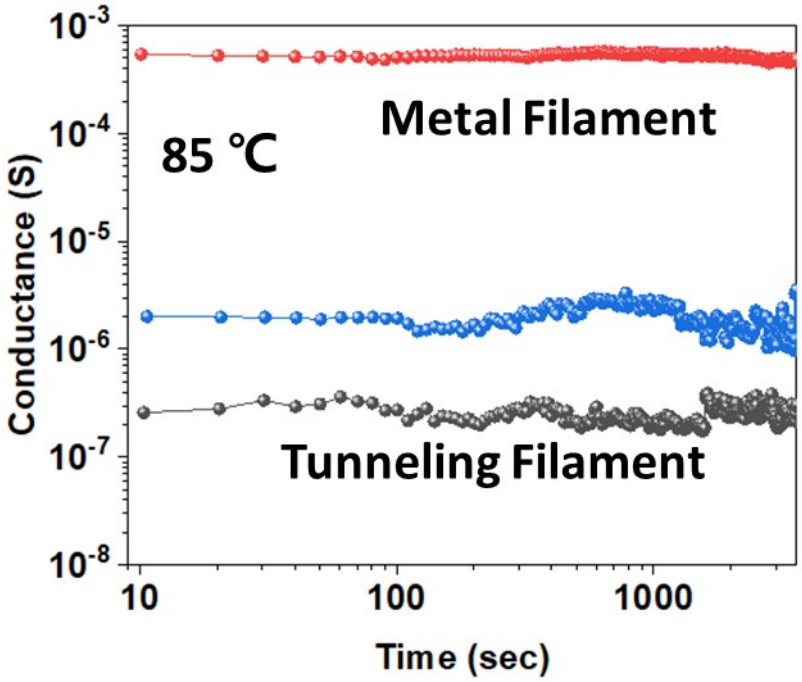

Fig. S3: Long-term retention stability test of the p(V3D3-*co*-VI) memristor at 85 °C.

3. Gradual Forming

The discharge of the parasitic capacitor connected in parallel to the memristor caused an overshoot current. When the memristor is switched from the HRS to the LRS with the I_{CC} level of the semiconductor-parameter-analyser system and the resistance is changed by more than two orders of magnitude, the discharged current from the parasitic capacitor flows through the memristor. If a high overshoot current flows through the memristor for a sufficiently long time to switch the memristor, the I_{CC} function is deactivated, and a large number of ions are injected. This eventually leads to the formation of a thick CF. Therefore, minimising the overshoot current by reducing parasitic capacitance is necessary. For this, we aimed to suppress a sudden change in resistance by gradually increasing the I_{CC} level. In this case, the response time of the parameter analyser system was still slower than the CF formation time; however, the minimised overshoot current did not exceed the I_{CC} level, preventing any unexpected filament growth. Fig. S4 shows the performance of a gradual-forming process of the p(V3D3-*co*-VI) memristor and the pV3D3 memristor.

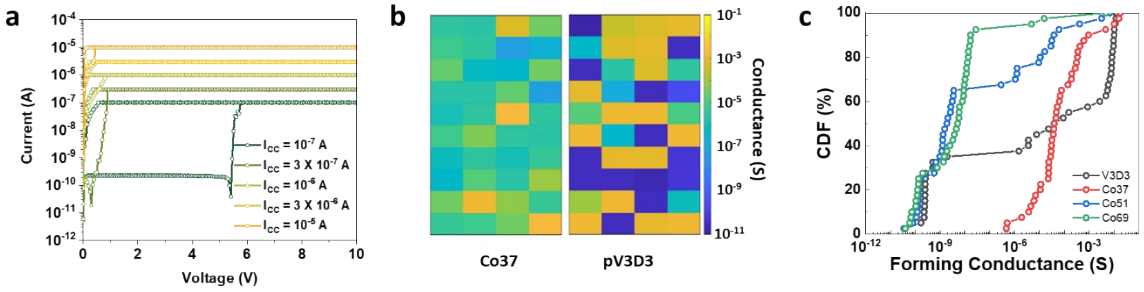

Fig. S4: (a) Gradual-forming process of the p(V3D3-*co*-VI) memristor. (b) Conductance maps after the gradual-forming process with maximum I_{CC} = 1 μA of the p(V3D3-*co*-VI) memristors and the pV3D3 memristors. (c) Cumulative distribution function of the forming conductance of the pV3D3 and p(V3D3-*co*-VI) memristors with different VI contents.

4. Switching Characteristics of Sub-Quantum Memristor

The p(V3D3-*co*-VI) memristors reported sub-quantum resistive switching with switching windows greater than 10^6 by using various I_{CC} at 200 nA, 500 nA, and 1 μA. However, pV3D3 exhibited a switching window of 10 or less. This difference can be attributed to the different morphologies of CF, which can be predicted using a conduction-mechanism analysis.

Since, among the memristors studied the p(V3D3-*co*-VI) memristor exhibits a wide dynamic range, understanding the conduction mechanism in the intermediate LRS state, as well as the HRS and LRS states, is necessary. Fig. S5c–d shows the reset process of the p(V3D3-*co*-VI) memristor with several data points of the intermediate LRS state. To understand the change in the conduction mechanism during the reset process, we confirmed the conduction mechanisms by using the slope of the $\ln(I/V^2)$-$1/V$ reset curves. In the $\ln(I/V^2)$-$1/V$ curve, direct tunnelling and F-N tunnelling had positive and negative slopes, respectively. Thus, predicting the CF collapse process of the p(V3D3-*co*-VI) memristor is possible. The CF of p(V3D3-*co*-VI) memristors initially exhibits direct tunnelling conduction, and the partial collapse of the tunnelling filament shows F-N tunnelling conduction because of the increased tunnelling gap, followed by a complete collapse. However, the pV3D3 memristor features only direct tunnelling during the reset, as shown in Fig. S5e.

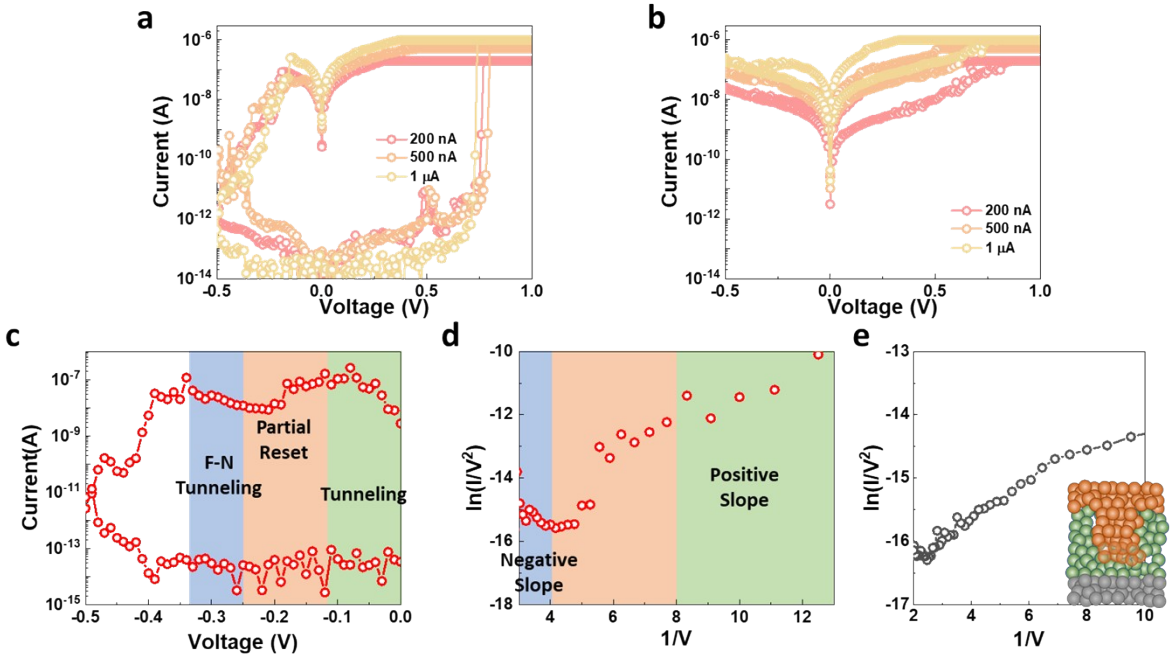

Fig. S5: Sub-quantum switching of (a) p(V3D3-*co*-VI) and (b) pV3D3 memristors. (c–d) Conduction mechanism change according to the CF collapse of p(V3D3-*co*-VI) memristor. (c) Current-Voltage and (d) $\ln(I/V^2)$-$1/V$ reset curves of the p(V3D3-*co*-VI) sub-quantum memristor. (e) $\ln(I/V^2)$-$1/V$ curve during the reset process of the pV3D3 memristor.

5. Switching Performance of the p(V3D3-*co*-VI) Memristor

The switching speed of the p(V3D3-*co*-VI) memristor was measured and is shown in Fig. S6. Since we measured the resistance state change with a 1 μs voltage pulse, we simultaneously measured the transition time from the high-resistance state (HRS) to the low-resistance state (LRS) and the CF potentiation/depression time due to the current offset (~ 30 μA) of the measuring equipment. As a result, we confirmed a set switching of 170 ns at a positive voltage of 3 V and reset switching of 100 ns at a negative voltage of −1.5 V. We expected digital switching to be faster than the measured switching time because it includes the HRS to LRS transition time and CF expansion/decay time.

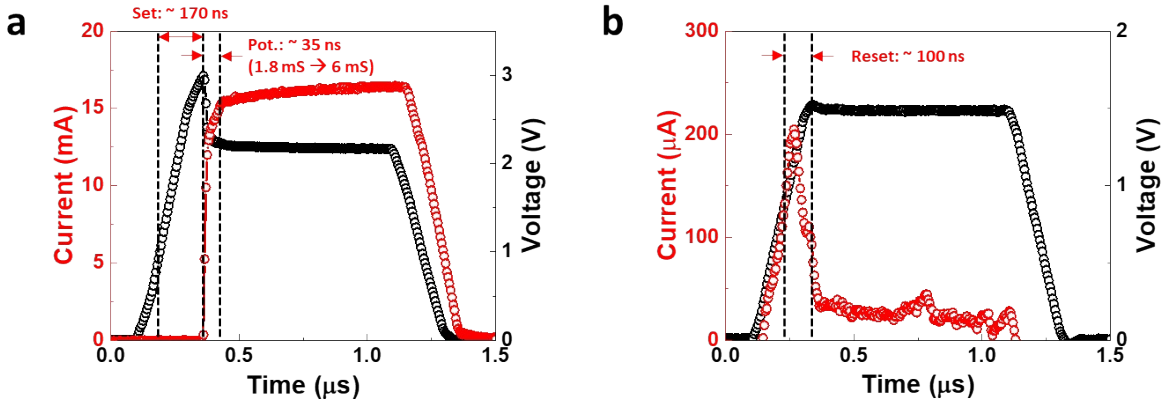

Fig. S6: (a) Set and (b) reset switching speed of the p(V3D3-*co*-VI) memristor.

Table S2 lists the low-power operation performance of the p(V3D3-*co*-VI) memristor. The p(V3D3-*co*-VI) memristor, which can maintain a low conductance at the LRS from several hundred nS to several mS, can operate the LRS conductance under 1 μS. The low-power operation performance of the p(V3D3-*co*-VI) memristor is estimated at 1 μS of the LRS through the switching speed measured in Fig. S6, with an energy consumption of 50 fJ / 20 fJ or less expected in the set/reset operation.

Device Structure	Strategy	Multi-level Retention	Nonlinearity	Switching Voltage (Set/Reset)	On/Off Ratio (Digital)	Switching Speed	Switching Energy (Set/Reset)	Analog Tunable Range
Cu/p(V3D3-*co*-VI)/Al (This Work)	CF morphology control by molecular engineering	4 states / >3.6×10^3 s @ 85 ℃ (Log conductance scale) 32 stats / 200 s (Linear conductance scale)	−0.23 / −0.99	1 V / −0.5 V	10^5 ~ 10^9	<170 ns / <100 ns (Digital)	50 fJ / 20 fJ (Digital) @ 1 μS	>10^4 (100 nS ~ 3 mS)
Ag/i-SiGe/p-Si [S1]	CF confine with line defect	1 state / 48 h @ 85 ℃	0.5 / −0.5	5 V / −3V	10^3	5 μs / 5 μs (Analog)	25 nJ / 1.5 nJ (Analog)	240
Ag-Cu/a-Si/p-Si [S2]	Alloy CF	6 states / >3.6×10^3 s @ 85 ℃ (Log conductance scale)	NA	3 V / −3 V	10^2	50 ns / 50 ns (Analog)	1.5 pJ / 1.5 pJ (Analog)	10^2
Ag/$Ti_{4.8\%}$:a-Si/Au [S3]	Doped Ti as nucleation site	3 state / >3.6×10^3 s @ 200 ℃ (Log conductance scale)	2.28 / −2.46	0.5 V / −0.5 V	10^2	1 μs / 1 μs (Analog)	1 nJ / 1 nJ (Analog)	2.4×10^2
Ru/Ta_2O_5/Pt [S4]	Ru CF	6 states / >1×10^3 s @ RT (Log conductance scale)	NA	0.7 V / −0.7 V	10^3	50 ns / 50 ns (Digital)	350 fJ / 1.75 pJ (Digital)	NA
Pt/Ag:TaO_x/TaO_x/Pt [S5]	Ag cluster doping	5 States / > 1×10^4 s @ RT (Log conductance scale)	NA	0.5 V / −0.5 V	10 ~ 10^4	60 ns / 70 ns (Digital)	30 fJ / 350 fJ (Digital)	NA
ZrTe/Al_2O_3/Ta [S6]	Semimetallic CF	NA	NA	2 V / −2 V	10^2	10 ns / 10 ns (Digital)	< 10 pJ / < 10 pJ (Digital)	10^2

Table S2: Summary of the electrical performance of filamentary switching CBRAMs with different strategies.

6. Resistive Switching of the pVI Memristor

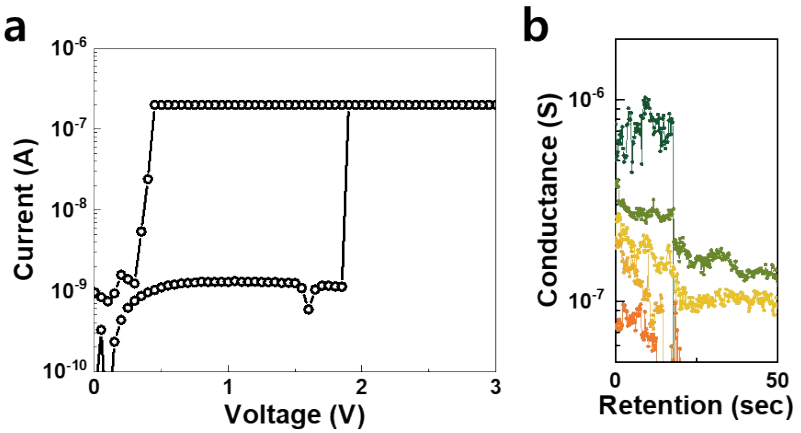

Fig. S7: Volatile resistive switching of Cu(50 nm)/poly vinylimidazole(15 nm)/Al(50 nm) memristors: a) Resistive switching and b) retention.

7. Read Variation of the Sub-Quantum Filaments

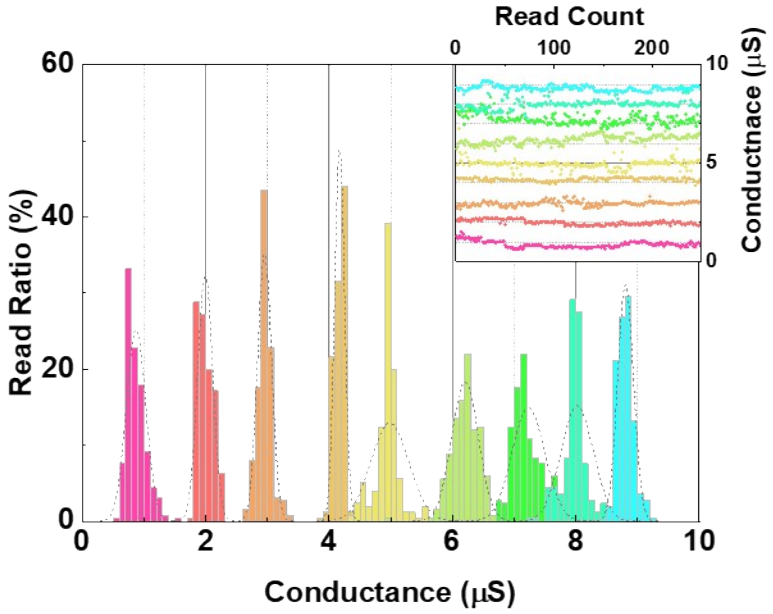

Fig. S8: Analog read fluctuation of the p(V3D3-*co*-VI) memristor in the sub-quantum region with 0.1 V read voltage and 250 read cycles. Inset shows the conductance state for each read count.

8. Polymeric Memristors with Ag Active Electrode

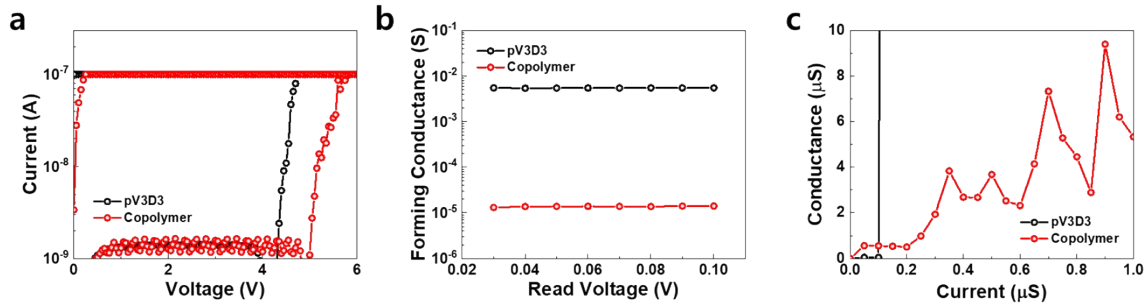

Fig. S9: Resistive switching of Ag(50 nm)/pV3D3(15 nm)/Al(50 nm) and Ag(50 nm)/ p(V3D3-co-VI)/Al(50 nm) memristors: a) Forming, b) forming conductance and conductance modulation under current sweep.

9. Device-to-Device Variations of the PD Curves

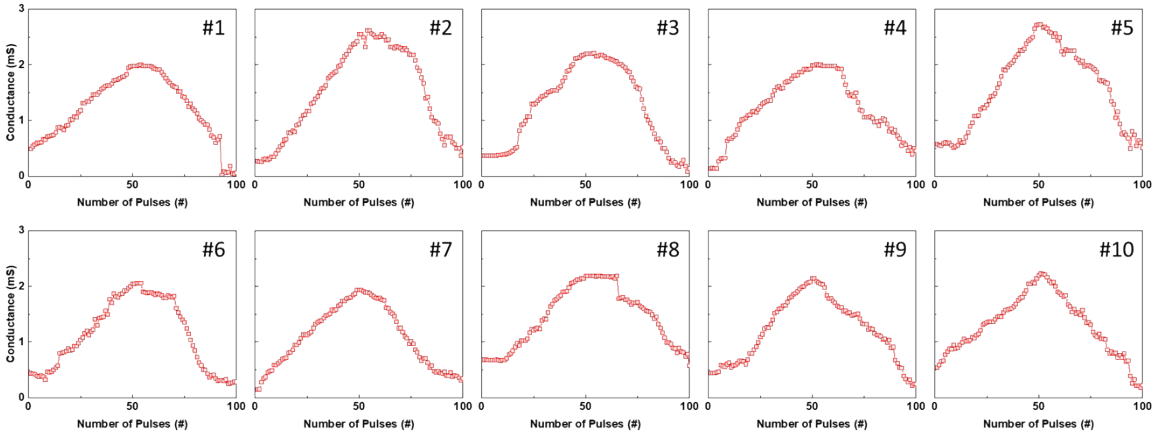

Fig. S10: PD curves of the p(V3D3-*co*-VI) memristors from 10 representative devices.

10. State Retention in the Synapse Array

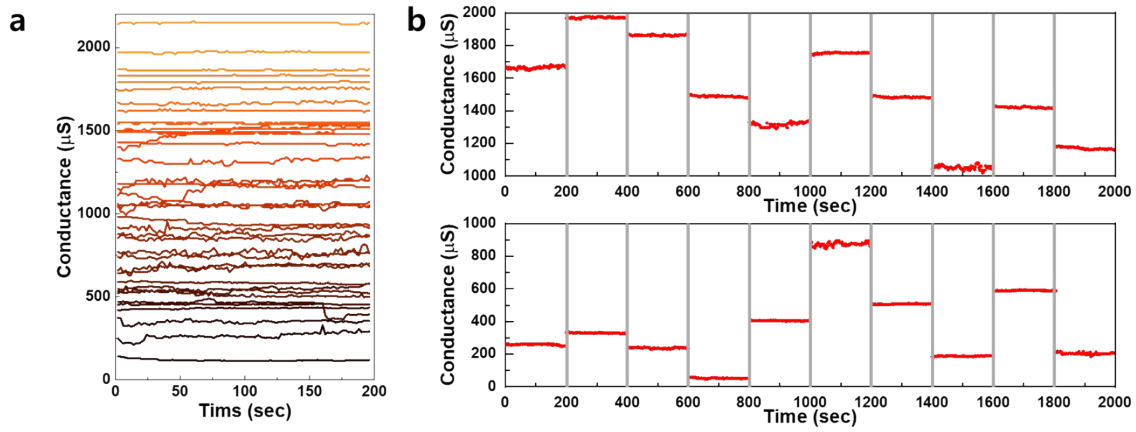

Fig. S11: State stability the p(V3D3-co-VI) memristor. (a) Randomly chosen 40 conductance state retentions of 20 p(V3D3-co-VI) memristors. (b) State retention of a p(V3D3-co-VI) memristor under 20 successive conductance updates. Gray line indicates conductance update.

References

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