Electronic Supplementary Information for

Image Processing with Multi-level Ultra-fast Three Dimensionally Integrated Perovskite Nanowire Array

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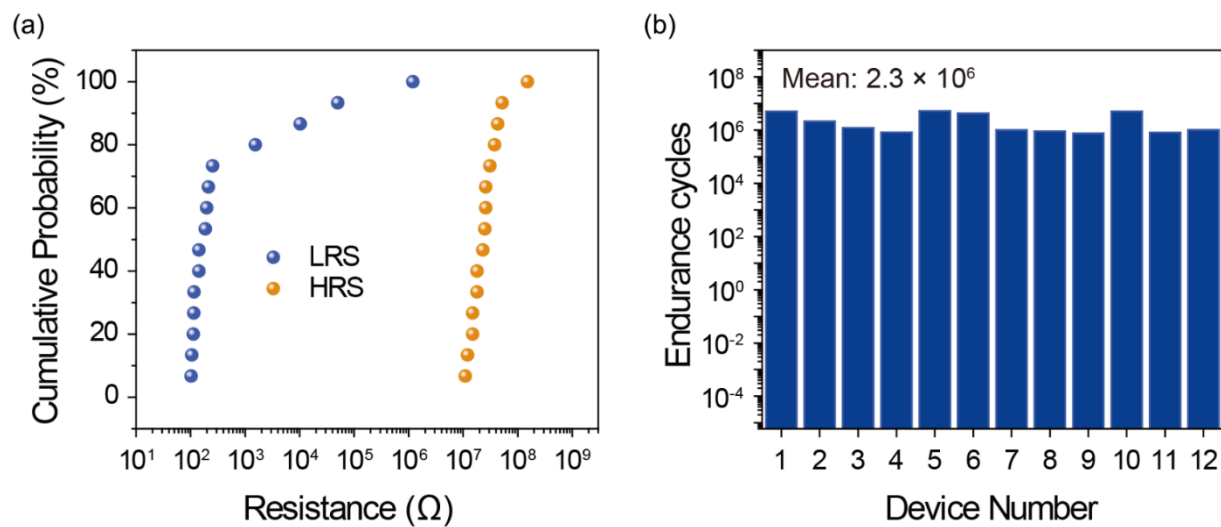[*]Corresponding author email: eezfan@ust.hk ; ztsong@mail.sim.ac.cn

'†'These authors contributed equally to this work.
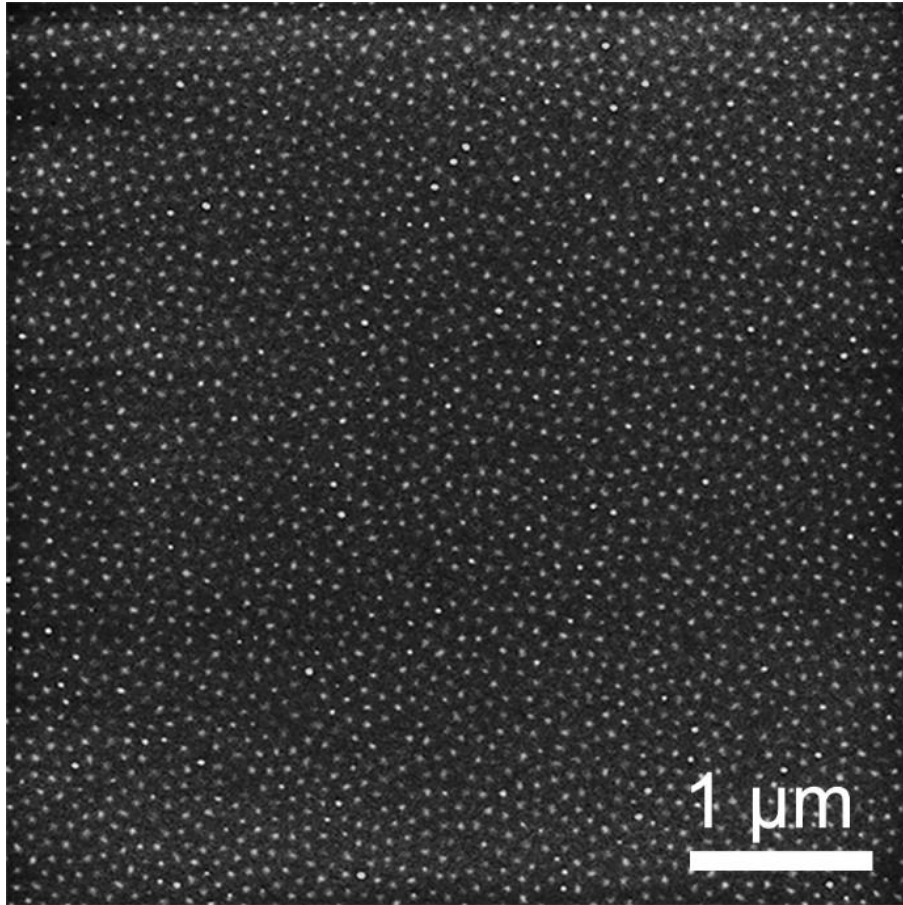
Fig. S1 Top view of MBI NW array in the PAM demonstrating almost 100 % filling ratio.
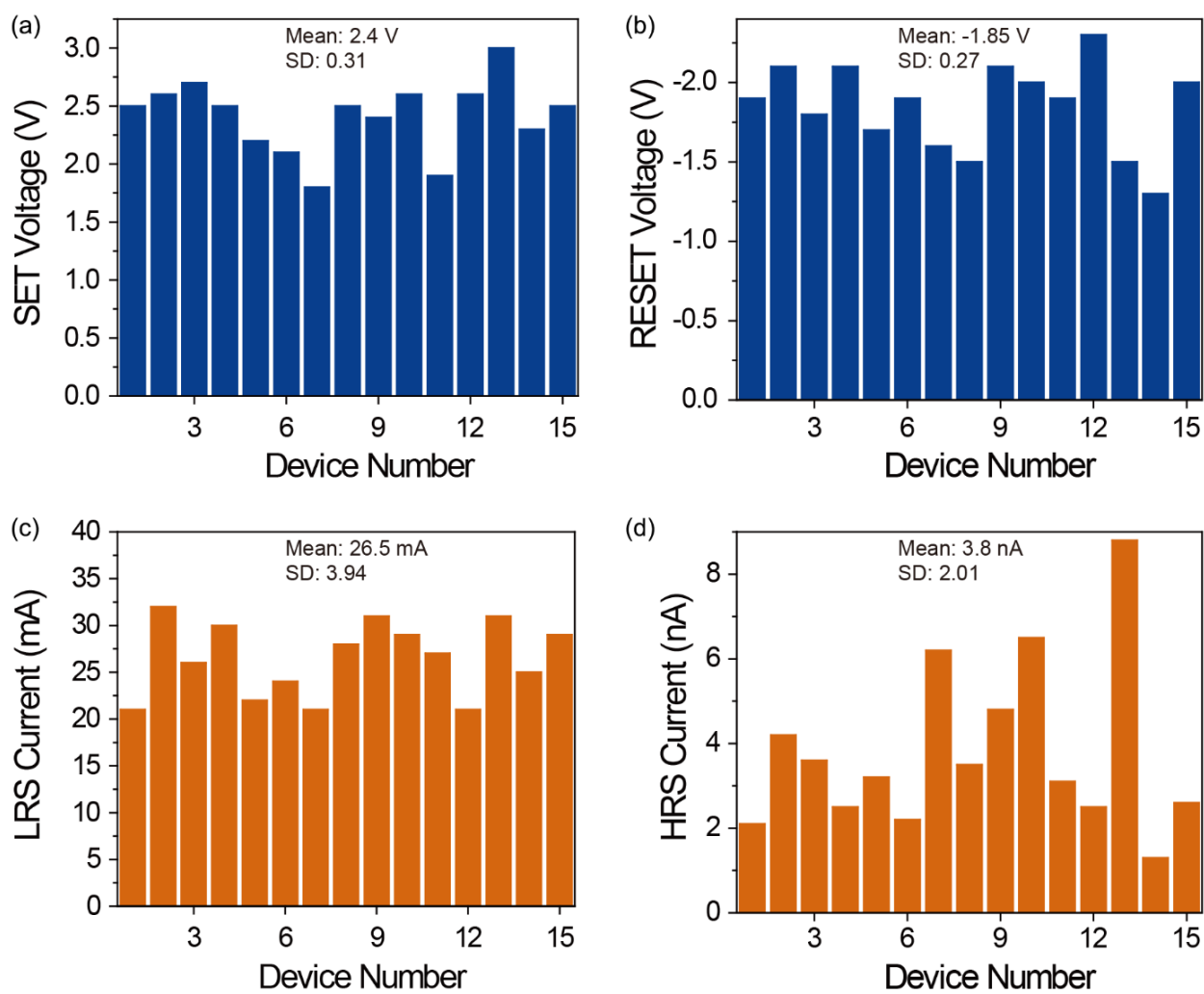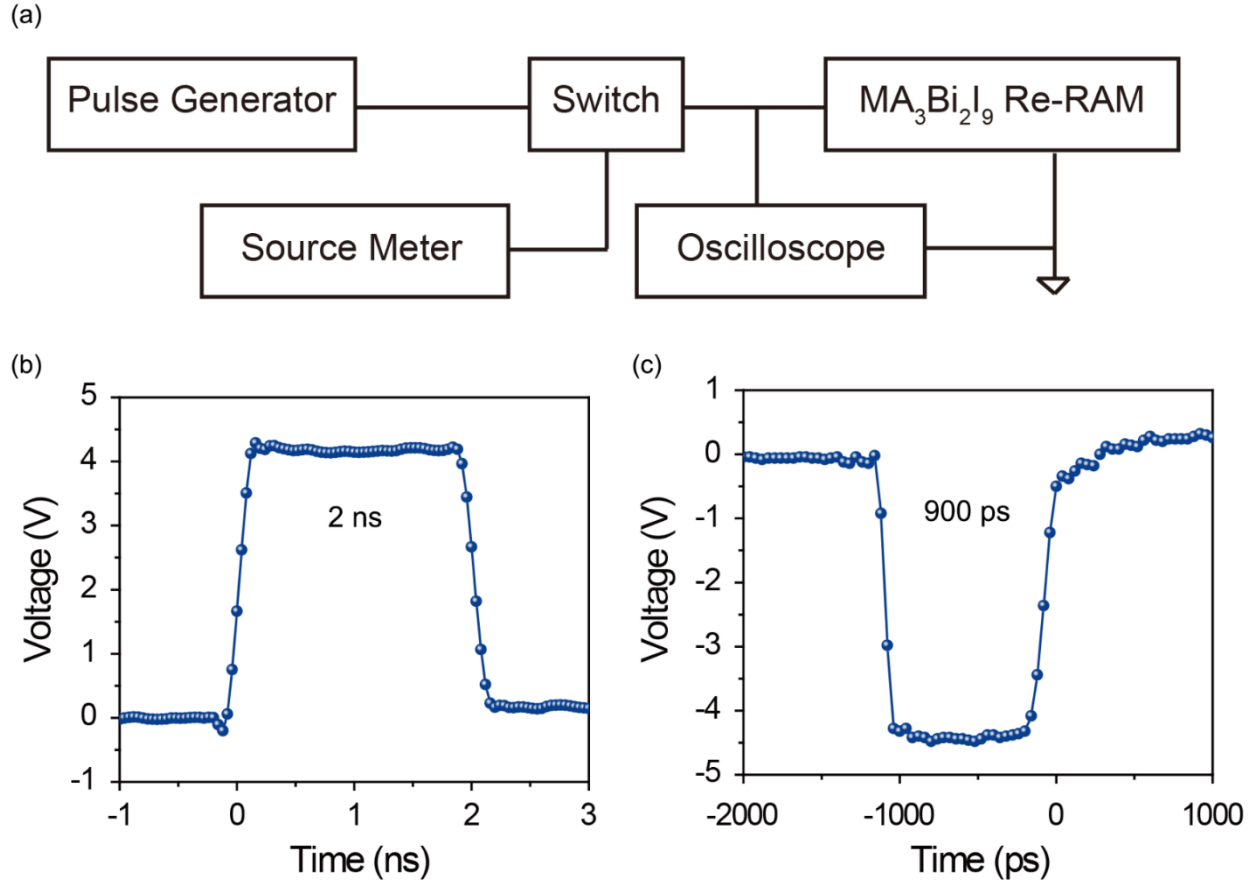
Fig. S2 (a) SET voltage variation of MBI NW Re-RAM. (b) RESET voltage variation of MBI NW Re-RAM. (c) LRS current variation of MBI NW Re-RAM. (d) HRS current variation of MBI NW Re-RAM.

Fig. S3 (a) Cumulative Density Function (CDF) plot of MBI NW Re-RAM. (b) Statistical variation of device cyclic AC endurance for MBI NW Re-RAM.
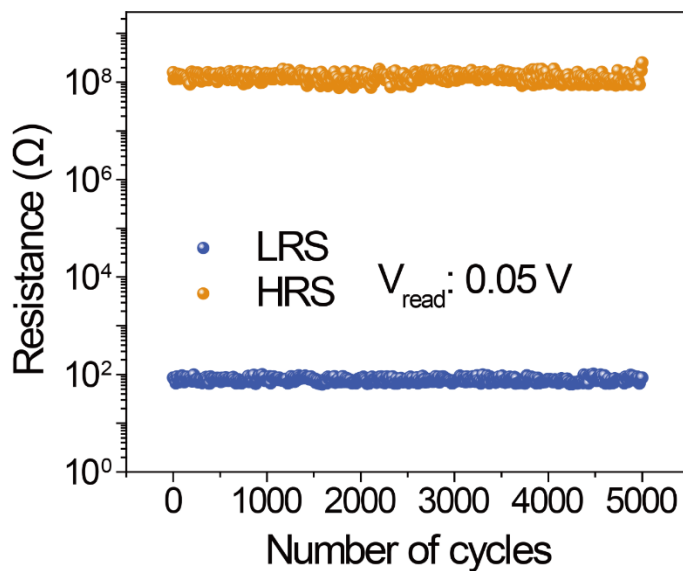
Fig.S4 DC endurance performance of MBI NW Re-RAM.

Fig. S5 (a) Schematic of circuit design utilized for switching speed measurement of MBI NW Re-RAM. (b) Plot showing the fastest writing source pulse of 2 ns width for MBI NW Re-RAM. (c) Plot showing the fastest erasing source pulse of 900 ps width for MBI NW Re-RAM.
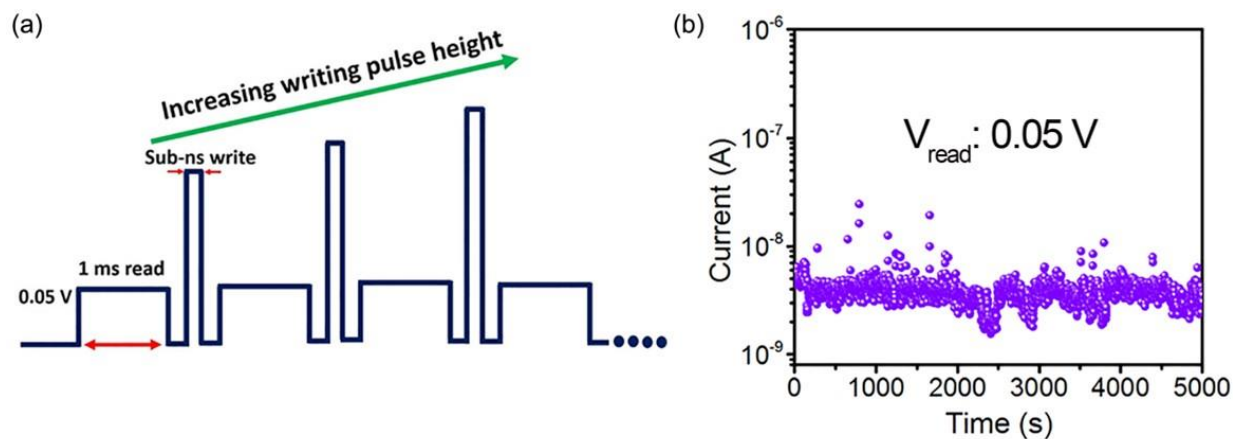
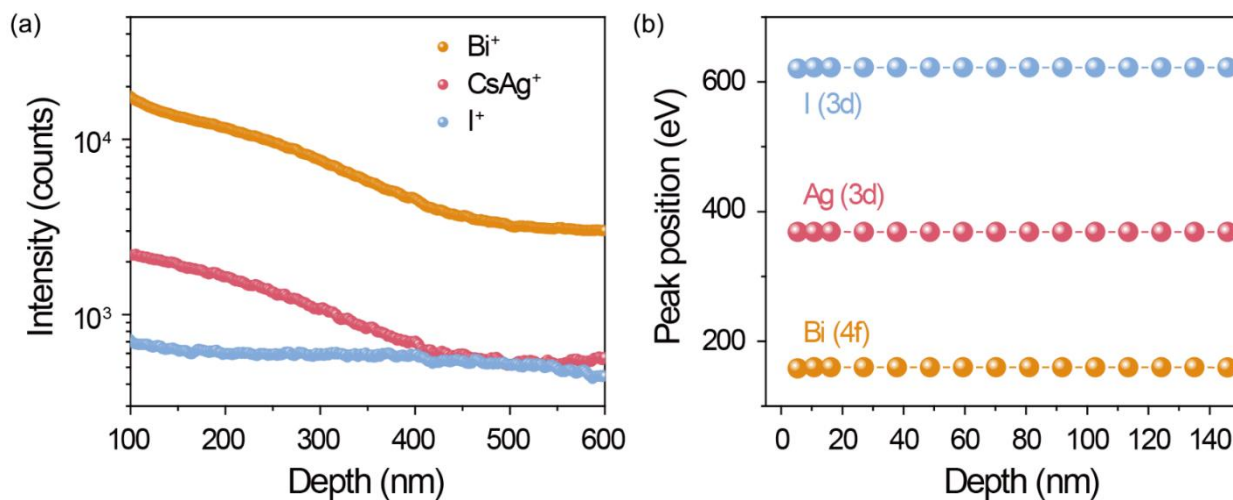**Fig. S6** (a) Schematic illustrating the pulse train used in switching speed measurement. (not drawn to scale). (b) DC mode stress test of MBI NW Re-RAM with read voltage of 0.05 V.

Fig. S7 (a) ToF-SIMS depth profile of bismuth, silver and iodine secondary ions in MBI PNW Re-RAM. (b) XPS depth profile depicting the binding energy peak positions of I (3d), Ag (3d) and Bi (4f) in MBI PNW exhibiting no peak position shift during the milling process.
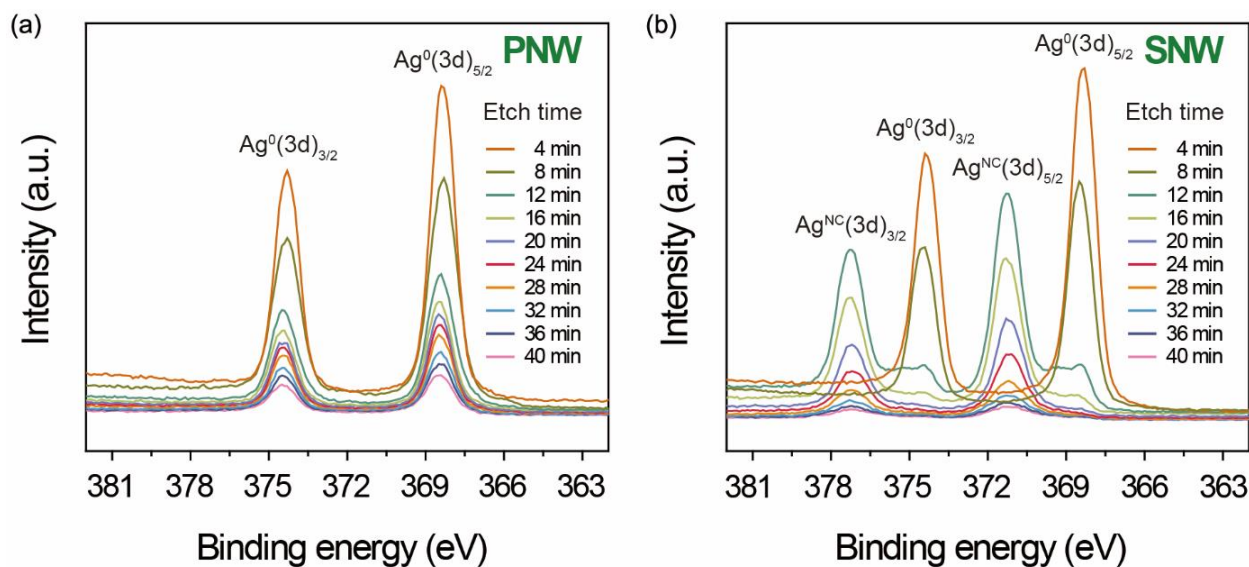
Fig. S8 (a) XPS spectrum of MBI PNW exhibiting no binding energy peak shift with vertical Ar etching. (b) XPS spectrum of MBI SNW showing binding energy upshift originating at the Ag/MBI SNW interface, indicating transformation of Ag morphology from bulk to nanoclusters.
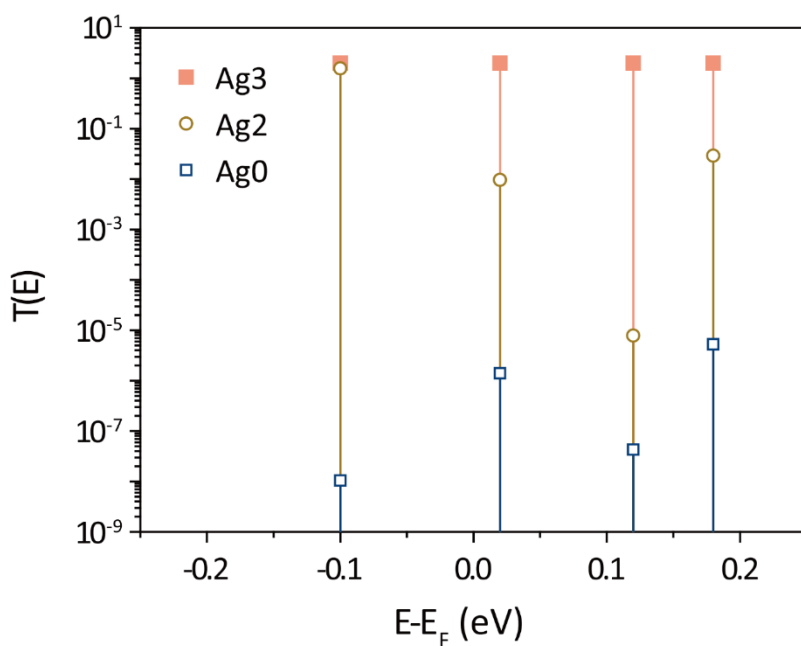
Fig. S9 Transmission co-efficient spectrum of MBI NWs with varying number of intruded Ag atoms in the scattering region.
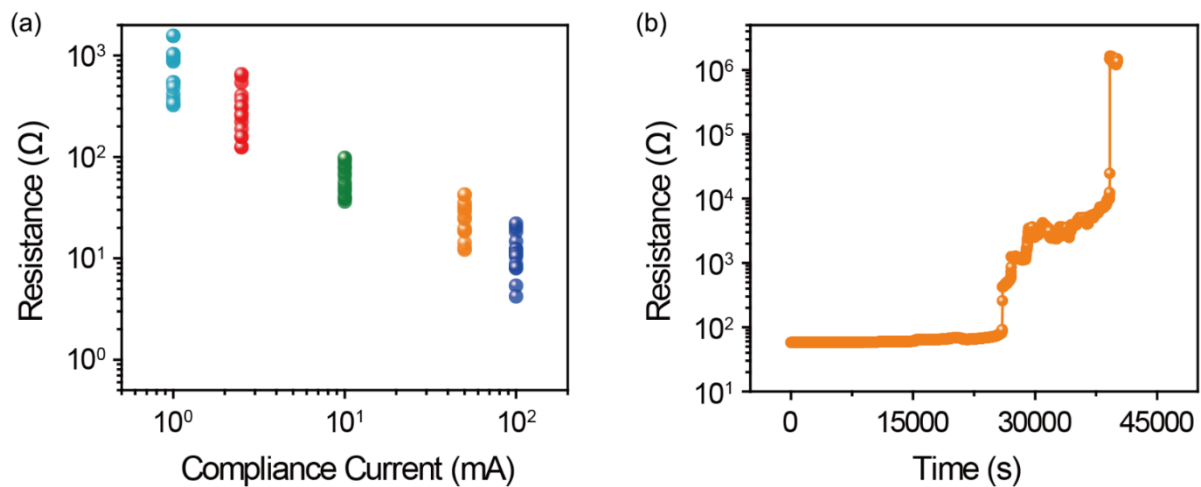
Fig. S10 (a) LRS states of 15 different MBI thin-film Re-RAMs obtained by operating under different current compliances. (g) Plot showing temporal retention of LRS in MBI thin-film Re-RAM.
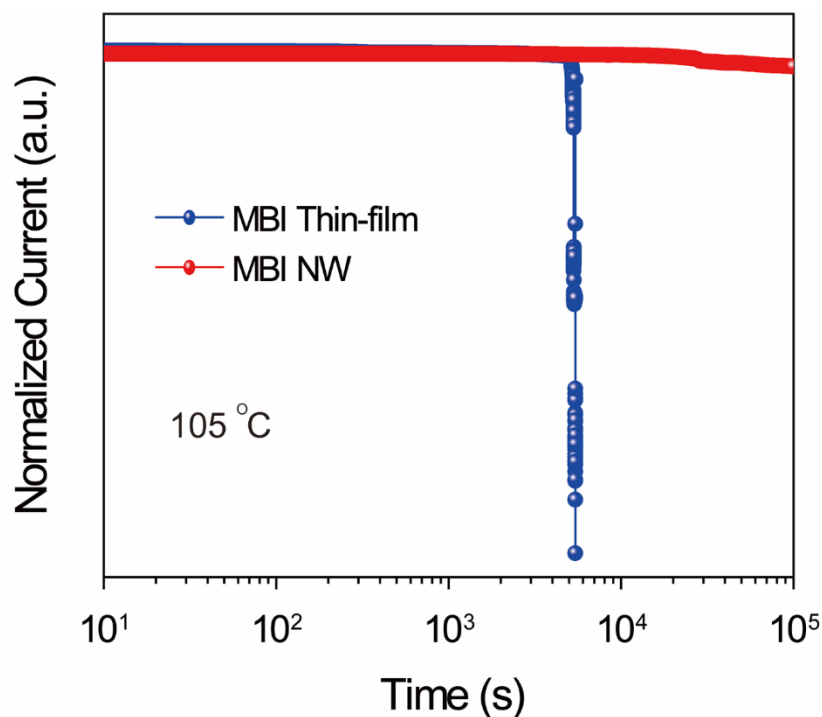
Fig. S11 High temperature comparative retention of MBI NW and thin-film devices.

Fig. S12 (a) Multilevel behavior exhibited by the MBI NW Re-RAM with varying pulse height. The width of the pulses were fixed to 150 ms. The erasing voltage and read voltage used were − 9V and 0.05 V respectively. (b) Statistical study of LRS currents read at a voltage of 0.05 V f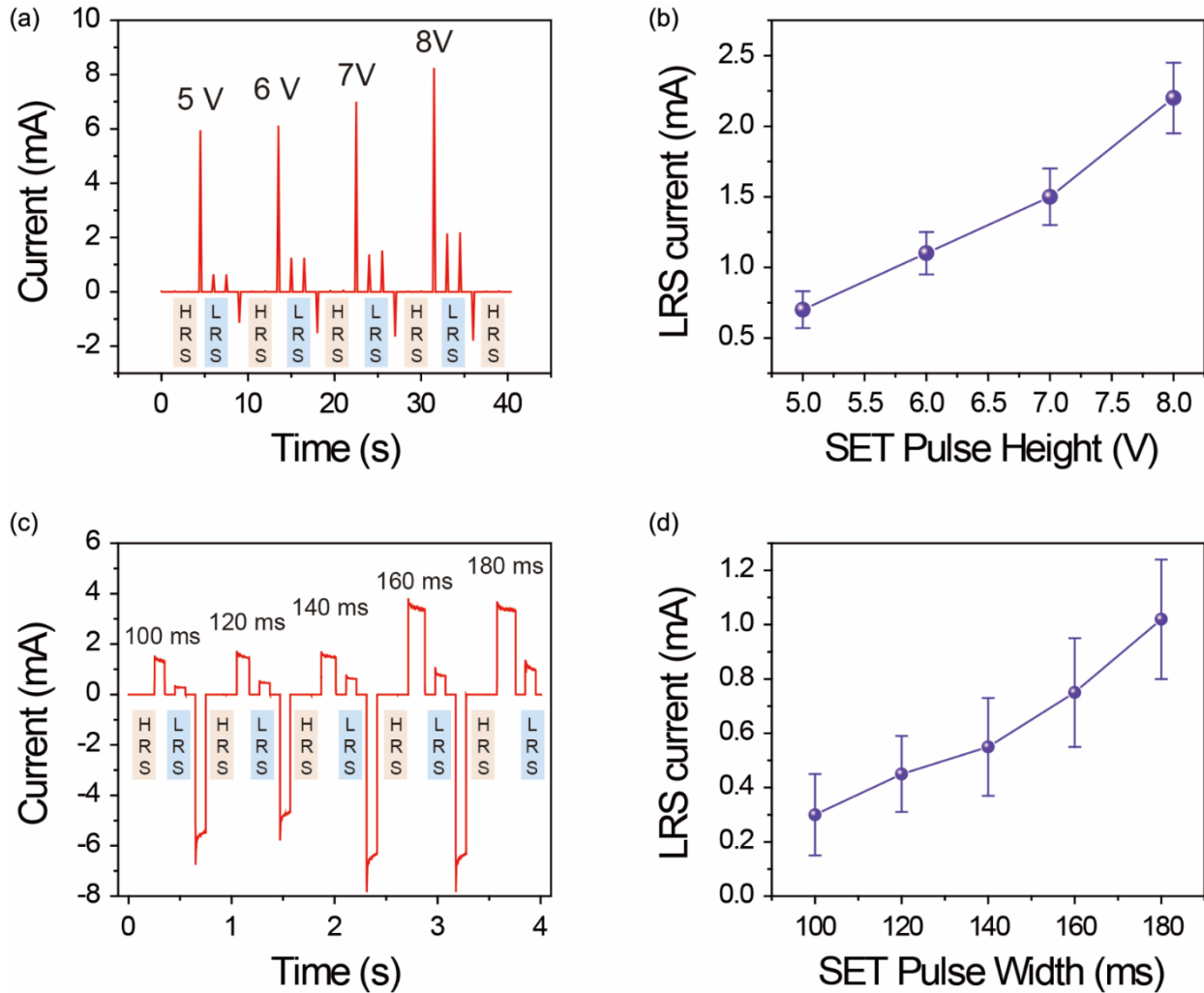or varying writing pulse height for a batch of 15 devices. (c) Multilevel behavior exhibited by the MBI NW Re-RAM with varying pulse width. The height of the writing pulses were fixed to 5 V. The erasing voltage and read voltage used were − 9V and 0.05 V respectively. The width of the erasing and read pulses were 100 ms. (d) Statistical study of LRS currents read at a voltage of 0.05 V for varying writing pulse width for a batch of 15 devices.
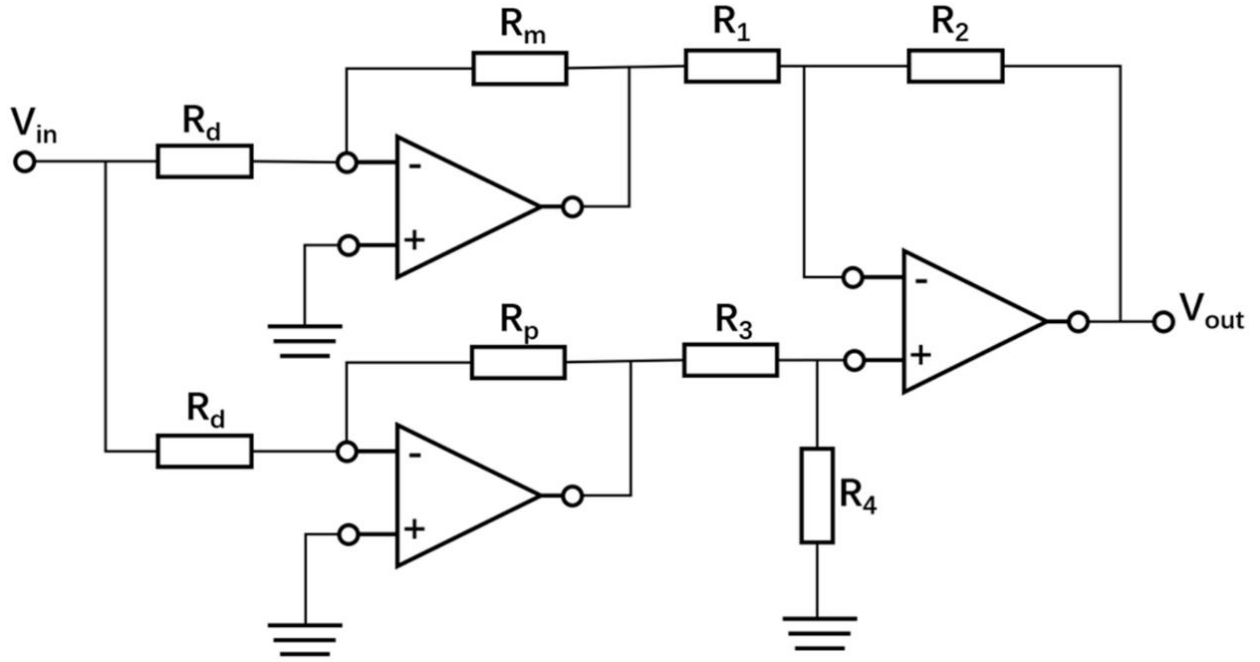
Fig. S13 Weights transfer circuit for implementing image processing task with the MBI NW Re-RAM.

V_{in} is pixel of input image, V_{out} is pixel of output image. To achieve image processing with 3*3 MBI Re-RAM convolutional kernel, the weights transfer circuit used, is shown in Fig. S13 above. In the circuit, R_m is the resistance of MBI NW Re-RAM, and $R_1 = R_2 = R_3 = R_4$. V_{out} is calculated as :

$$V_{out} = V_{in} \frac{R_m - R_p}{R_d}$$

where R_p and R_d are determined by function of convolutional kernel, V_{in} and V_{out} represent the pixel of input image and output image respectively. Let K_m be the 3*3 memristor convolutional kernel, and $K_m[n,m]$ is the value of kernel pixel at row n and column m. For different image processing functions, the value of R_p and R_d were calculated according to the rule stated below.

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Emboss: (the position of R_d and R_m needed to be switched)

$$R_p = \left(\left(\sum K_m\right) - K_m[2,2]\right)/8$$

$$R_d = K_m[2,2] - R_p$$

Outline: (The output pixel of outline function was reversed for better visualization, representing 0 by white color)

$$R_p = \left(\sum K_m\right)/9$$

$$R_d = R_p - \left(\left(\sum K_m\right) - K_m[2,2]\right)/8$$

Sharpen:

$$R_p = \frac{(K_m[1,1] + K_m[1,3] + K_m[3,1] + K_m[3,3])}{4}$$

$$R_d = \left(\sum K_m\right) - 9 * R_p$$

After pixel of input image was converted to the pixel of output image, convolution operation by scanning the whole image was performed with 3*3 MBI NW Re-RAM convolutional kernel. A single output pixel was obtained by summing up the 3*3 input pixels accordingly.
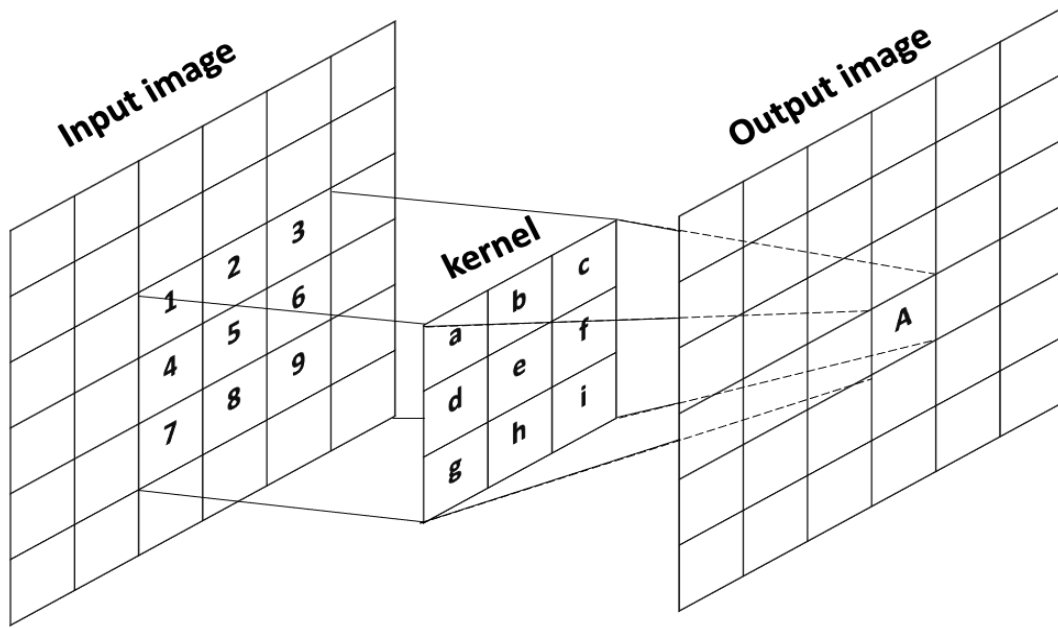
Fig. S14 Diagram of image processing by convolution kernel.

Convolution kernel, including edge detection, embossing, sharpening, is a small matrix in image processing. It focuses on processing and extracting local features of target images. The multiplication between the input images and convolution Kernel extracts the information in the frequency domain. Fig. S14 describes the convolution operations. Firstly, the convolution Kernel can be regarded as the weights of deep neural network. While scanning the Kernel on the input images from left to right and from top to bottom, the weights of this Kernel remain unchanged, and the pixel A of output image is calculated as:

A = 1*a+2*b+3*c+4*d+5*e+6*f+7*g+8*h+9*i

Depending on the element values, a to i, in the expression above, a Kernel can achieve different effects, including embossing, outlining and sharpening.
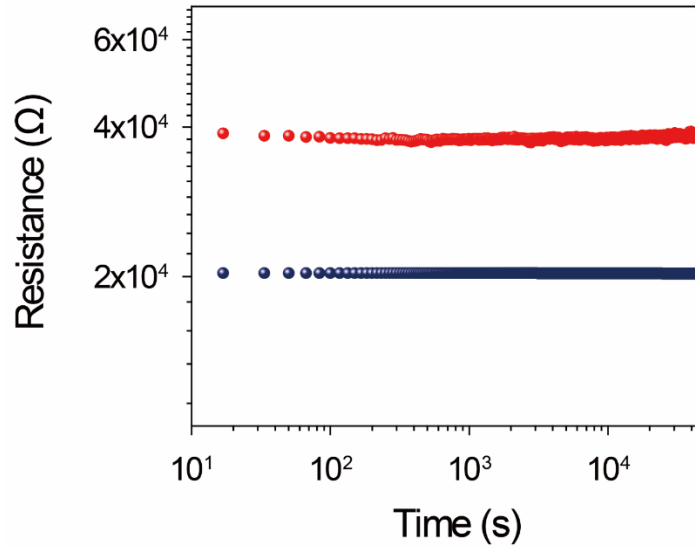
Fig. S15 Temporal retention of 2 states outside the 10 Ω - 2 kΩ range for the MBI NW devices.
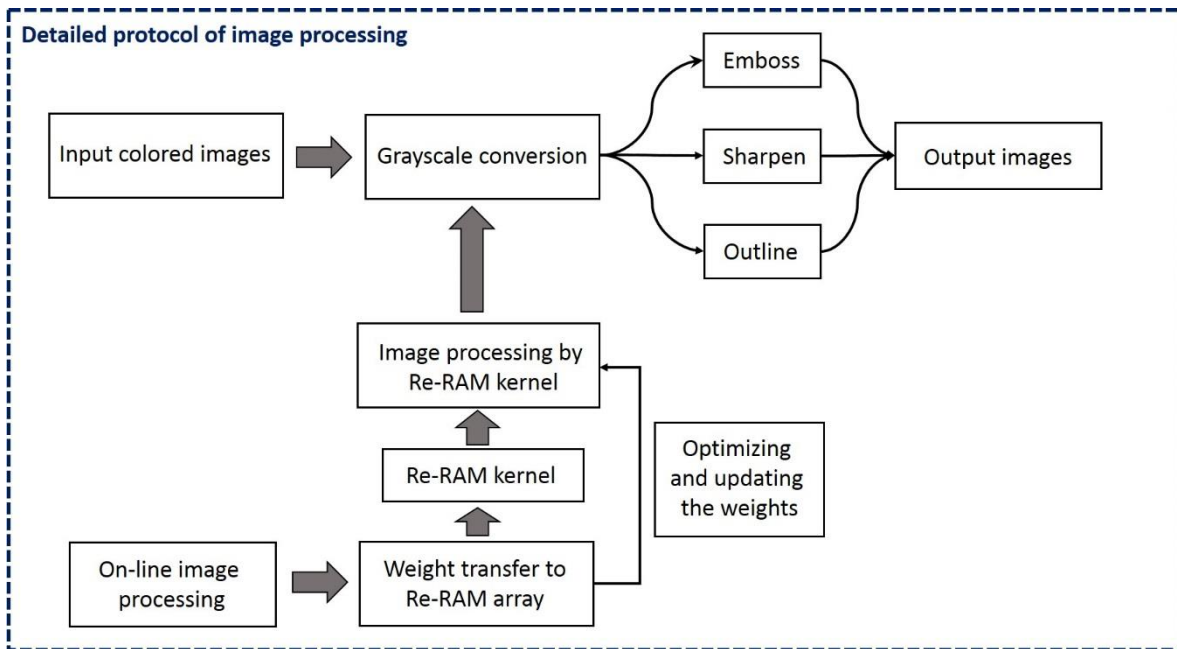
Fig. S16 Flow chart depicting the image processing implementation with the MBI NW Re-RAM. On-line image processing refers to obtaining the weights with the assistance of software simulation and converting the weights to resistance values which were subsequently mapped into the memristor array.
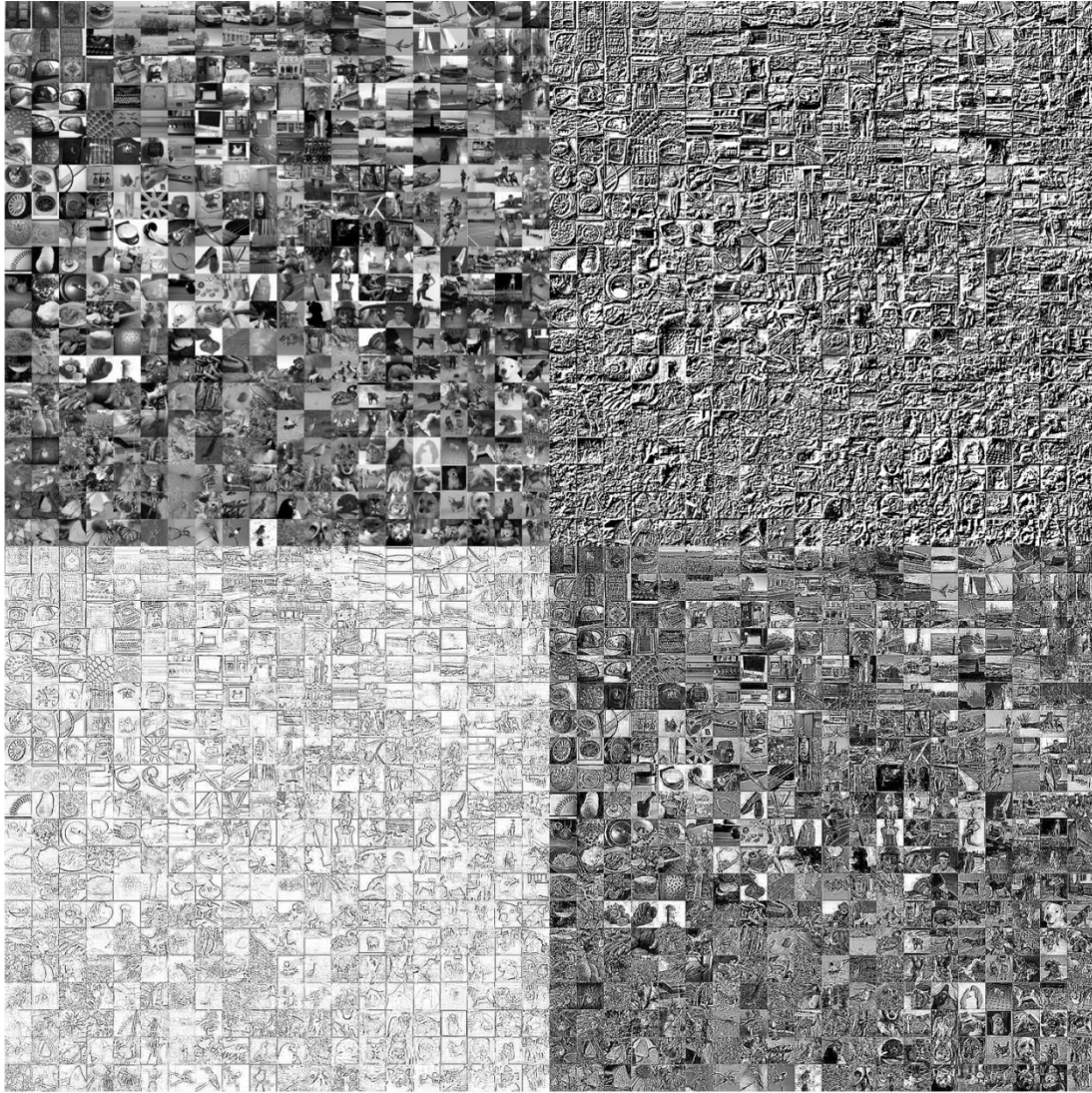
Fig. S17 Raw image (Up-left), embossing (Up-right), outlining (Bottom-left), and sharpening (Bottom-right) of images from classic dataset.

Impact of resistance deviation and MBI NW device variation on image processing performance.

The primary task of the MBI NW Re-RAM is the precise and accurate attainment and transfer of weights. Therefore, there is always a target resistance value R_t which needs to be attained by a kernel or a Re-RAM cell. The observed resistance R_o is often different from the R_t value, triggering a deviation which can be standardized as: **Relative Deviation (RD) = $(R_o - R_t)/R_t$**. The impact of RD on the image processing performance can be visualized in terms of a parameter standardized as **Difference = mean (grayscale values of obtained image due to RD – grayscale values of benchmarked image)/ grayscale values of benchmarked image**. In the simulations a large range of RD spanning from -40% to 1000% was chosen. And the images exhibited in Fig.5a-d of main-text were taken as the benchmarking images with the corresponding difference being taken as 0 for embossing, outlining and sharpening functions.

The simulation curves for embossing, outlining and sharpening have been plotted as (a) in Fig. S18-S20 below, respectively. As evident from the plots, for different image processing techniques, the performance will be affected by different pixels. For example, embossing is mainly affected by kernel pixel 6 and kernel pixel 8, outlining is mainly affected by kernel pixel 7, sharpening is mainly affected by kernel pixel 1, kernel pixel 3, kernel pixel 7, kernel pixel 9 (see Fig. S21 below for kernel diagram). By fixing the RD corresponding to the highest difference value in the plots (a) of Fig. S18-S20, the processed images for the embossing, outlining and sharpening functions have been shown in the red-dash outlined boxes of the respective figures which provides a fair estimate of the amount of distortion possible in the processed images. As it can be noticed, the visual effect does not change too much despite the difference compared with the benchmarked results. Slight changes in visual appearances of processed images are sometimes apparent as in the

case of embossing where the results of kernel pixel 8 with a RD of -0.4 presents high noise in the dark color part of the sundial. This is however attributed to the rough texture of the raw image in that area and the "emboss" kernel makes it more obvious, while it is not proper to say that the emboss effect is severely affected. Also, in Fig. S22a-c below, the entire set of images for embossing, outlining and sharpening, as obtained for varying RD within the entire range of -40% to 1000%, for all the nine pixels, have been provided. The simulation results are sufficient to gauge the maximum amount of possible distortion for the processed images.

Furthermore, experiments of cycle to cycle (10 cycles) and cell to cell variations (10 devices) were carried out to ascertain the experimental RD and its impact on the processed images. Cycle to cycle variations is defined as the variation in low resistance state (LRS) values upon multiple I-V scans from the same pixel. Cell to cell variation is defined as the variation of LRS among different pixels. Plots (b) of Fig. S18-S20 show the RD for cycle to cycle and cell to cell variations for the embossing, outlining and sharpening image processing functions. We used the R_t for benchmarked device: for instance, pixel 8 for embossing, pixel 5 for outlining and pixel 3 for sharpening functions. The cell to cell and cycle to cycle variation induced RDs for the embossing function ranges between -1.7% to 1.6% and -5.8% to 12% respectively. The cell to cell and cycle to cycle variation induced RDs for the outlining function ranges between -2.6% to 1.46% and -7.9% to 8.23% respectively. The cell to cell and cycle to cycle variation induced RDs for the sharpening function ranges between -1.8% to 2.2% and -13.8% to 10.22% respectively. Based on the simulation results, such range of RD will have negligible impact on the visual appearance of the processed images. Also, the maximum magnitude of RD from the respective plots have been extracted and further the processed images corresponding to cell to cell (top image) and cycle to

cycle (bottom image) have been shown in the blue-dash outlined boxes of Fig. S18-S20 for the embossing, outlining and sharpening functions respectively.

Based on the experimental and simulation results, therefore we can safely claim that the variation in our MBI NW devices is within acceptable range for utilization in robust image processing applications.
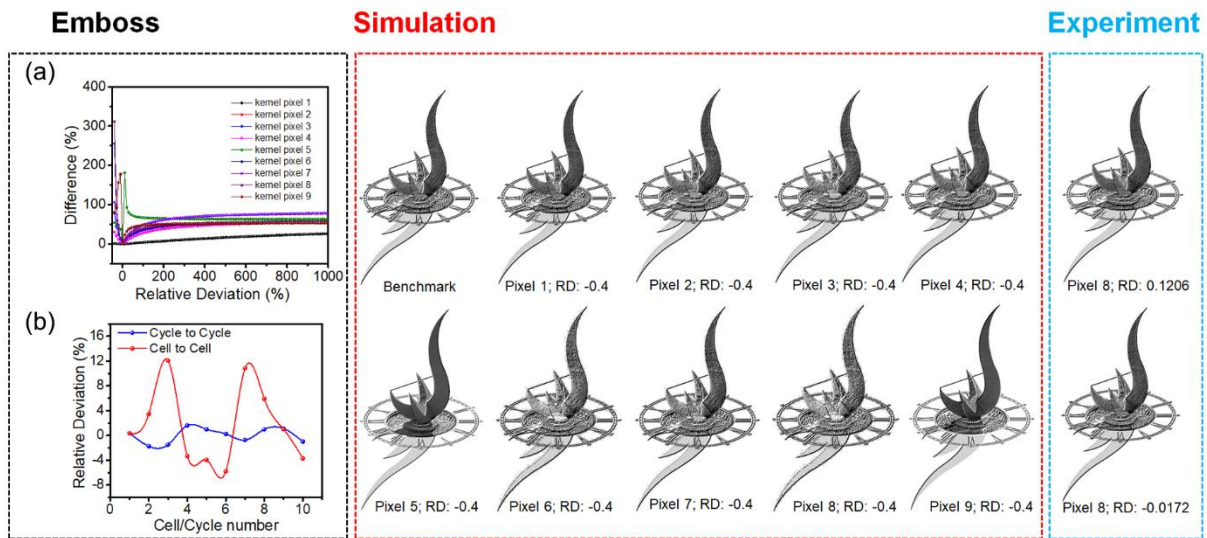
Fig. S18 (a) Difference vs RD plot for embossing function as obtained from simulation. (b) Cell to cell and cycle to cycle variation of RD as obtained from a batch of 10 devices experimentally. Red dashed box: Set of simulated output images corresponding to RD: -0.4 as obtained for all the 9 pixels. Blue dashed box: Top: Processed image corresponding to highest magnitude RD as obtained from cell to cell variation in (b). Bottom: Processed image corresponding to highest magnitude RD as obtained from cycle to cycle variation in (b).
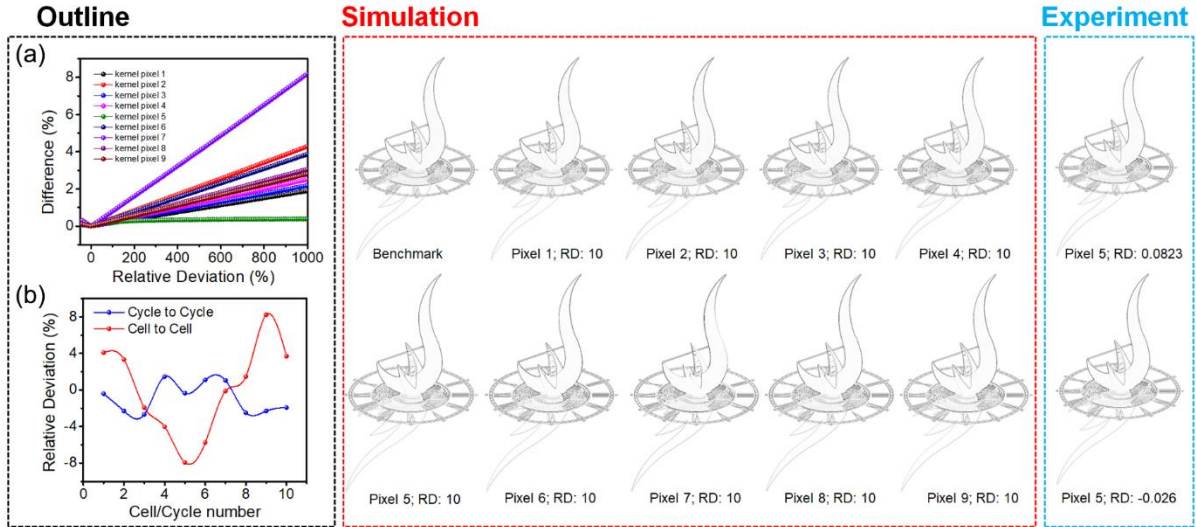
Fig. S19 (a) Difference vs RD plot for outlining function as obtained from simulation. (b) Cell to cell and cycle to cycle variation of RD as obtained from a batch of 10 devices experimentally. Red dashed box: Set of simulated output images corresponding to RD: 10 as obtained for all the 9 pixels. Blue dashed box: Top: Processed image corresponding to highest magnitude RD as obtained from cell to cell variation in (b). Bottom: Processed image corresponding to highest magnitude RD as obtained from cycle to cycle variation in (b).
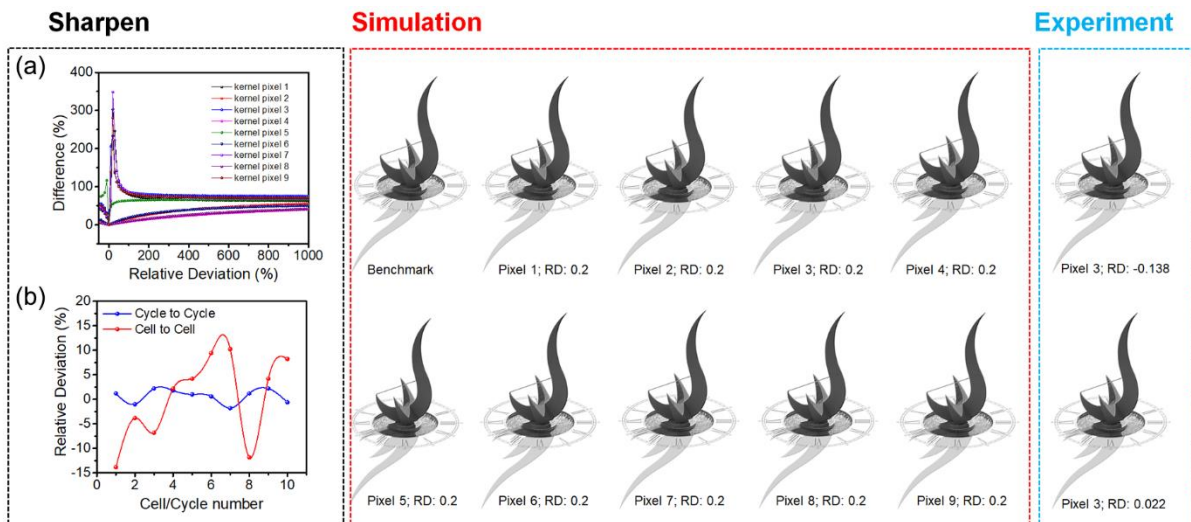
Fig. S20 (a) Difference vs RD plot for sharpening function as obtained from simulation. (b) Cell to cell and cycle to cycle variation of RD as obtained from a batch of 10 devices experimentally. Red dashed box: Set of simulated output images corresponding to RD: 0.2 as obtained for all the 9 pixels. Blue dashed box: Top: Processed image corresponding to highest magnitude RD as obtained from cell to cell variation in (b). Bottom: Processed image corresponding to highest magnitude RD as obtained from cycle to cycle variation in (b).

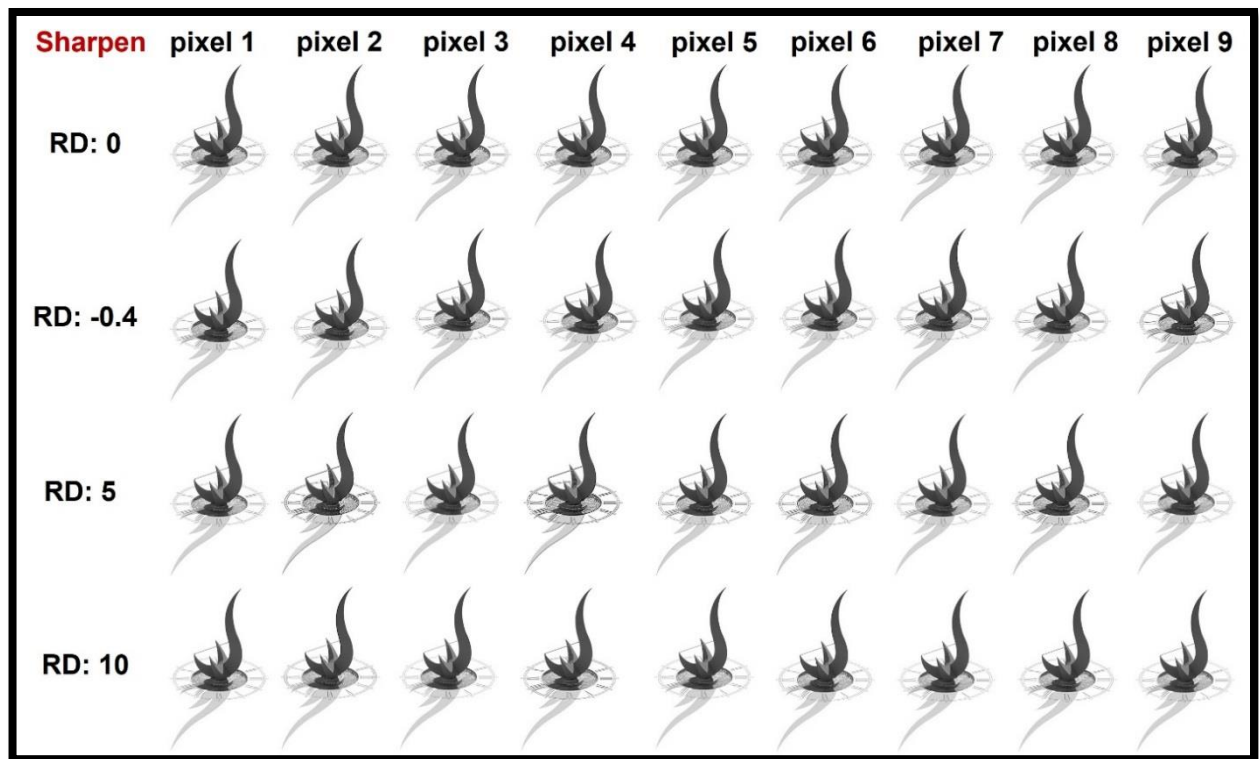| Pixel 1	Pixel 2	Pixel 3
Pixel 4	Pixel 5	Pixel 6
Pixel 7	Pixel 8	Pixel 9

Fig. S21 Schematic illustrating the order of kernel pixels formed by the MBI NW Re-RAM
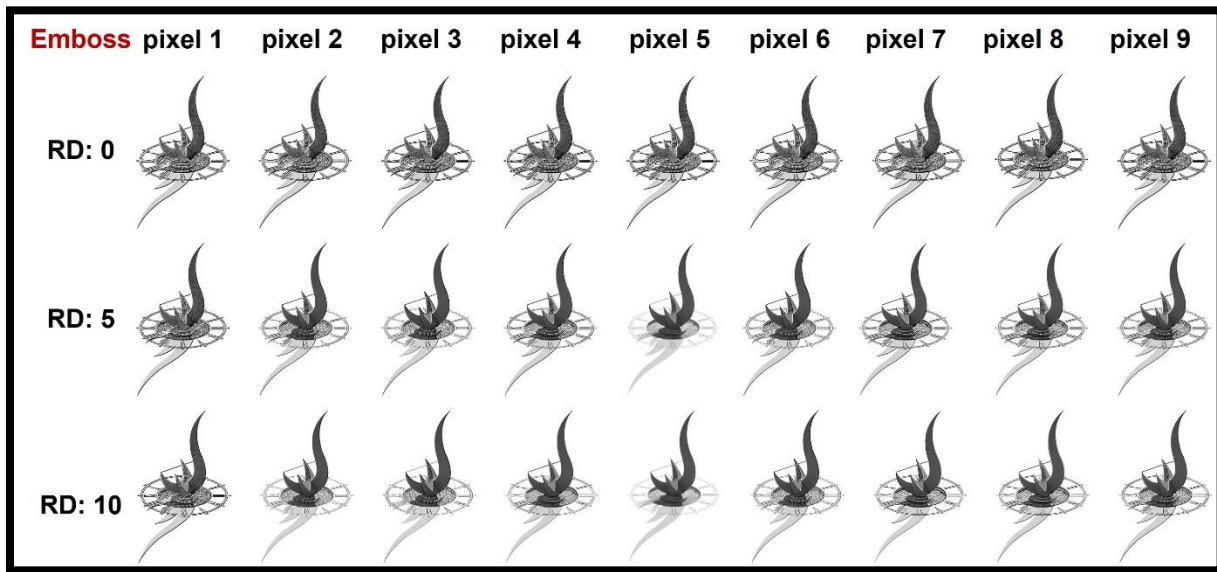
Fig. S22 (a) Embossed images for varying RD.
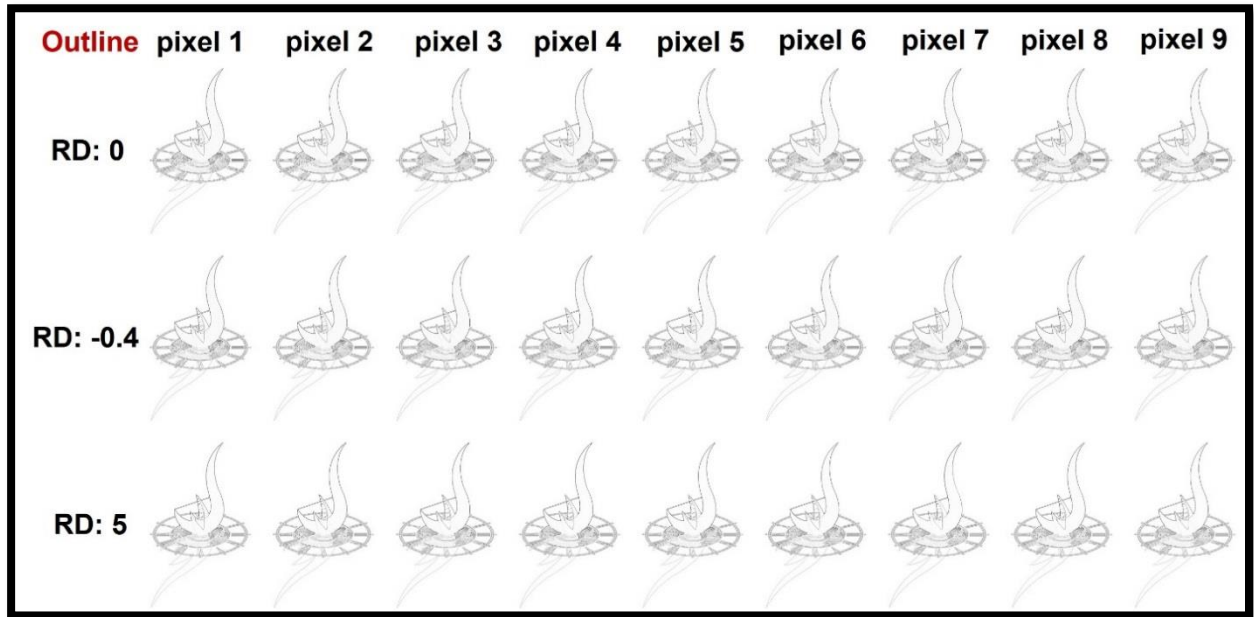
Fig. S22 (b) Outlined images for varying RD.

Fig. S22 (c) Sharpened images for varying RD.