Electronic Supplementary Material (ESI) for Nanoscale Horizons.


*Supporting Information*

# *Hardware Trojans based on Two-dimensional Memtransistor*

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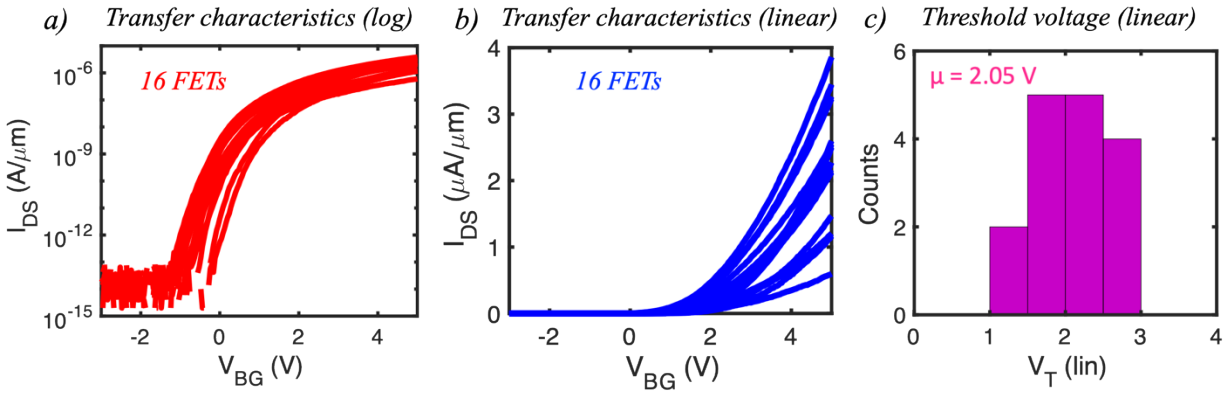
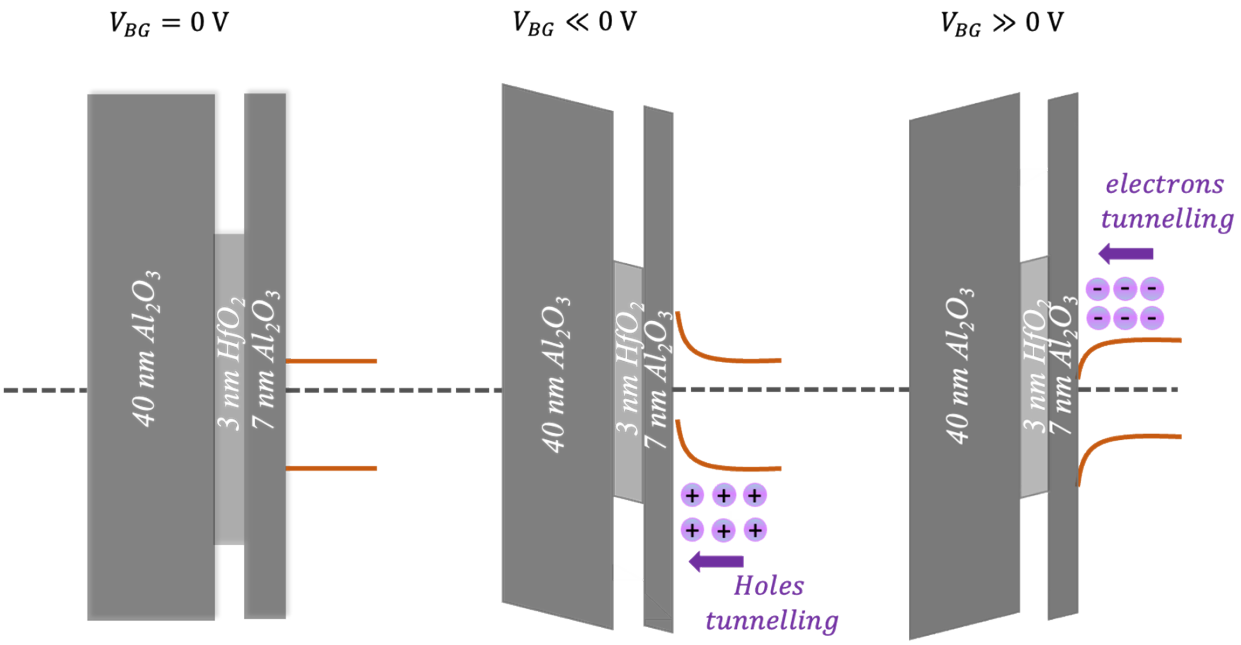
**Supporting Information S1**



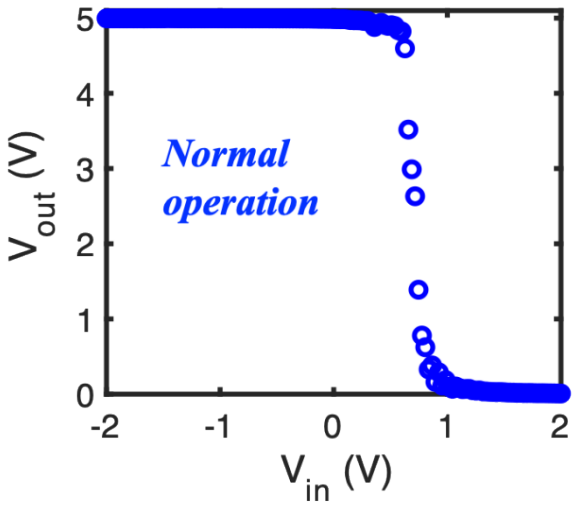

***Supporting Figure S1:*** *Evaluating device-to-device variation across a population of 16 $MoS_2$-based FETs by measuring the transfer characteristics in a) logarithmic scale and b) linear scale. The devices consistently show good $I_{ON}$ values with $I_{ON}/I_{OFF}$ ratios of about $10^7$. c) A histogram plot of the threshold voltage $(V_{TH})$ extracted from the linear scale once again prove the high quality of MOCVD grown $MoS_2$.*

**Supporting Information S2**



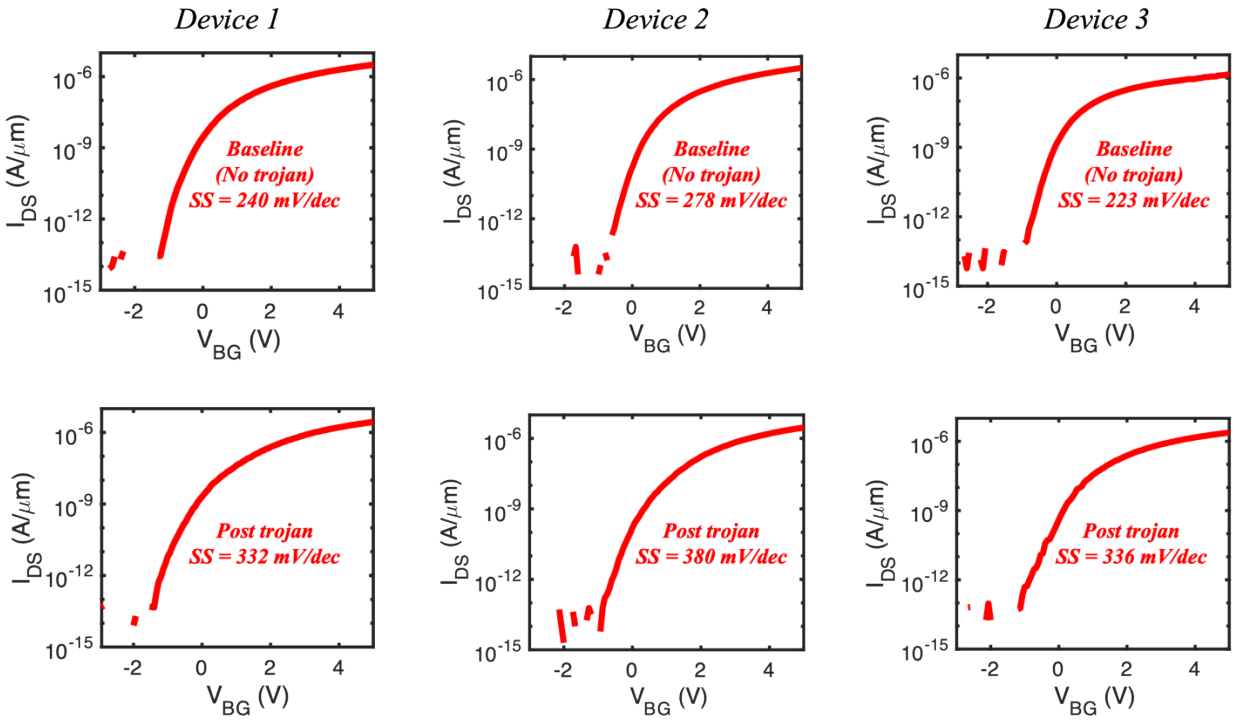

***Supporting Figure S2:*** *Band diagram profile of our 2D memtransistor architecture showing a 40 nm alumina ($Al_2O_3$) as the gate dielectric, a 3 nm hafnia ($HfO_2$) as a charge trapping layer in a floating gate (FG) configuration, and a 7 nm $Al_2O_3$ as the tunnelling layer under three different gate bias ($V_{BG}$) conditions. A large negative $V_{BG}$ facilitates tunnelling of holes through the tunnelling layer into the FG whereas a large positive $V_{BG}$ facilitates the tunnelling of electrons into the FG. These carriers remain trapped in the FG thereby causing a negative and a positive shift in the $V_{TH}$, respectively, by screening the electric field. The subsequent accumulation of these carriers is enabled by the Fowler Nordheim tunnelling*

**Supporting Information S3**



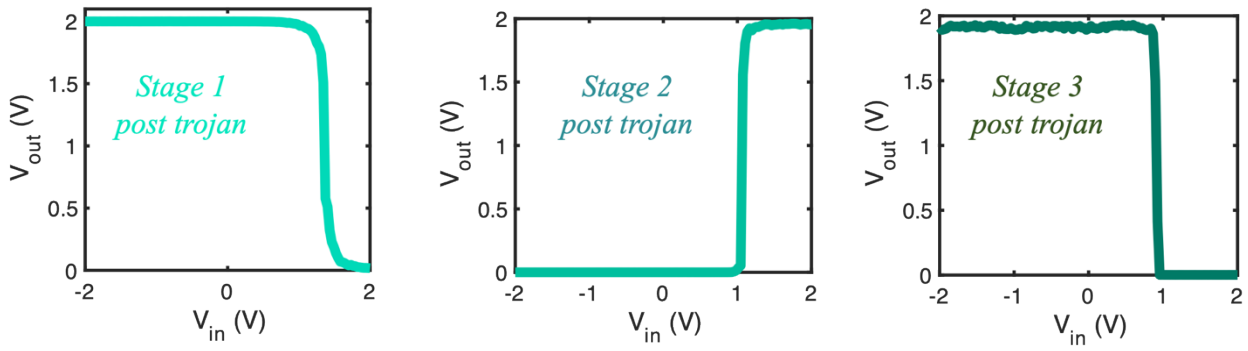

***Supporting Figure S3****: Inverter output characteristics for a supply voltage* $V_{DD} = 5V$. *The inverter shows normal characteristics at higher supply voltage in spite of the presence of a HT at lower* $V_{DD} = 2V$.

**Supporting Information S4**



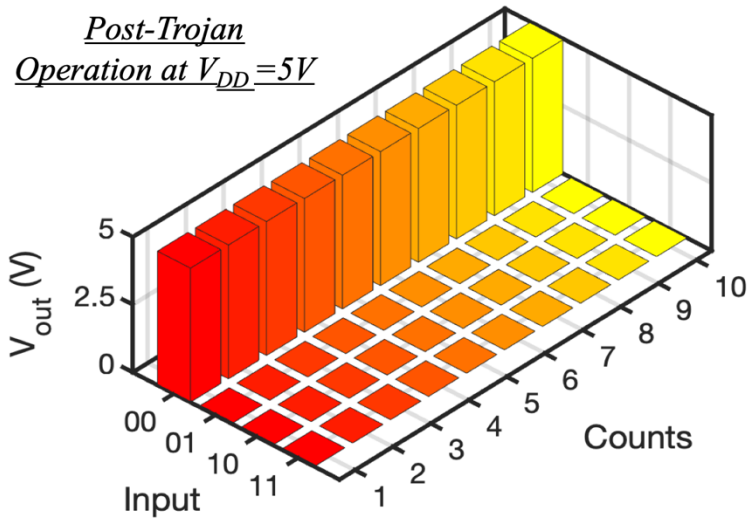

***Supporting Figure S4:*** *Evolution of degradation observed in the subthreshold slope (SS) of a 2D memtransistor in a cascaded three-stage inverter (TSI) circuit module as a form of HT for three different individual $MoS_2$ memtransistors post application of a $V_{HRT}$ of 15V followed by a $V_{LRT}$ of -15V to the local gates.*

**Supporting Information S5**



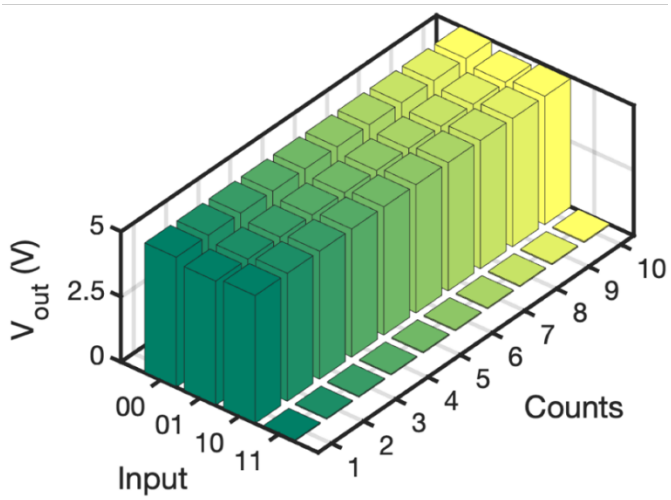

***Supporting Figure S5:*** *The corresponding output inverter plots post* $V_{HRT}$ *application of 15 V to one of the local gates* $MT2$ *from stage 1. A clear shift in the switching voltage* $V_m$ *is observed for all the stages.*

**Supporting Information S6**



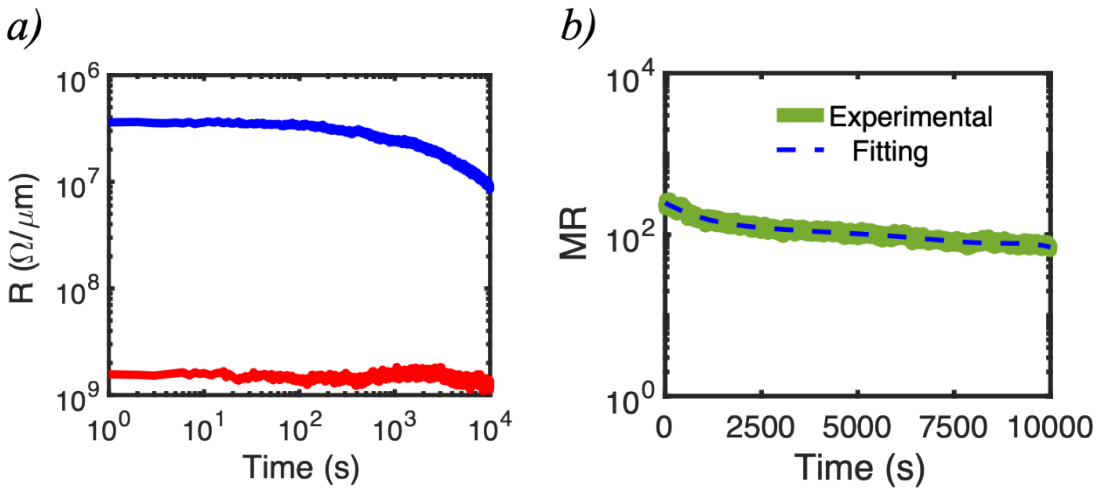

***Supporting Figure S6:*** *Normal* $NOR$ *functionality observed for a* $V_{DD} = 5V$ *despite the presence of HT at the rare node (*$V_{DD} = 2V$*).*

**Supporting Information S7**




***Supporting Figure S7:*** *Normal* $NAND$ *functionality observed for a* $V_{DD} = 5V$ *despite the presence of HT at the rare node (*$V_{DD} = 2V$*).*

**Supporting Information S8**




***Supporting Figure S8:*** *a) A 2D plot for long term retention of two representative analog resistance states for an extended period of time approximately $10^4$ seconds or roughly 3 hours. b) A plot of memory ratio (MR) between the two states with time. MR varied from 3 x $10^2$ to 1 x $10^2$ with an exponential decay time constant $\tau_{decay}$ of 7x $10^3$ seconds. The fit was carried out using the following equation:* $G(t) = G_F\left(\frac{t}{\tau}\right)^{-\gamma}$, *where* $\tau = 7 \times 10^3 s$ *is the decay constant, G(t) is the MR value at* $10^4 s$ *and* $G_F$ *is the MR value at* $10^0 s$. *The total time extracted before the two states converge using these fitting parameters was estimated to be ~*