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Supplementary Materials for

Laminated three-dimensional carbon nanotube integrated circuits

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#These authors were equal major contributors to this work.

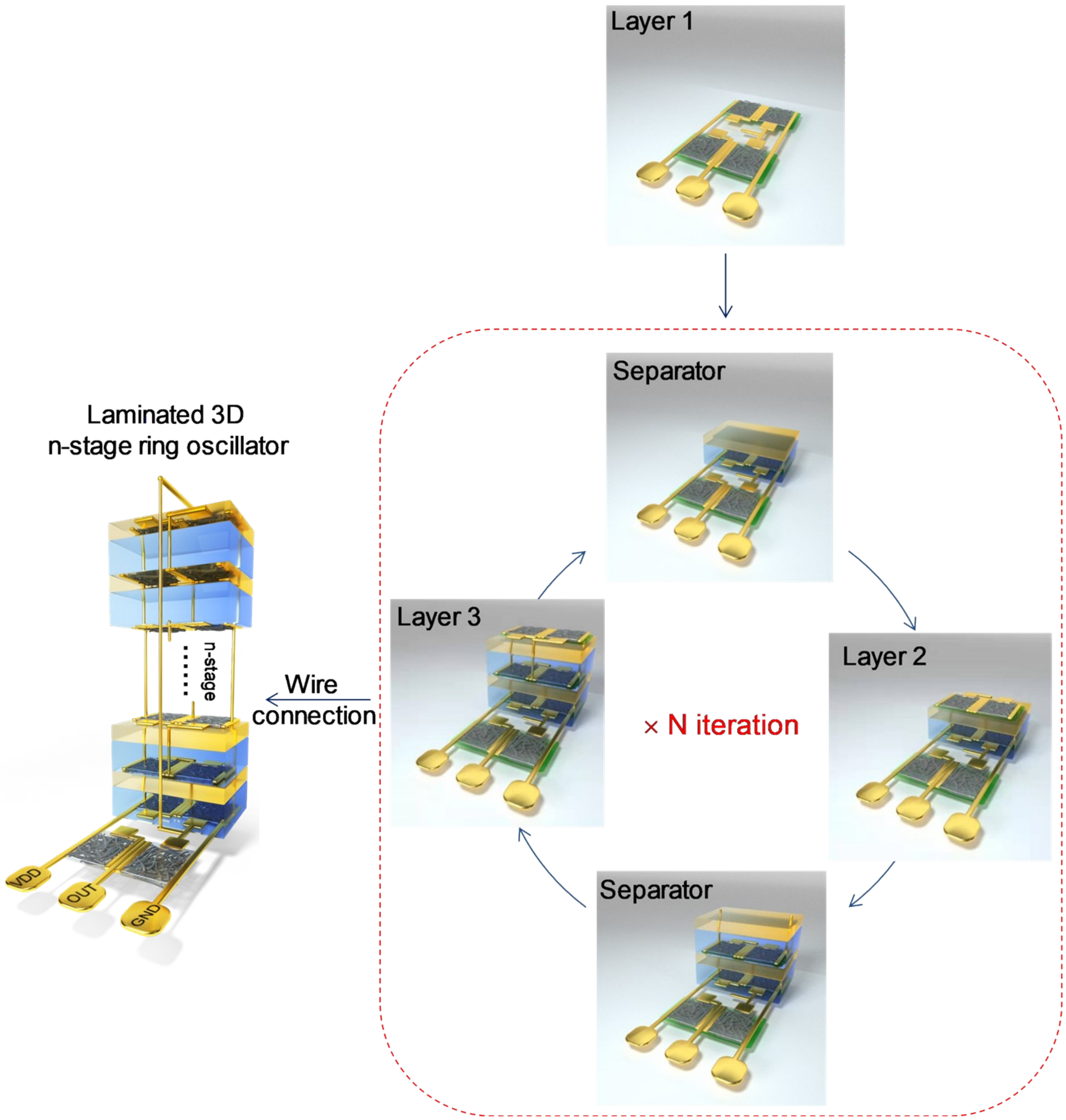

Figure S1. Device fabrication procedure. Schematic of fabricating the laminated 3D n-stage ring oscillators. The fabrication of the buffer and the first component, an inverters, was completed on a silicon substrate by standard photolithography, metallization and lift-off processes. CNT thin films were used as the channel materials followed by PTFE/Al_2O_3 encapsulation. The fabrication of the other layers replicated the first layer until n layers were completed and the whole unit was finally connected to the buffer inverter with wires.

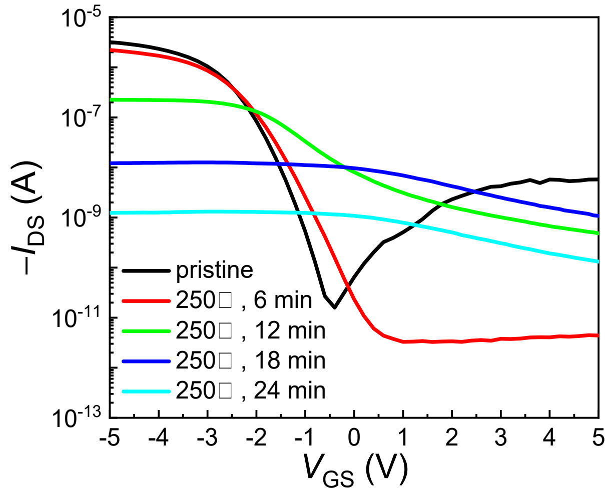

Figure S2. Influence of photoresist encapsulation. Typical transfer characteristics of CNT TFTs after repeated heating treatments.

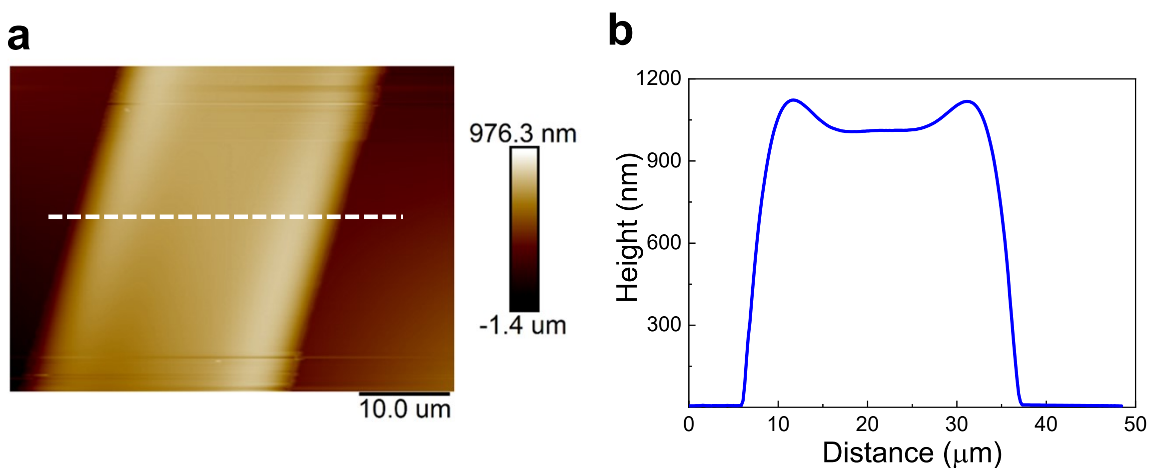

Figure S3. (a) Atomic force microscopy (AFM) image of the morphology of the photoresist film after heat treatment and (b) the height distribution of the dashed line region.

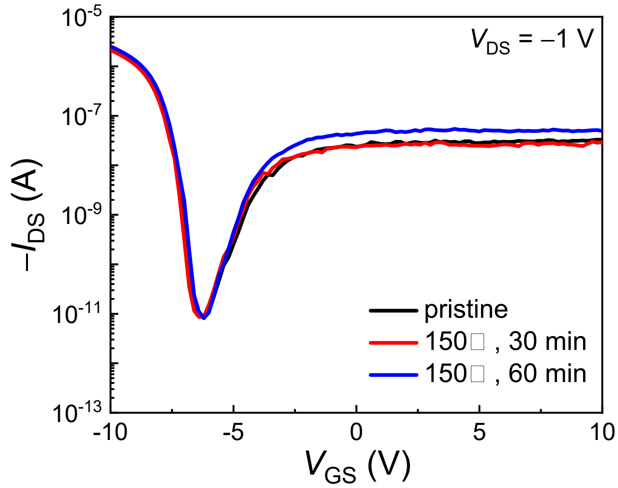

Figure S4. Testing separator materials for laminated 3D devices. Typical transfer characteristics of CNT TFTs after PTFE encapsulation treated at 150 ℃ for various times.

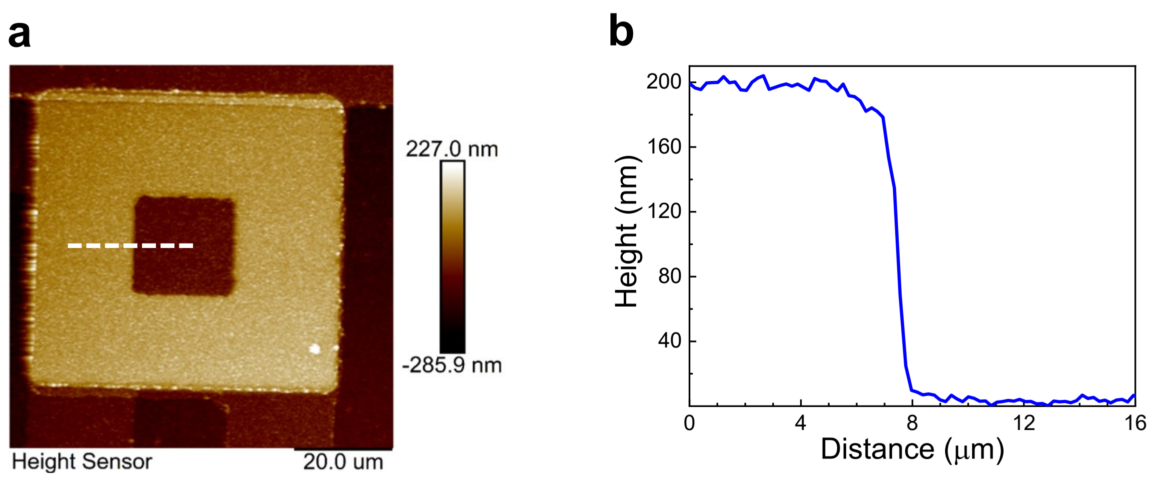

Figure S5. (a) AFM image of the morphology of PTFE/Al_2O_3 separator after heating and (b) height distribution along the dashed line region.

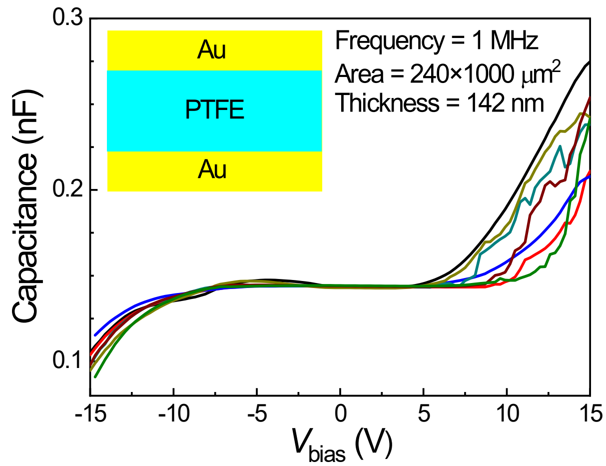

Figure S6. Capacitance-voltage measurement of the PTFE layer. The dielectric constant of the PTFE layer is calculated using the equation $C = \varepsilon\varepsilon_0 S/d$, where C is the capacitance of the PTFE layer (~0.26 nF), ε and d are the relative dielectric constant and thickness of the PTFE layer (~142 nm), ε_0 is the dielectric constant in a vacuum, and S is the area of the electrodes.

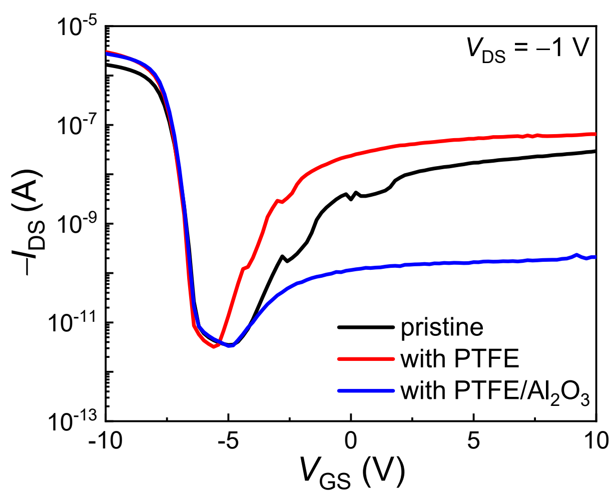

Figure S7. Typical transfer characteristics of one CNT TFT after sequential PTFE, PTFE/Al_2O_3 encapsulation at V_{DS} of −1 V. The PTFE was treated at 150 °C for 60 min.

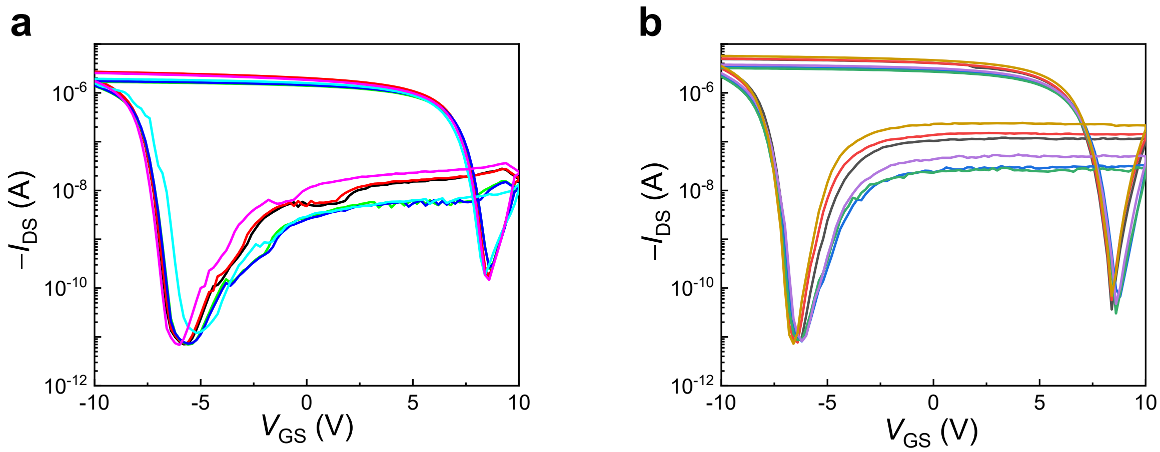

Figure S8. Influence of PTFE/Al_2O_3 encapsulation on the electrical performance. Transfer characteristics of CNT TFTs (a) without and (b) with PTFE/Al_2O_3 encapsulation.

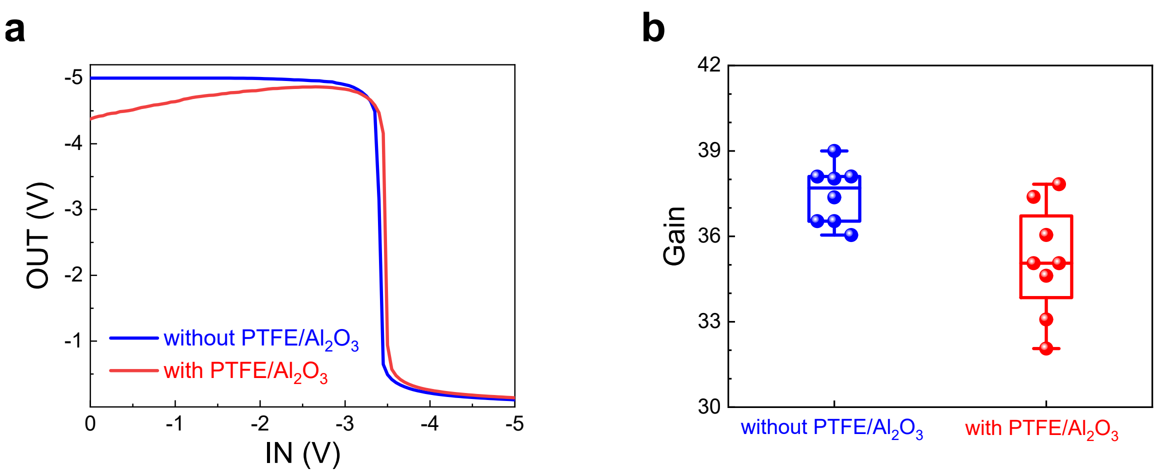

Figure S9. Influence of PTFE/Al_2O_3 encapsulation on the electrical performance. (a) Input-output characteristics of a PMOS inverter without/with PTFE/Al_2O_3 encapsulation. (b) Gain distribution of 8 PMOS inverters without/with PTFE/Al_2O_3 encapsulation remains almost constant.

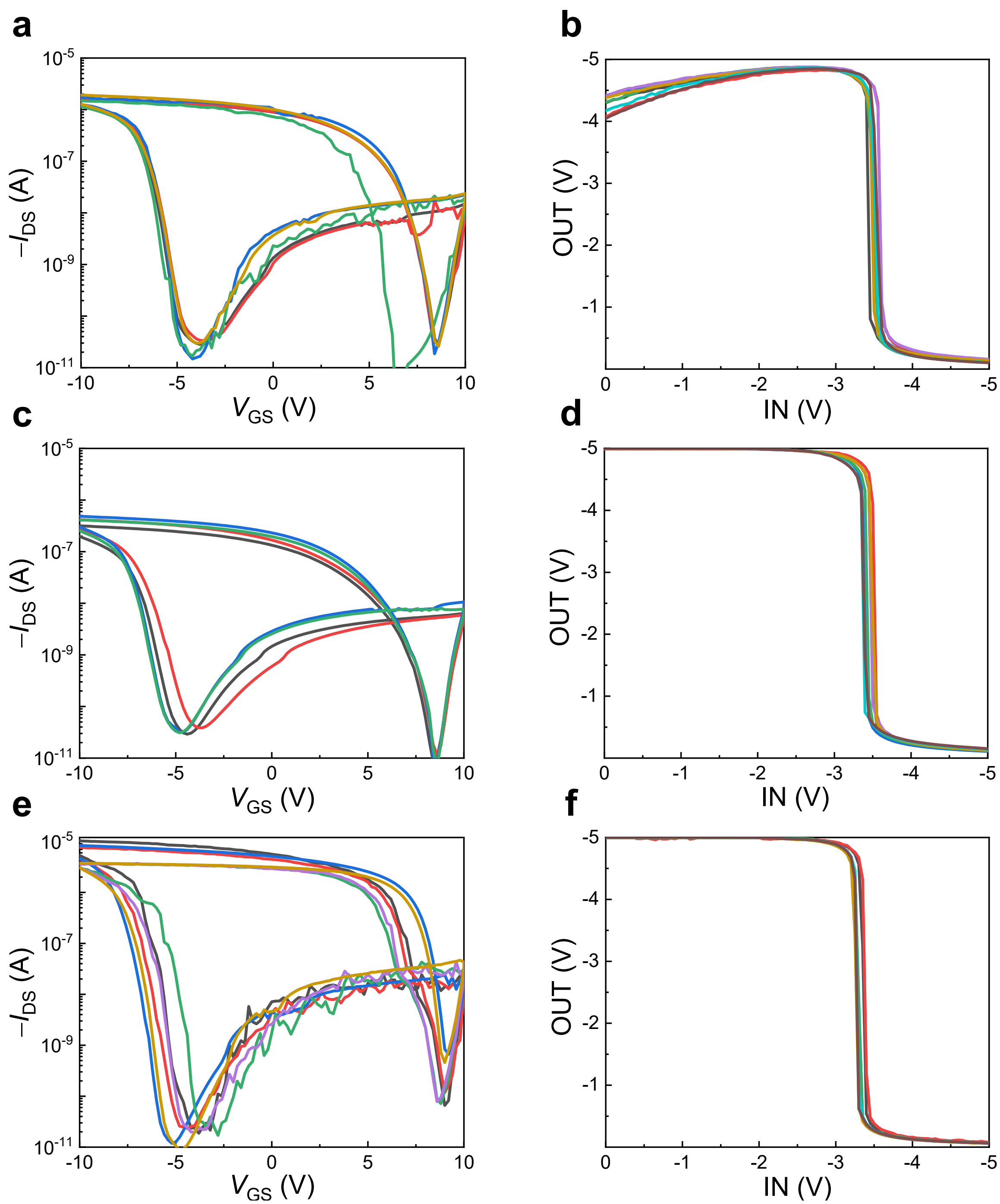

Figure S10. Electrical performance of CNT TFTs and inverters on each layer within the 3D structure. Transfer and input-output characteristics of CNT TFTs and inverters on the (a-b) first, (c-d) second and (e-f) third layers.

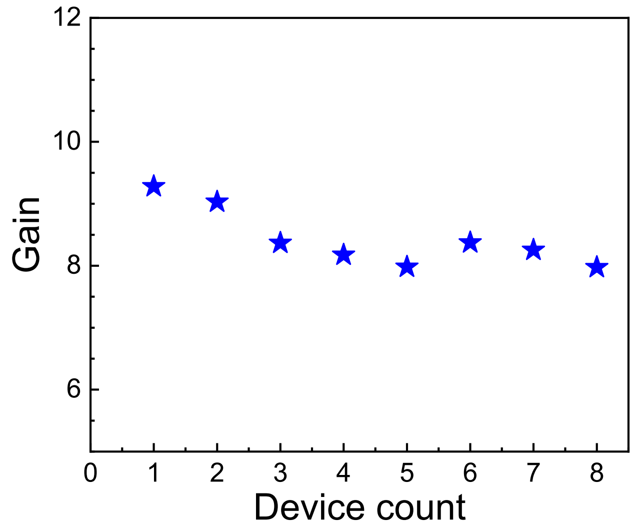

Figure S11. Statistical gain distribution of 8 laminated 3D inverters at V_{DD} = −5 V indicating the good uniformity.

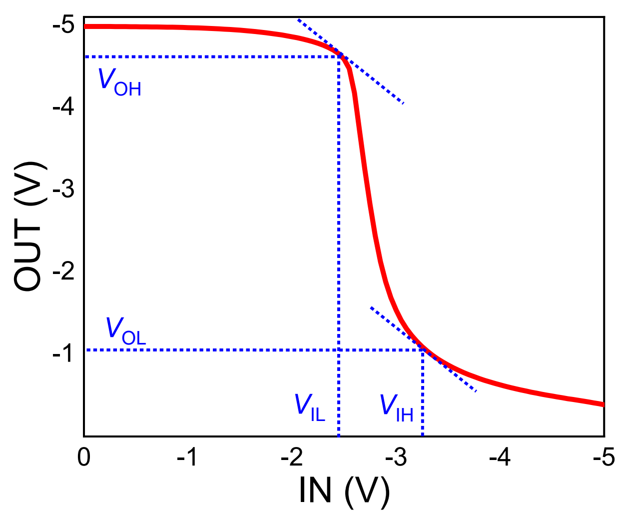

Figure S12. Calculation of noise margin. Definition of V_{OH}, V_{OL}, V_{IH} and V_{IL} based on the transfer characteristics of an inverter, where V_{OH}, V_{OL}, V_{IH} and V_{IL} corresponding the largest output voltage, smallest output voltage, highest input voltage and smallest input voltage where slope = −1, respectively.

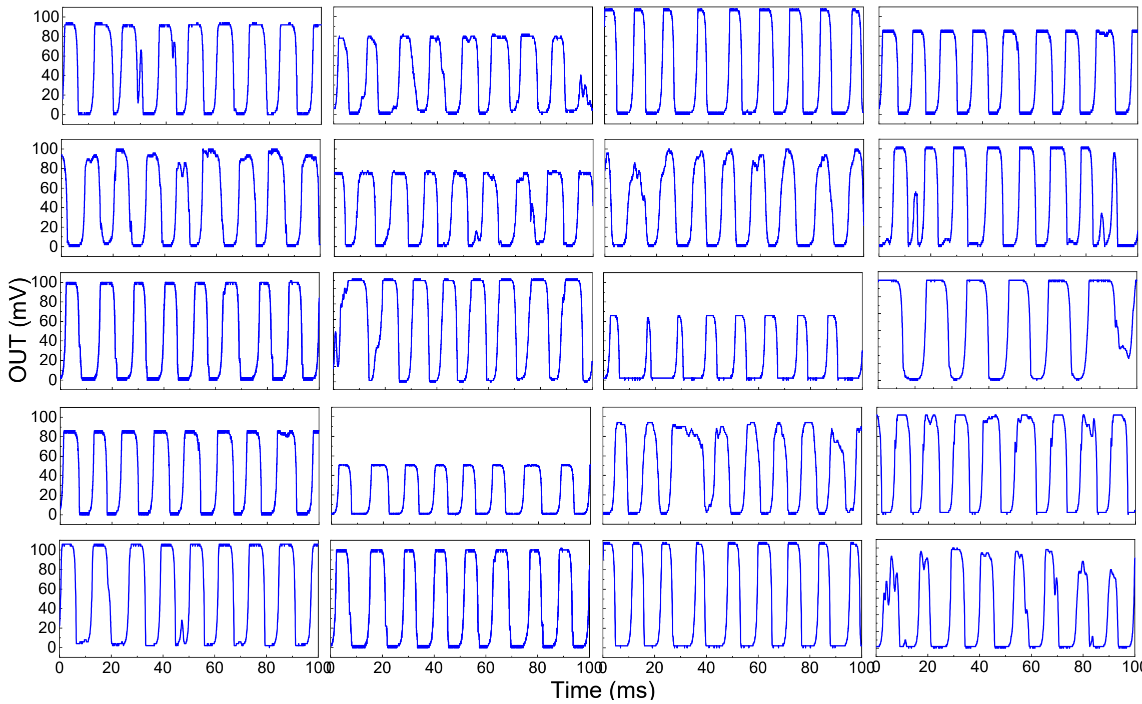

Figure S13. Laminated 3D CNT ring oscillators array. The output characteristics of a laminated 3D ring oscillator array at $V_{DD} = -10$ V.

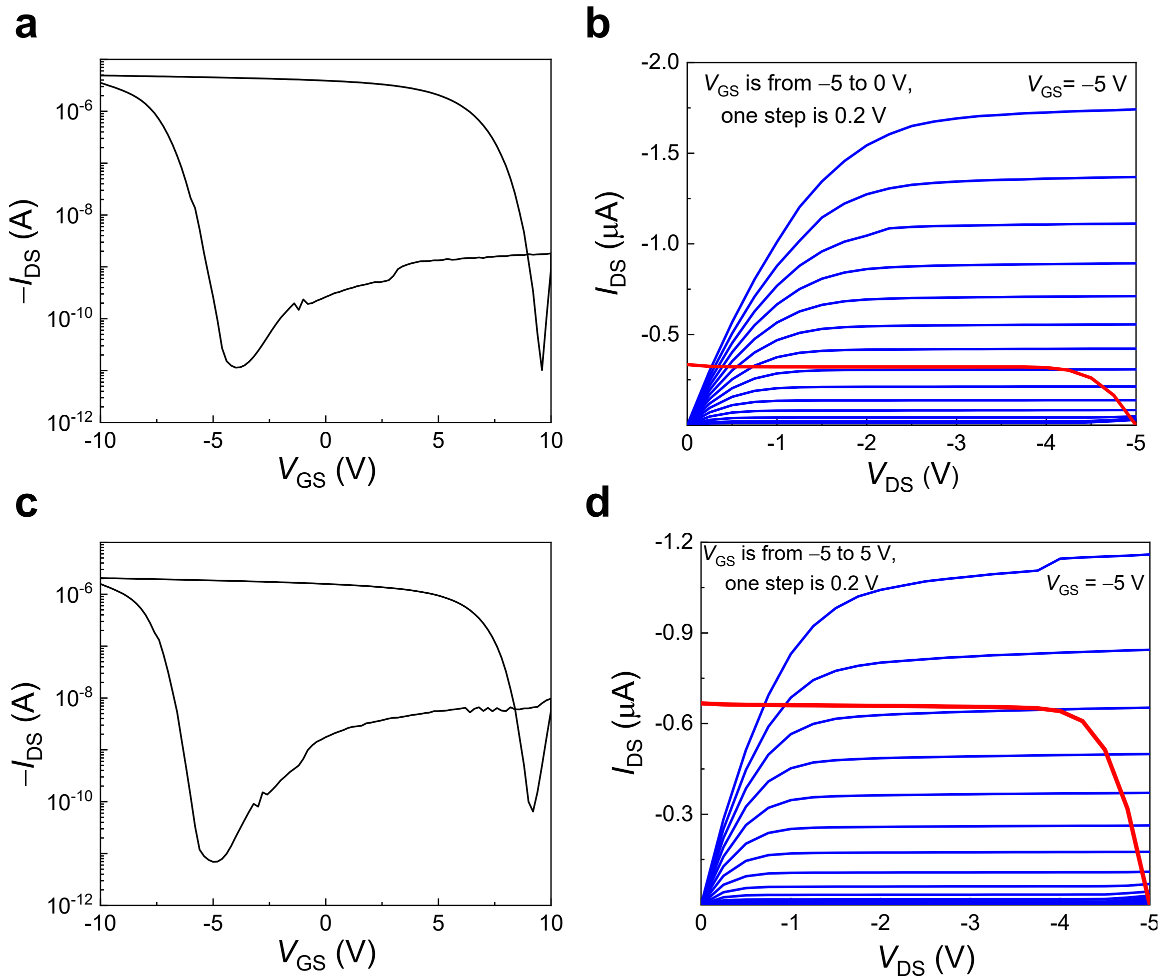

Figure S14. Analyzing the functional operation of the ring oscillator. Typical transfer and output characteristics of a drive TFT and a load TFT with PTFE/Al_2O_3 encapsulation (a, b) once and (c, d) twice.