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Electronic Supporting Information

Bias-Dependent Hole Transport through Multi-Channel Silicon Nanowire Transistor with Single-Acceptor-Induced Quantum Dots

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Section 1. Device fabrication

The p-type multi-channel silicon JNT devices investigated in this work were fabricated on a boron-doped (10^{15} cm^{-3}) (110)-oriented SOI wafer with 88-nm-thick top silicon and 145-nm-thick buried oxide. Device fabrication began with electron-beam lithography (EBL) and inductively coupled plasma (ICP) etching, which were performed to define the source/drain region and the nanowire-array channels along the <110> direction, followed by sacrificial oxidation to eliminate the etching induced damage. Under etching occurred in the buried oxide during the subsequent sacrificial oxide removal in the buffered hydrofluoric solution, suspending the silicon nanowires. Then, a 25-nm-thick SiO_2 layer was formed by thermal oxidation at 900 °C in dry oxygen. Next, a 200-nm-thick heavily boron-doped (10^{19} cm^{-3}) polysilicon (poly-Si) layer was deposited by in-situ doping low-pressure chemical vapor deposition (LPCVD). Then, the polysilicon gate was defined by EBL and ICP etching, followed by a poly-Si re-oxidation process to repair the gate oxide integrity and grow an oxide layer at the surface of the poly-Si gate. Next, gate spacers were formed after depositing a 200-nm-thick SiO_2 layer by plasma-enhanced chemical vapor deposition (PECVD) and etching by ICP.

Source/drain doping was carried out by self-aligned BF_2^+ implantation with an energy of 33 keV and a dose of 3×13 cm^{-2}, followed by rapid thermal annealing (RTA) at 1050 °C for 10 seconds under 1 bar nitrogen atmosphere. After depositing a 200-nm-thick SiO_2 layer by PECVD as the protective layer, contact holes were opened using optical lithography and ICP etching. Following 25-nm-thick nickel film evaporation, the nickel-silicide ohm contact layer was formed by RTA at

500 °C for 1 minute under 1 bar nitrogen atmosphere. The unreacted nickel was removed by piranha solutions without attacking the silicide. To form the source/drain and gate electrode pads, optical lithography was executed to define the pattern in the photoresist, and then 400-nm-thick aluminum was evaporated and lifted off. The device fabrication process was finished with RTA at 400 °C for one minute under 1 bar nitrogen atmosphere. The p-type JNT devices were enclosed in the vacuum chamber of a CRX-4K cryogenic probe station whose temperature can be cooled down to 6 K, and measured by an Agilent B1500 semiconductor parameter analyzer. Analogous current oscillations can be observed in all single- and multi-channel JNT devices fabricated on the same wafer.

Section 2. Simulation of boron atom distributions using Silvaco ATHENA TCAD tools

The simulation and modeling of boron atom distributions were simulated using the commercial Silvaco ATHENA TCAD tools.

The as-deposited two-dimensional (2D) structure consists of a 150-nm-thick boron-doped (10^{15} cm^{-3}) (110)-oriented Si channel, a 25-nm-thick SiO_2 dielectric layer, a 200-nm-thick and 180-nm-wide boron-doped (10^{19} cm^{-3}) poly-Si, and two 200-nm-thick SiO_2 spacers.

The boron-ion (BF_2^+) implantation was simulated using the binary collision approximation (BCA) Monte Carlo ion implant model at an implant energy of 33 keV and an area dose of 3×13 cm^{-2}.

The annealing process includes three RTA steps, 1050 °C for 10 seconds under 1 bar nitrogen atmosphere, 500 °C for 1 minute under 1 bar nitrogen atmosphere, and 400 °C for one minute under 1 bar nitrogen atmosphere.

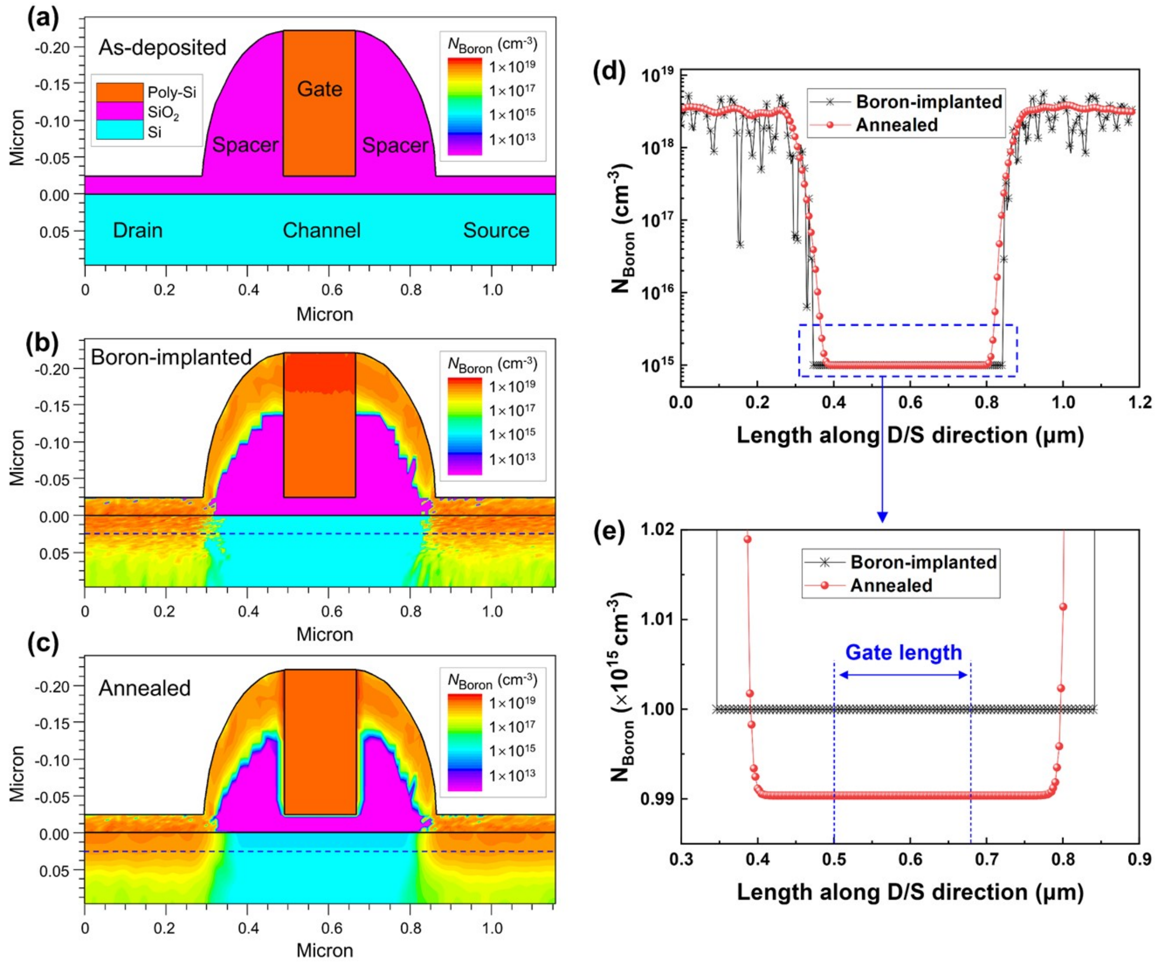

Fig. S1 The simulation results of the boron atom concentration N_{Boron} distributions. The 2D profiles of N_{Boron} distributions in the nanowire and gate directions at different process states: (a) As-deposited; (b) Boron-ion implanted; and (c) Annealed. (d) The boron-implanted and annealed N_{Boron} distributions of the 25-nm-depth Si layer along the nanowire direction extracted along the dashed lines in Fig. S2b and c. (e) The local magnification of the region between the two spacers in Fig. S1d. Because of the spacers, the boron-ion implant and annealing have basically no influence on the N_{Boron} of the Si underneath the gate region, which is a constant that only slightly decreases (~1%) after annealing.

Section 3. Arrhenius activation energy

Fig. S2 shows the temperature-dependent $I_{DS} - V_{GS}$ characteristics for Dev. 13Ch with the temperature ranging from 6 K to 300 K. Clear oscillations can be seen in the I_{DS} curves at low temperatures (< 75 K), attributed to holes transporting via dopant-induced QDs (in the black dotted line frame) and 1D confinement-induced discrete energy subbands (in the red dotted line frame).[1] The oscillations indicated by the black arrows diminish as the temperature rises and disappear above 100 K, attributed to the thermal broadening of the conductance.[2]

Fig. S2b plots the conductance G extracted from Fig. S2a in logarithmic form as a function of T^{-1}. The temperature-dependent G follows the Arrhenius model[3]

$$G = G_0 \exp(-E_a / k_B T) \quad \text{* MERGEFORMAT (1)}$$

where k_B is Boltzmann's constant and E_a represents the activation energy, which equals the energy barrier E_b for carriers transporting from the source to the drain. Then, E_b could be obtained from the slope of the linear region (100 ~ 300 K).

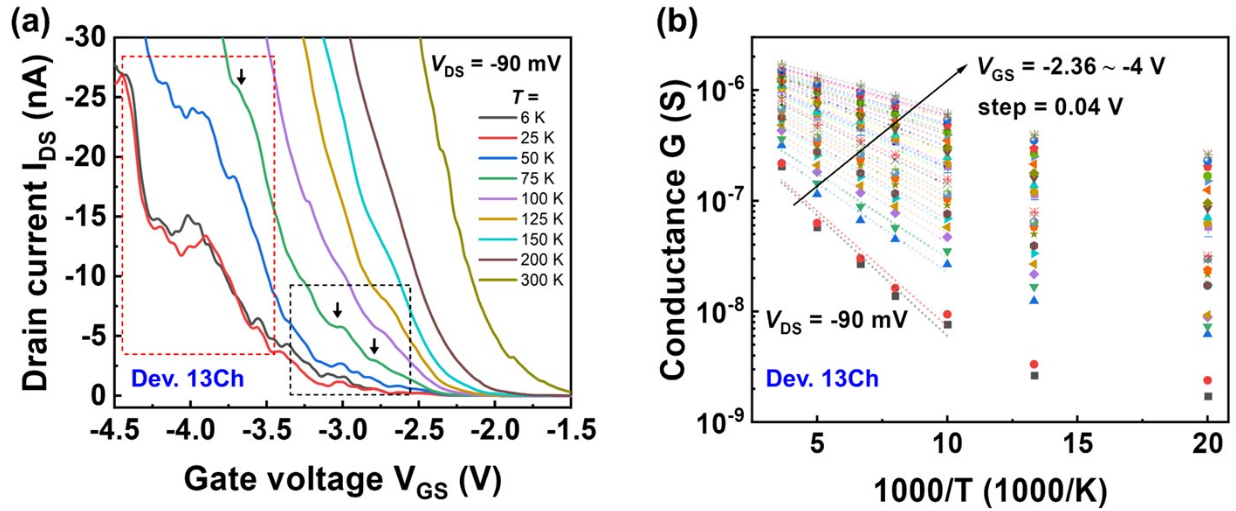

Fig. S2 (a) Temperature-dependent $I_{DS} - V_{GS}$ characteristics at V_{DS} = -90 mV for Dev. 13Ch. With the temperature increasing from 6 K to 300 K, the oscillations gradually vanish owing to the thermal smearing of the conductance. Arrows: quantum oscillations. Black dotted line frame: 0D transport. Red dotted line frame: 1D transport. (b) Arrhenius plots of the conductance at V_{DS} = -90 mV. The energy barrier was extracted by fitting the linear region (100 ~ 300 K).

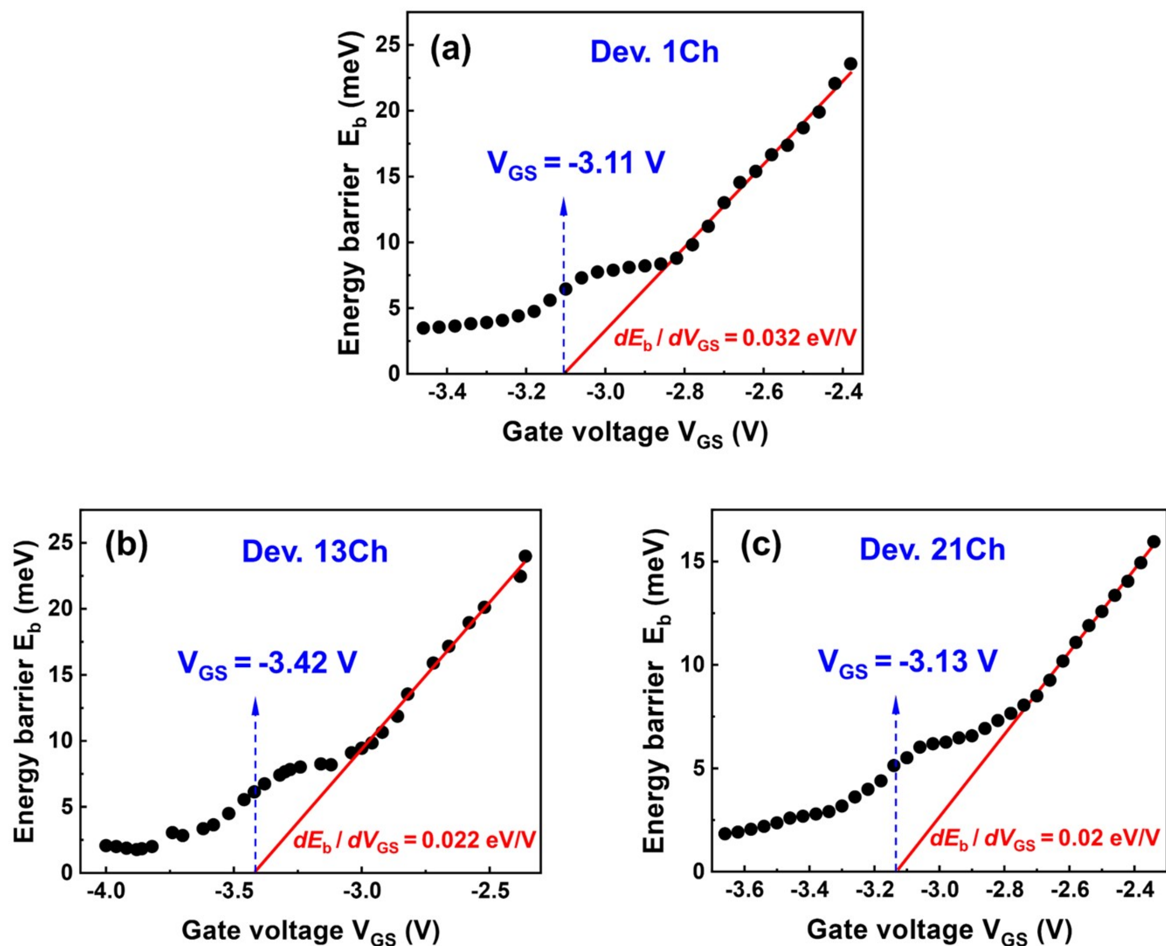

Fig. S3 (a-c) E_b versus V_{GS} characteristics of Dev. 1Ch, 13Ch, and 21Ch. The linear extrapolations give the threshold voltage of -3.11 V, -3.42 V, and -3.13 V for Dev. 1Ch, 13Ch, and 21Ch, respectively.

Section 4. The V_{GS} shift of the splitting spikes for A⁺ state

Fig. S4 shows the V_{GS} shift of the splitting spikes for the A^+ state extracted from Fig. 4a. According to the relation $\Delta V_{GS}^{R} + \Delta V_{GS}^{L} = \beta V_{DS} / \gamma$, the value of β was estimated to be 0.01 for the A^+ state, which is smaller than that for the A^0 state (0.012). As the V_{GS} increases negatively, the conducting nanowire channel under the gate is broadened, thus decreasing its resistance. Consequently, the ratio of the effective bias (V_{DS}^{eff}) to the applied bias (V_{DS}) is lowered. Using the estimated β, the γ of the A^+ state for dopant-a, -b, and -c were obtained to be 0.25, 0.37 and 0.31, respectively. Meanwhile, the values of 1-γ were obtained as 0.78, 0.67 and 0.72 for dopant-a, -b, and –c, respectively, according to the ΔV_{GS}^{L}-V_{DS} curves.

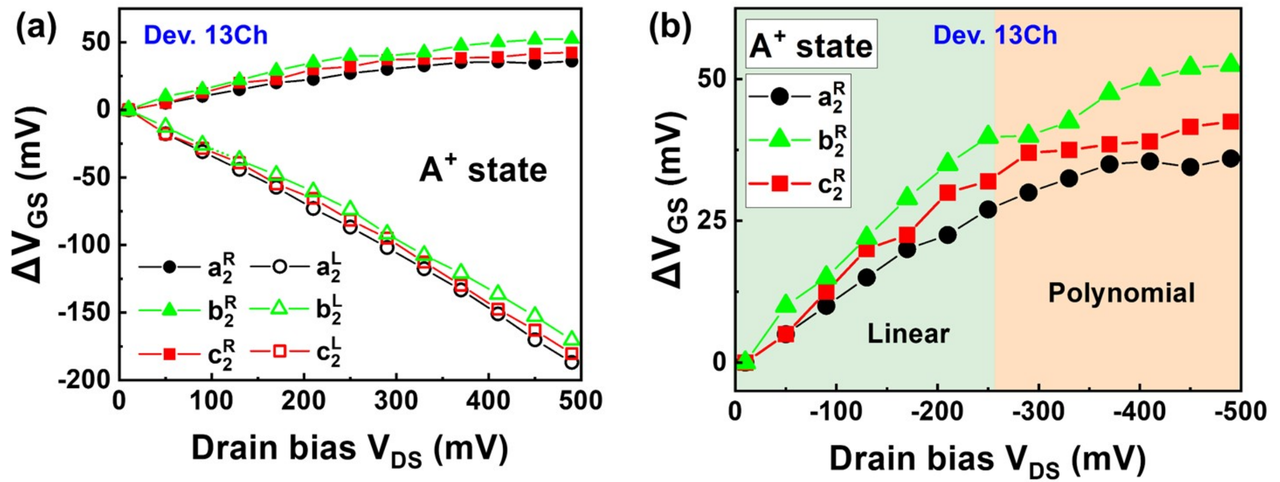

Fig. S4 (a) The relative V_{GS} shift of the splitting spikes for the A^+ state extracted from Fig. 4a. (b) The relative V_{GS} shift of the right splitting spikes for the A^+ state.

Section 5. The conductance of single hole resonant tunneling in a double-barrier system

In a double-barrier system, the amplitude of the conductance spike for single hole resonant tunneling is given by[4]

$$G = \frac{e^2}{h}\frac{4\Gamma_S\Gamma_D}{\left(\Gamma_S + \Gamma_D\right)^2} \qquad \text{* MERGEFORMAT (2)}$$

where $\Gamma_{S,D} = u_0 e^{-2r_{S,D}/\lambda}$ is the leak rate of a hole from the dopant to the source (drain) contact, u_0 the height of the barrier, λ the hole localization length, and $r_{S,D}$ the distance between the dopant to the source (drain) contact. Here we assume the boundaries of the gated and ungated nanowire channel is the edges of the source/drain region. Under small V_{DS}, the u_0 of Γ_S and Γ_D can be considered equal (as shown in Fig. 4c). Substituting this into equation 6 yields

$$G = \frac{e^2}{h}\frac{4e^{-2L}}{2e^{-2L} + e^{-4r_S} + e^{-4r_D}} \qquad \text{* MERGEFORMAT (3)}$$

where $L = r_S + r_D$ is the gate length.

Fig. S5 plots the result of equation 3. The curve shows that the closer the dopant atom is to the drain/source region, the smaller G is, and G reaches its maximum value of $G = e^2/h$ as $r_S = r_D$ (i.e., the dopant atom is placed in the middle of the channel).

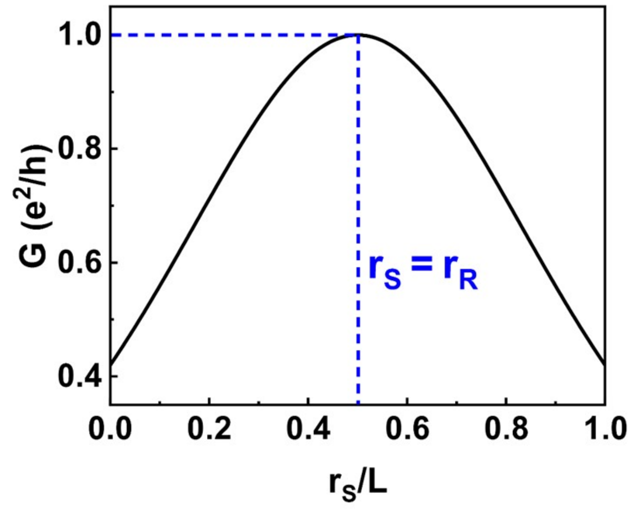

Fig. S5 The G of a single hole resonant tunneling in a double-barrier system. G reaches its maximum value of $G = e^2 / h$ at $r_\mathrm{S} / L = 0.5$ (i.e., $r_\mathrm{S} = r_\mathrm{D}$).

Section 6. DOS of HH and LH in silicon nanowires

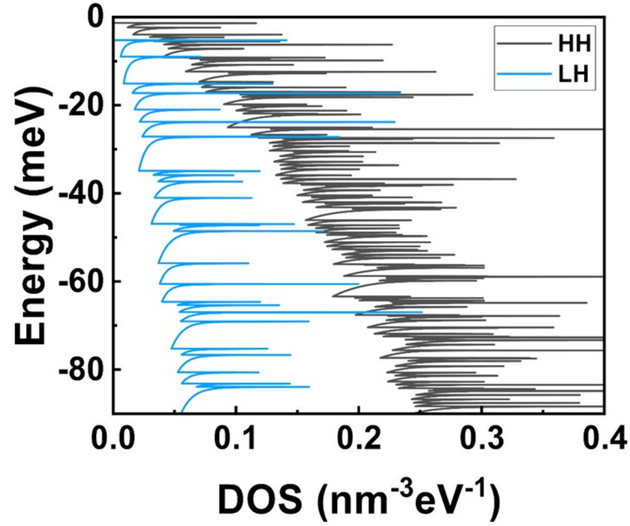

Fig. S6 The theoretical 1D DOS of HH (black) and LH (cyan) in silicon nanowire along the <110> direction with a cross-sectional area of $W_{\mathrm{Si}} \times H_{\mathrm{Si}} = 25 \times 45\ \mathrm{nm}^2$. The effective masses for HH and LH in the silicon channel are $m^*_{\mathrm{HH}} = 0.58\, m_0$ and $m^*_{\mathrm{LH}} = 0.15\, m_0$, respectively.

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