Supporting Information

Impact ionization threshold switching field-effect transistor

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Supplementary Section 1. Fabrication and characteristics of I^2S-FET

a. Fabrication process

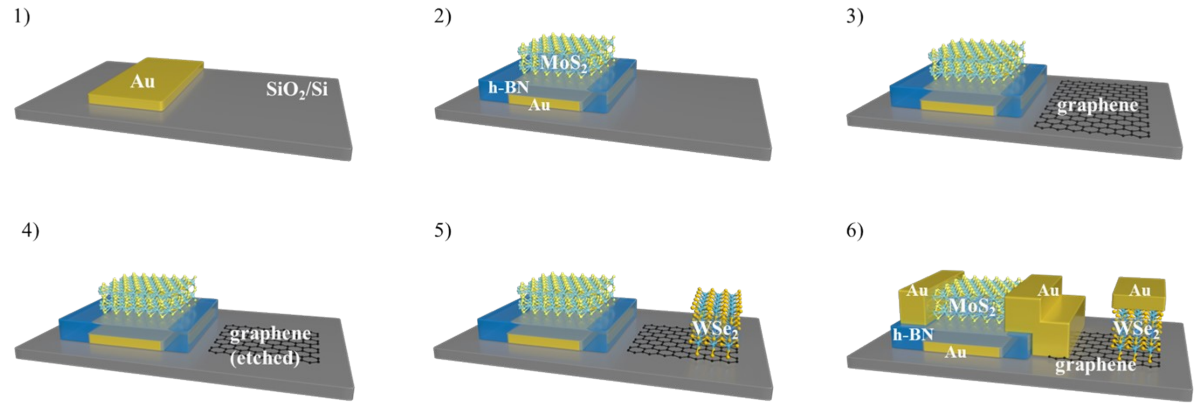

Figure S1. Schematic of the process flow for I^2S-FET fabrication.

Figure S1 illustrates the fabrication process of the I^2S-FETs. First, an individual back-gate electrode (Au, 25 nm) was deposited on the SiO_2/Si substrate. A dielectric layer (h-BN 75–100 nm) was then transferred onto the top of the back-gate electrode using a polydimethylsiloxane (PDMS) stamp. To prepare the MoS_2 channel layers, mechanically exfoliated MoS_2 flakes (25–40 nm) were transferred onto a previously prepared back-gate dielectric layer using a PDMS stamp. Graphene and WSe_2 were sequentially dry transferred onto the substrate similarly. Finally, the source-drain electrodes of the baseline MoS_2 FET and the top electrode of WSe_2 I^2S, which acts as a drain electrode of the entire device, were simultaneously defined using e-beam lithography and e-beam deposition of Au (~50 nm), followed by a lift-off process. Figure S2 shows optical images in the order of device fabrication.

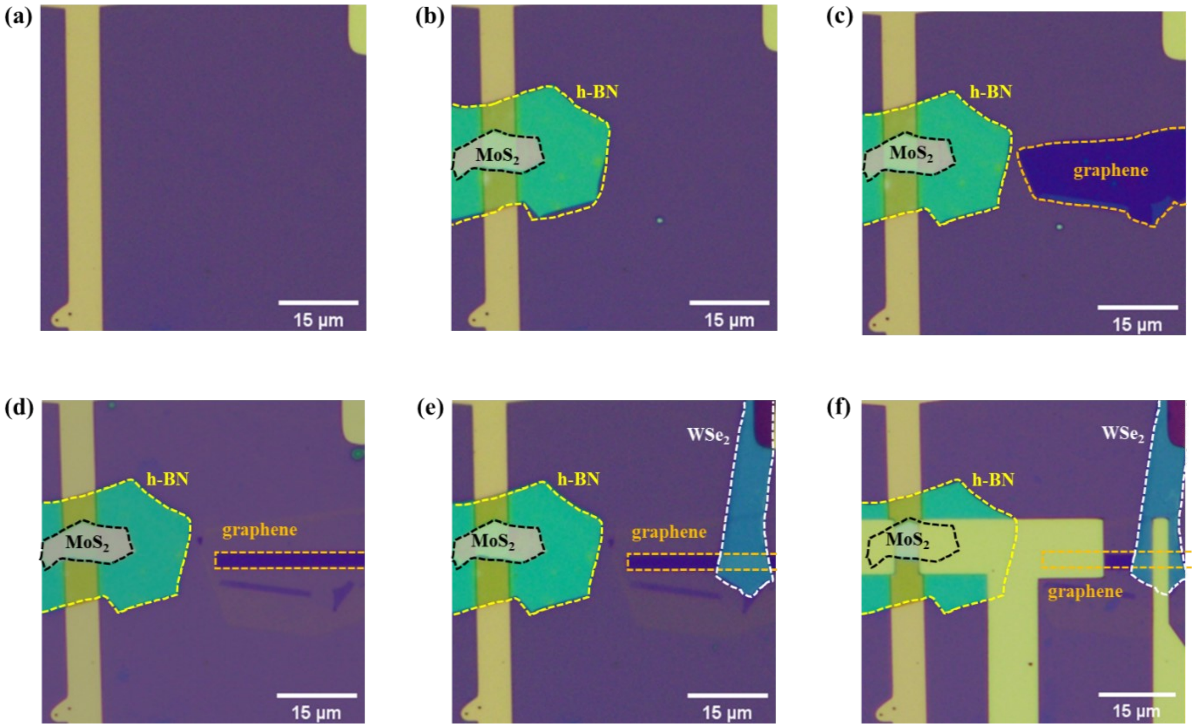

Figure S2. Optical images in the order of device fabrication. (a) Bottom electrode. Sequentially transferred (b) MoS$_2$, h-BN, and (c) bi-layer graphene (BLG). (d) ICP-etched BLG. (e) Stacked WSe$_2$ on BLG. (f) Source-drain electrodes.

b. Current oscillation in sub-threshold region

We divided the I_{DS}-V_{GS} curve into three regions (i.e., off, oscillation, and on regions) to explain the working mechanism of the I^{2}S-FET. The MoS$_2$ transistor still has a high resistance when an insufficient gate voltage is applied; thus, the magnitude of the drain voltage applied to the WSe$_2$ I^{2}S is not sufficient to cause impact ionization. Therefore, the overall current was limited to the off state of WSe$_2$ I^{2}S, as shown in the off region. As the gate voltage increases, the drain voltage applied to WSe$_2$ I^{2}S gradually increases. When the critical electric field is reached, electron-hole pairs are generated, and WSe$_2$ I^{2}S becomes metallic. However, because WSe$_2$ I^{2}S is switched to a low resistance (metallic), the baseline MoS$_2$ transistor is formed as if it has a relatively high resistance, and a redistribution of the drain voltage occurs, causing the voltage across the WSe$_2$ I^{2}S to drop below V_{BR}. Therefore, WSe$_2$ I^{2}S quickly transitions back to that before impact ionization occurs. These processes are quickly repeated and form oscillations, as shown in the oscillation region. The resistance of the MoS$_2$ transistor will be much lower when the gate voltage is sufficiently high such that the MoS$_2$ transistor will have a small drain voltage even when WSe_2 I^2S becomes metallic. It maintained the drain voltage distribution concentrated on WSe_2 I^2S over the V_{BR}. Therefore, the electric field applied to WSe_2 would not be dropped below the E_{CR} and the WSe_2 I^2S remained as a metallic channel, eventually turning on the entire device, as shown in the on state.

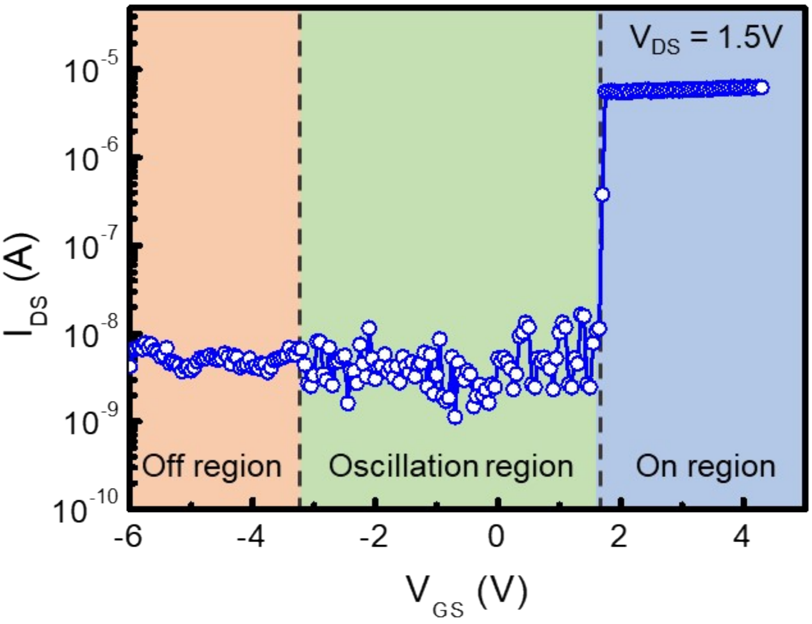

Figure S3. I_{DS}-V_{GS} transfer characteristics of the I^2S-FET, separated into off / oscillation (sub-threshold) / on (impact ionization) regions.

Supplementary Section 2. Electrical and transport properties of WSe_2 I^2S and I^2S-FET

a. Impact ionization characteristics of the WSe_2 I^2S

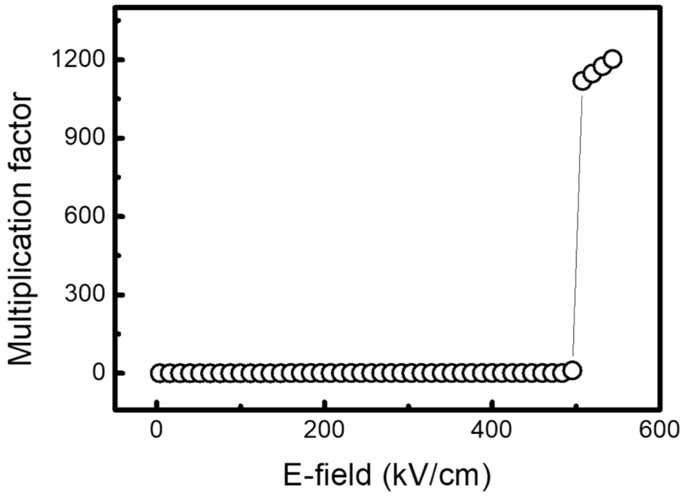

Figure S4. Multiplication factor as a function of the electric field

Figure S4 shows the multiplication factor defined as $M = I_{DS}/I_{sat}$ (here, I_{sat} is set as the saturation current just before the impact ionization-induced abrupt current increase), which is a function of the electric field. WSe_2 showed a high multiplication factor of over 1000, indicating that a large amount of carrier multiplication occurred in the WSe_2 channel.

b. Thickness dependence of the WSe_2 I^2S and I^2S-FET

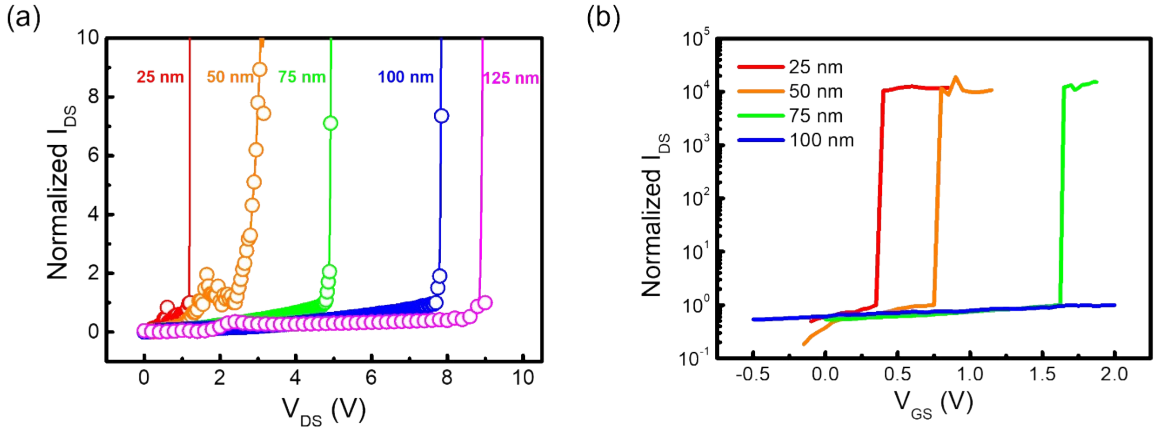

Figure S5. (a) I_{DS}-V_{DS} characteristics of the WSe_2 I^2Ss with various thicknesses. **(b)** Normalized I_{DS} of I^2S-FETs with various thicknesses as a function of V_{GS} at same applied drain bias of 5 V.

The impact ionization that induces an abrupt increase in the channel current can be reduced by adjusting the WSe_2 thickness of I^2S and the breakdown voltage (V_{BR}). Because the primary mechanism of I^2S is based on impact ionization, V_{BR} may be controlled by adjusting the channel thickness. Figure S5a shows the I-V characteristics of WSe_2 I^2S with different channel thicknesses. The V_{BR} decreased because the E_{CR} is a material-specific parameter (Figure 2c) as the thickness decreased. Moreover, Figure S5b shows the I_{DS}-V_{GS} characteristics of I^2FETs with various WSe_2 thicknesses under the same drain bias of 5 V. For this fixed V_{DS}, the V_{TH} required for impact ionization also decreases with the WSe_2 thickness.

c. Effect of Schottky barrier of Graphene/WSe_2 interface

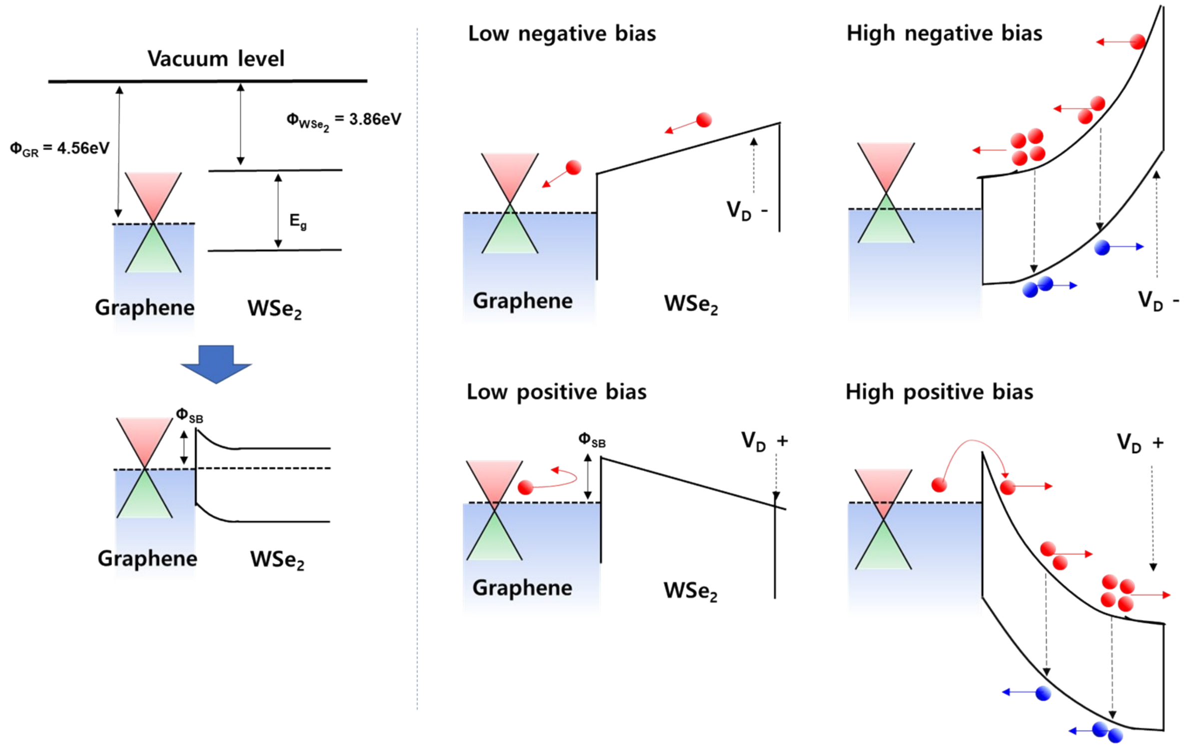

Figure S6. Band diagram of the WSe_2 I^2S under various drain bias conditions

WSe_2 I^2S exhibits steep switching characteristics with only a positive drain bias. Compared to a negative drain bias, a positive drain bias limits the off-current. This is the result of the asymmetric structure of Graphene/WSe_2, which will be exhibited through the analysis of each band alignment in Fig. S6. The band alignment after the corresponding drain voltage was applied. The Schottky barrier is formed in the direction of graphene crossing WSe_2 because the WSe_2 electron affinity is smaller than that of graphene [S1]. For a low negative drain voltage, the right side of the WSe_2 band rises, and electrons directly flow, regardless of the Schottky barrier. Even if impact ionization occurs by applying a strong negative drain voltage, a sharp increase in current cannot be observed because many electrons are already flowing. On the other hand, at a low positive drain voltage, the right side of the WSe_2 band is lowered and the flow of electrons is restricted by the Schottky barrier, ensuring a low off-current. Subsequently, a sharp increase in the current through impact ionization can be observed if a strong positive drain voltage is applied.

d. Device-to-device variation

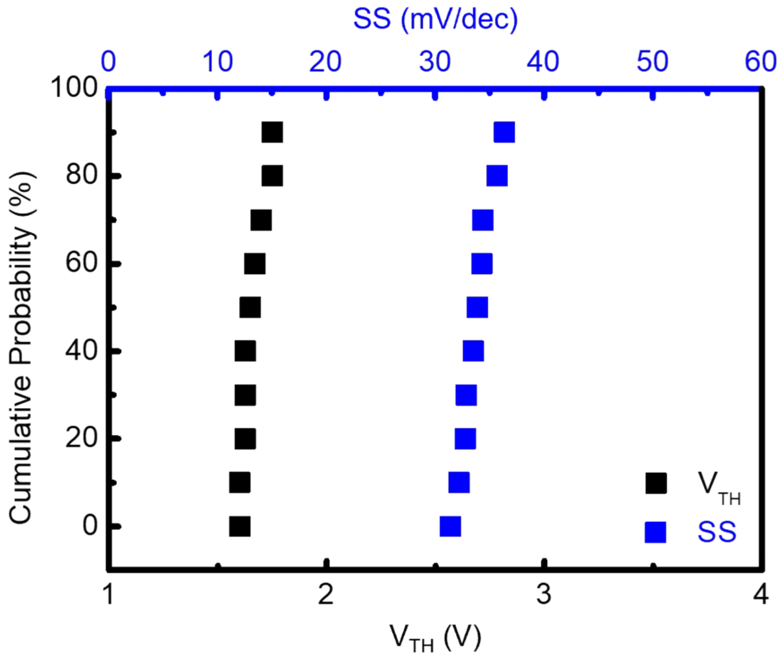

Figure S7. Device-to-device variation of V_{TH} and SS for 10 devices.

Figure S7 depicts the device-to-device variation of 10 samples. It shows the uniformity of threshold voltage (V_{TH}) and subthreshold swing (SS) of the device-to-device from 10 devices. The coefficient of variation (CV) for these values was calculated as CV = $(\sigma/\mu) \times 100$ (%), where σ and μ denote the standard deviation and absolute mean value. The measured results of these I2S-FETs show low CV values for both VTH (3.41 %) and SS (4.54 %), demonstrating the uniformity of VTH and SS under the same device conditions.

Supplementary References

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