Controllable digital and analog resistive switching behaviors of 2D layered WSe_2 nanosheets for neuromorphic computing

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(a)

Element	Wt%	Atomic %
C	5.53	20.38
O	2.86	7.90
Si	32.18	50.67
Se	21.62	12.11
W	27.94	6.72
Au	9.86	2.21
Total:	100.00	100.00

(b)

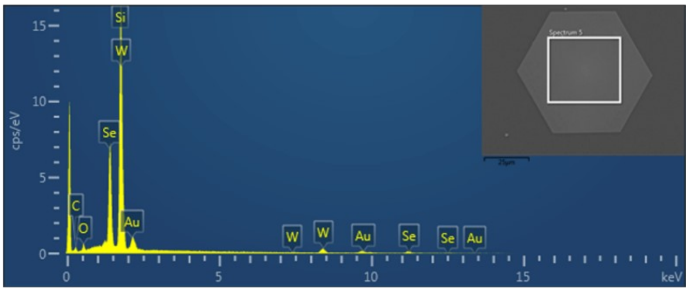

Fig. S1. Energy dispersive X-ray spectroscopy (EDS) analysis of the grown WSe_2 nanosheet. (a) Element weight percent of the WSe_2 nanosheet. (b) EDS spectrum of the WSe_2 nanosheet.

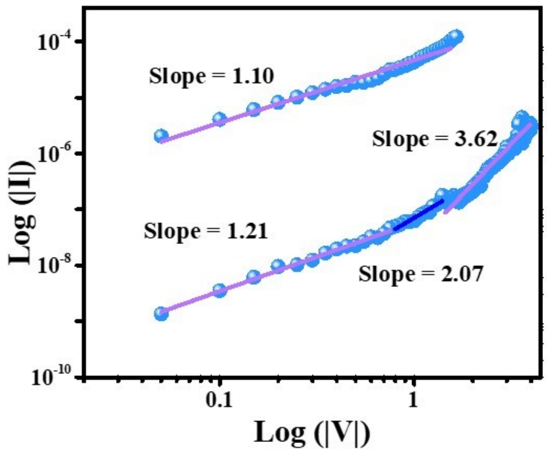

Fig. S2. The negative part of the current−voltage (*I*−*V*) curve in double logarithmic coordinates.

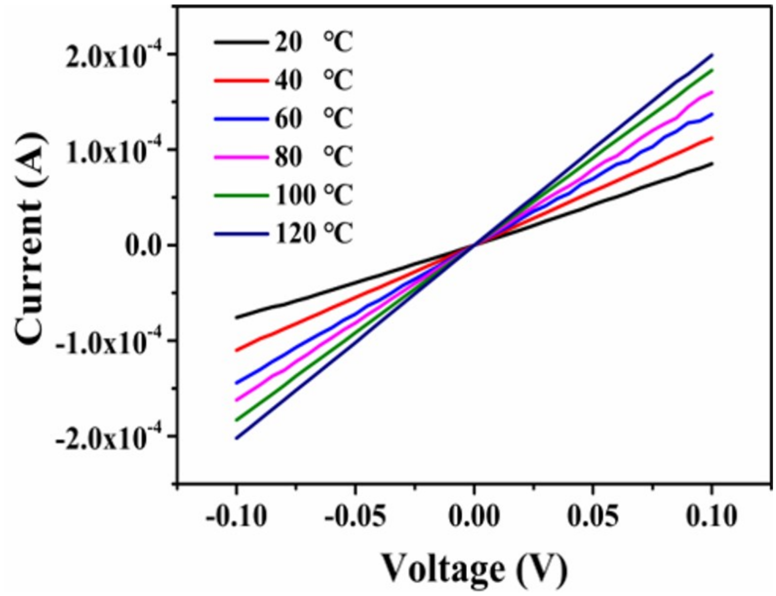

Fig. S3. The temperature dependent conductive behaviors of the WSe_2-based memristor at the low resistance state. As the temperature increases, the current increases, indicating the semiconducting conductive behaviors rather than the metallic conductance.

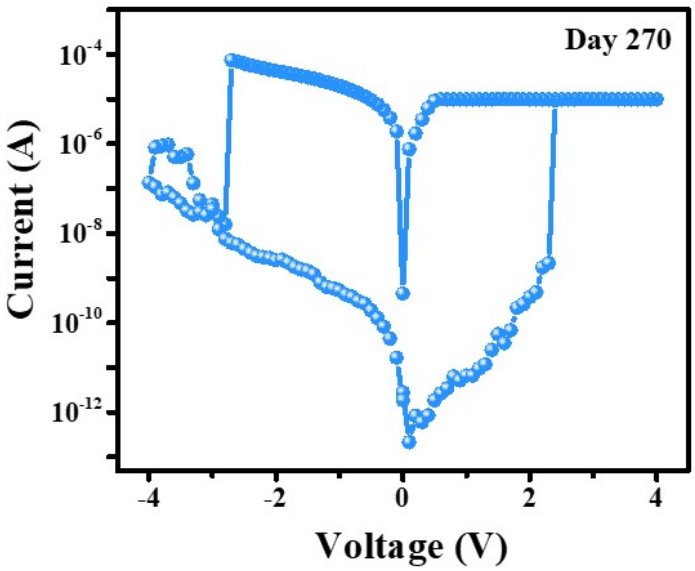

Fig. S4. The *I−V* curve of the Pt/WSe_2/Pt memristor for day 270 under ambient air condition. The non-volatile RS behavior can be maintained well.

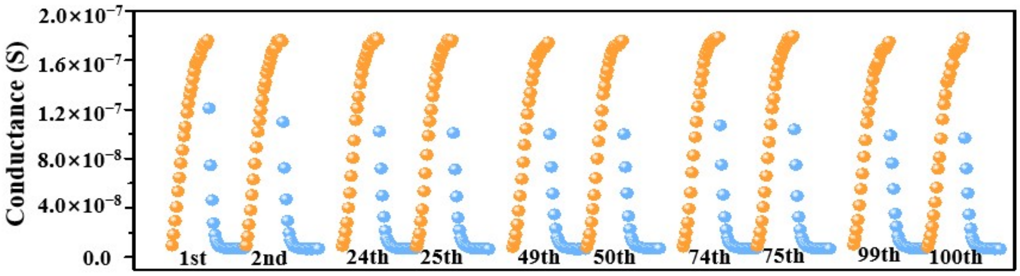

Fig. S5. Endurance test for the synaptic device in 100 LTP/LTD cycles. The selected cycles demonstrate consistent linearity and conductance margin.

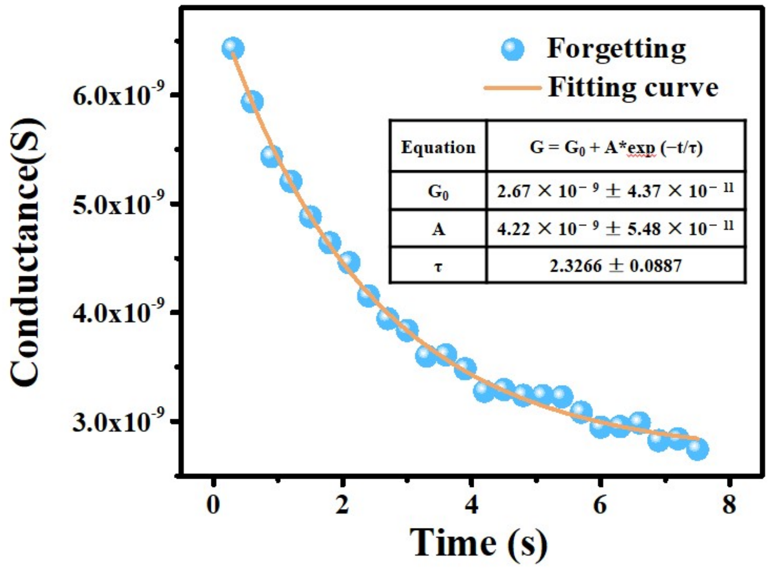

Fig. S6. The fitted forgetting curve of the synaptic memristor.

The forgetting process is fitted by an exponential decay with the equation of $G = G_0 + A*\exp(-t/\tau)$, where G is the recorded conductance, G_0 is the final conductance, A is the pre-factor, and τ is the relaxation time. For our synaptic memristor, the conductance decreases exponentially. By fitting the forgetting process, it can be concluded that the conductance decreases exponentially and finally can be retained at G_0 (2.67 nS). Thus, 41% in the conductance can be retained in the end after the forgetting process

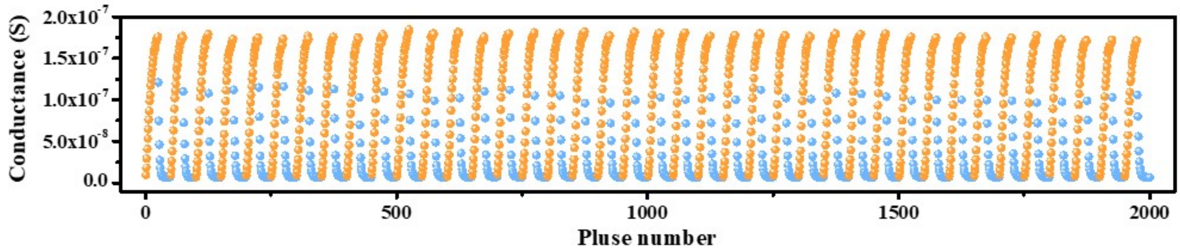

Fig. S7. The 40 sets of LTP/LTD cycles.