Electronic Supplementary Material (ESI) for Nanoscale.

Quantum transport of sub-5 nm InSe and In_2SSe monolayer and their heterostructure transistors

Hailing Guo[†], Yinheng Yin[†], Wei Yu[†], John Robertson[†], Sheng Liu[‡], Zhaofu Zhang[‡, *], and Yuzheng Guo[†, *]

[†] School of Electrical Engineering and Automation, Wuhan University, Wuhan, Hubei 430072, China

[‡] The Institute of Technological Sciences, Wuhan University, Wuhan 430072, China

* E-mail: yguo@whu.edu.cn

* E-mail: zhaofuzhang@whu.edu.cn

Table S1. Main parameters required by ITRS for the current (2022), mid-term (2026) and long-term (2028) nodes for both high-performance (HP) and low-power (LP) technologies.

	HP2022	**LP2022**	**HP2026**	**LP2026**	**HP2028**	**LP2028**
Channel length (nm)	8.8	10.1	6.1	7.0	5.1	5.9
V_{DD} (V)	0.72	0.72	0.66	0.66	0.64	0.64
EOT (nm)	0.54	0.54	0.45	0.45	0.41	0.41
I_{off} (μA/μm)	0.10	2×10^{-5}	0.10	4×10^{-5}	0.10	5×10^{-5}
I_{on} (μA/μm)	1350	461	1030	337	900	295
PDP (fJ/μm)	0.45	0.52	0.29	0.34	0.24	0.28
τ (ps)	0.46	1.56	0.43	1.51	0.42	1.49
I_{on}/I_{off}	1.35×10^{4}	2.31×10^{7}	1.03×10^{4}	8.43×10^{6}	9×10^{3}	5.9×10^{6}

[a] V_{DD} is the supply voltage; I_{off} and I_{on} are the currents in the off and in the on state, respectively; PDP is the dynamic power indicator; τ is the intrinsic delay time; and I_{on}/I_{off} is the ratio between the on and the off currents.[1]

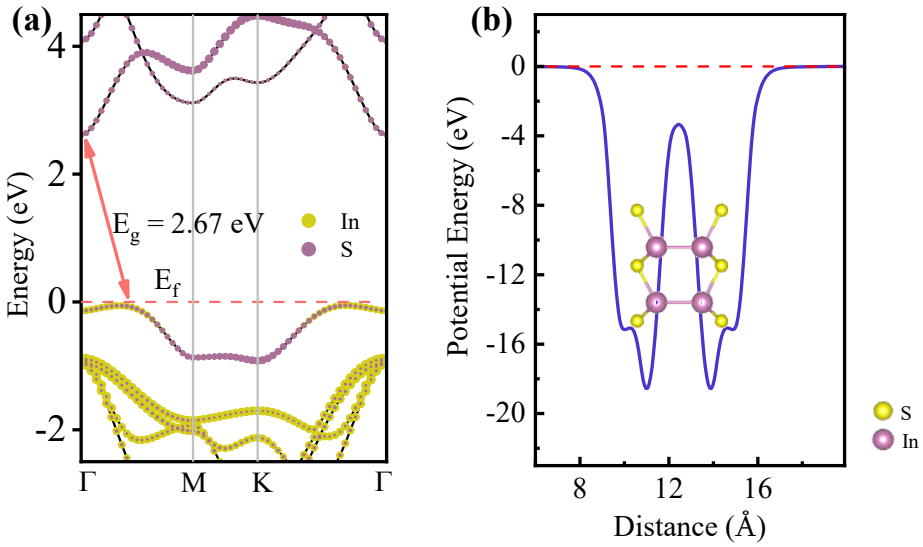

Fig. S1. (a) Projected band structures of InS monolayer by HSE06 functional. The VBM is set to zero. (b) Average electrostatic potential for InS monolayer. The inserted figures show the side views of monolayer structures.

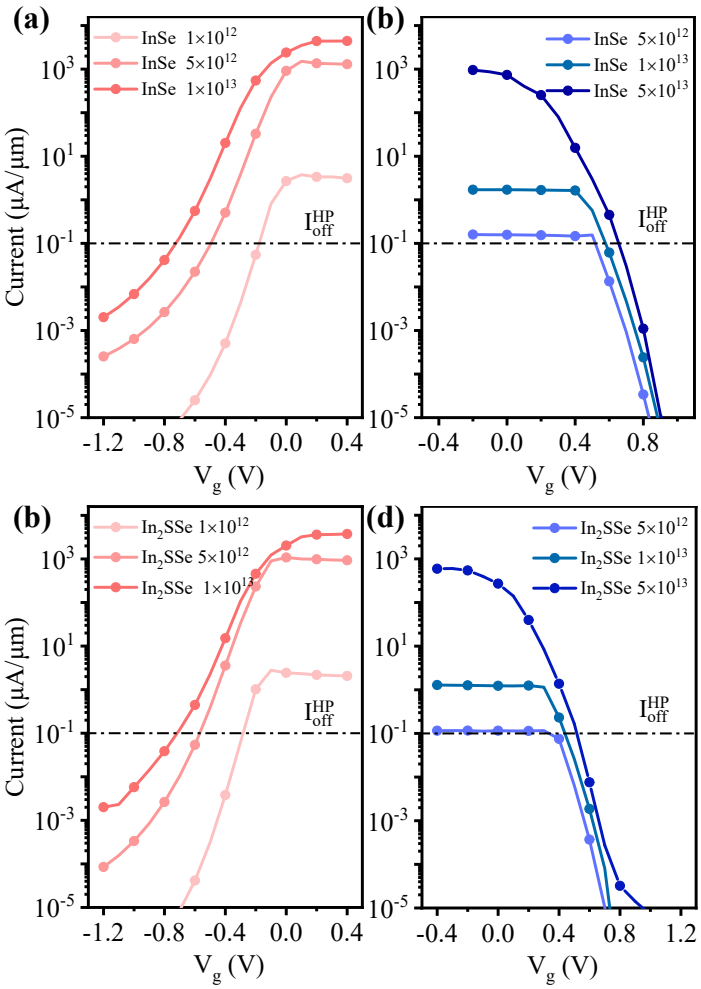

Fig. S2. Transfer characteristics of the (a) n-type and (b) p-type 5nm L_g ML In_2SSe MOSFETs without UL for different electron doping concentrations in the source and drain.

Three kinds of doping level are tested for the 5nm-L_g InSe and In_2SSe MOSFETs without underlap structure. The transfer characteristics are provided in **Fig. S2**. The maximum current increases significantly when the source and drain increase from *Ne* = 1.0×10^{12} cm^{-2} to *Ne* = 1.0×10^{13} for n-type MOSFET and from N_h = 5.0×10^{12} cm^{-2} to N_h =5.0×10^{13} for p-type MOSFET. Therefore, the optimal n-type doping concentration of 1.0×10^{13} cm^{-2} and p-type doping concentration of 5.0×10^{13} cm^{-2} are chosen here.

Table S2. Benchmark of the simulated ballistic device performances of the sub-5 nm gate-length of n-type InSe and Janus In_2SSe MOSFETs, and against the ITRS and IRDS requirements for HP and LP devices of the next decades[a]

System	Lg (nm)	L_{UL} (nm)	SS (mV/dec)	I_{off} (μA/μm)	I_{on} (μA/μm)	I_{on}/I_{off}	τ (ps)	PDP (fJ/μm)
InSe n-type	5	0	123	0.1	1418	1.42×10^4	0.032	0.029
	3	0	222	0.1	–	–	–	–
	3	2	155	0.1	1220	1.22×10^4	0.027	0.025
	1	0	593	0.1	–	–	–	–
	1	3	228	0.1	140	1.40×10^3	0.017	0.022
In_2SSe n-type	5	0	128	0.1	1206	1.21×10^4	0.035	0.032
	3	0	257	0.1	–	–	–	–
	3	2	121	0.1	1043	1.04×10^4	0.028	0.028
	1	0	665	0.1	–	–	–	–
	1	3	178	0.1	94	9.40×10^2	0.013	0.026
ITRS HP	5.1				900	9.00×10^3	0.432	0.24
IRDS HP					923			0.40
InSe n-type	5	0	123	4×10^{-5}	–	–	–	–
	5	2	97	4×10^{-5}	523	1.04×10^7	0.068	0.017
	5	3	83	4×10^{-5}	326	6.52×10^7	0.057	0.013
	3	0	222	4×10^{-5}	–	–	–	–
	1	0	593	4×10^{-5}	–	–	–	–
	1	3	155	4×10^{-5}	63	1.26×10^6	0.027	0.025
In_2SSe n-type	5	0	128	4×10^{-5}	–	–	–	–
	5	2	93	4×10^{-5}	465	9.30×10^7	0.072	0.024
	5	3	79	4×10^{-5}	321	6.42×10^7	0.062	0.025
	3	0	222	4×10^{-5}	–	–	–	–
	1	0	593	4×10^{-5}	–	–	–	–
	1	3	155	4×10^{-5}	56	1.12×10^6	0.026	0.035
ITRS LP	5.1				295	5.90×10^6	1.493	0.28
IRDS LP					520			0.40

[a]The off-state current is set to 0.1 μA/μm in terms of the ITRS HP standards and 5×10^{-5} μA/μm in terms of the ITRS LP standards. V_{dd}: supply voltage; SS: subthreshold swing; τ: delay time; PDP:

Table S3. Benchmark of the simulated ballistic device performances of the sub-5 nm gate-length of p-type InSe and Janus In_2SSe MOSFETs, and against ITRS and IRDS requirements for HP devices of the next decades[a]

System	Lg (nm)	L_{UL} (nm)	SS (mV/dec)	I_{off} (μA/μm)	I_{on} (μA/μm)	I_{on} /I_{off}	τ (ps)	PDP (fJ/μm)
InSe p-type	5	0	148	0.1	1216	1.22×10^4	0.048	0.035
	3	0	375	0.1	877	8.77×10^3	0.254	0.025
	1	0	794	0.1	–	–	–	–
In_2SSe p-type	5	0	157	0.1	1105	1.22×10^4	0.064	0.044
	3	0	390	0.1	654	6.54×10^3	0.056	0.036
	1	0	755	0.1	–	–	–	–
ITRS HP	5.1				900	9.00×10^3	0.423	0.240
IRDS HP	12				923			0.40
InSe p-type	5	0	148	4×10^{-5}	397	7.94×10^6	0.214	0.056
	3	0	375	4×10^{-5}	142	2.84×10^6	0.263	0.042
	1	0	794	4×10^{-5}	–	–	–	–
In_2SSe p-type	5	0	157	4×10^{-5}	361	7.22×10^6	0.312	0.065
	3	0	390	4×10^{-5}	132	2.64×10^6	0.258	0.051
	1	0	755	4×10^{-5}	–	–	–	–
ITRS LP	5.1				295	5.90×10^6	1.493	0.280
IRDS LP	12				520			0.40

[a]The off-state current is set to 0.1 μA/μm in terms of the ITRS HP standards and 5×10^{-5} μA/μm in terms of the ITRS LP standards. V_{dd}: supply voltage; SS: subthreshold swing; τ: delay time; PDP: power dissipation.

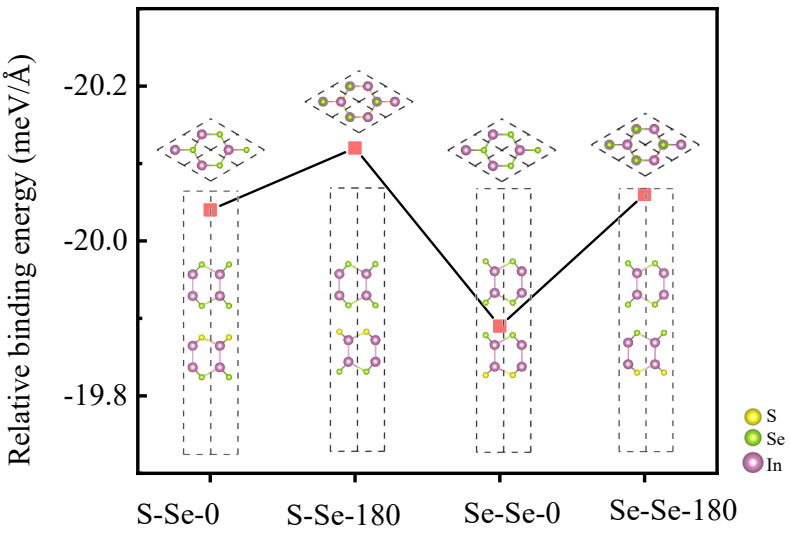

Fig. S3. The relative energy of InSe/In_2SSe heterostructures with high-symmetry stackings. Inserts in the figure are the top view and side view of the respective stacking geometry.

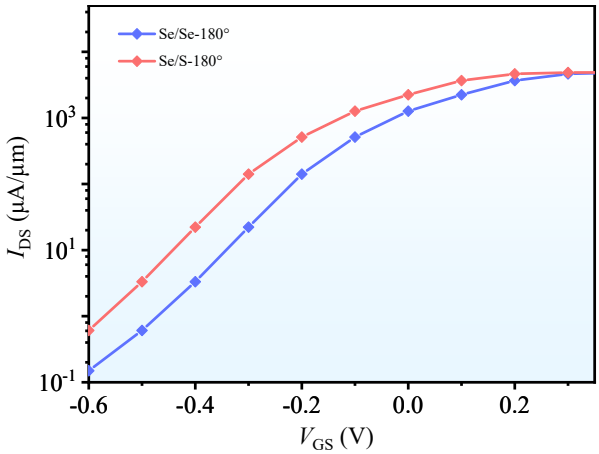

Fig. S4. Transfer characteristics of InSe/In_2SSe heterostructures with different stacking pattern. V_{ds} = 0.64 V is adopted.

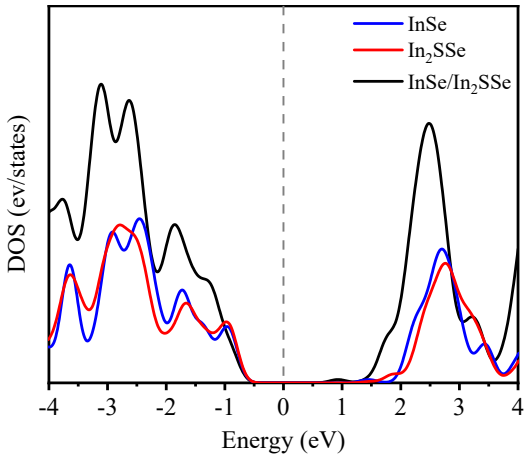

Fig. S5. Density of states of InSe monolayer, In_2SSe monolayer and InSe/In_2SSe heterostructure. The Fermi level is aligned at zero.

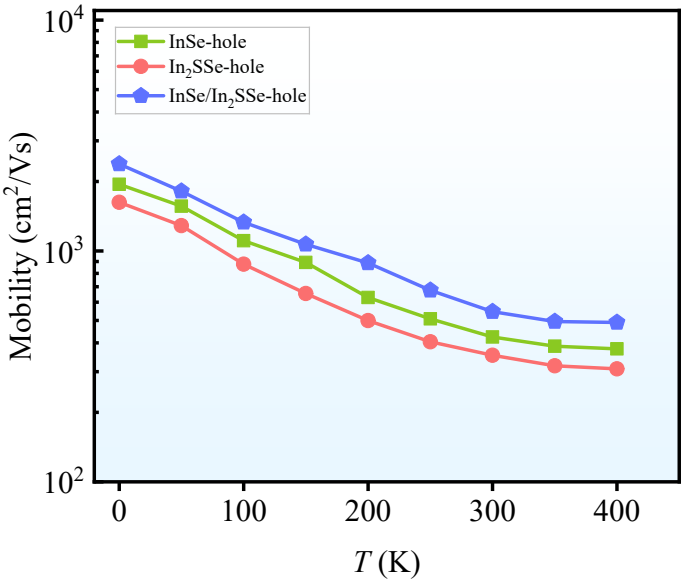

Fig. S6. Phonon-limited hole mobility of InSe monolayer, In_2SSe monolayer and InSe/In_2SSe heterostructure at different temperatures.

Fig. S7. (a) Band edge position of InSe/In_2SSe heterostructure. (b) The charge redistribution of InSe/In_2SSe. The yellow isosurface represents charge accumulation while blue represents depletion. The inner electric field points from InSe side to In_2SSe side.