Supplementary Information for:

Mimicking Biological Synaptic Plasticity with

a Leaky Charge-Trap FinFET

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1. Fabrication procedure of the leaky-charge trap (LCT) FinFET

**Figure S1.** Process flow of the LCT-FinFET fabrication.

**Figure S1a** shows the basic sequential process flow used to fabricate the LCT-FinFET. A p-type 8-inch silicon-on-insulator (SOI) wafer with (100) crystal orientation was used as a starting material. The thickness of the top Si and the buried oxide (BOX), were 145 nm and 400 nm, respectively (**Figure S1b**). The thickness of the top Si was thinned to 40 nm by thermal oxidation and subsequent wet etching with diluted HF. Using conventional photo-lithography and plasma etching, it was patterned to define the Si-fin as a channel (**Figure S1c**). Afterwards, nitride (Si₃N₄) with a thickness of 3.5 nm was deposited by low-pressure chemical vapor deposition (LPCVD) for a charge trap layer (**Figure S1d**). Tetraethyl orthosilicate (TEOS) oxide with 2 nm thickness was deposited as a blocking layer and then in-situ heavily doped n⁺ gate poly-silicon (poly-Si) with 100 nm thickness was sequentially deposited by LPCVD (**Figure S1e**). It was then planarized by chemical-
mechanical polishing (CMP). Then, nitride was deposited by LPCVD, to serve as a hard-mask for patterning the gate electrode (Figure S1f). After patterning the hard-mask nitride using gate photo-lithography (Figure S1g), the photoresist (PR) was removed. With the aid of the etching stopper (hard-mask nitride) the poly-Si gate was patterned by plasma etching (Figure S1h). Afterwards, the residual hard-mask nitride was eliminated during the formation of sidewall spacers (Figure S1i). Source and drain (S/D) regions were doped with arsenic by ion implantation with a dose of $5 \times 10^{15}$ cm$^{-2}$. Lastly, dopants were activated by a rapid thermal annealing (RTA) process at 1000 °C for 5 sec (Figure S1j). Forming gas annealing (FGA) with diluted H$_2$ gas was adopted to minimize the trap density at the interface of the charge trap nitride (Si$_3$N$_4$) and the Si-fin.

2. Device-to-device variability of LCT-FinFETs

Device-to-device variability was determined for 20 different LCT-FinFETs, as shown in Figure S2. Three basic parameters, transfer characteristics ($I_D-V_G$), threshold voltage with forward bias sweeping ($V_{T,FWD}$), and hysteresis voltage window ($\Delta V_T$).
and hysteresis voltage window ($\Delta V_T$) were measured. Here, $\Delta V_T$ is defined as the difference in the threshold voltage between forward biasing and reverse biasing, i.e., $\Delta V_T = V_{T,REV} - V_{T,FWD}$. Twenty different devices were randomly selected among all the LCT-FinFETs on an 8-inch wafer. Although there were some limitations due to the university equipment and facility, fairly uniform characteristics were obtained using a 100% CMOS process. This uniformity is expected to be further improved if industrial facilities used for mass-production are employed.

3. PSC and PPF index after inhibition spike

![Graphs showing IPSC and PPF index](image)

Figure S3. Inhibitory post-synaptic current (IPSC) response. a, IPSC after a single positive pre-synaptic spike, b, Inhibitory PPF index with respect to different time intervals ($\Delta t_{interval}$).
Figure S4. Memory transition from sensory memory (SM) via short-term memory (STM) to long-term memory (LTM) according to positive $V_G$. STM and LTM plasticities also coexisted in the inhibitory operation.

Figure S3a shows the IPSC after a single positive pre-synaptic spike with a $V_G$ of 5 V and $t_G$ of 10 $\mu$s. The post-synaptic current was reduced after the inhibitory spike. In addition, the inhibitory PPF index with respect to different time intervals ($\Delta t_{\text{interval}}$) was also well-fitted to a double-exponential decay function (Figure S3b). Memory transition from SM via STM to LTM was also achieved in the inhibitory operation (Figure S4). When a $V_G$ of +5 V was applied, the change in synaptic weight ($\Delta W$) was reduced to less than |5| % prior to 50 sec. In contrast, when the $V_G$ of +6 V was biased, a $\Delta W$ of more than |20| % was maintained even after 200 sec.
4. Energy consumed during for modulation of synaptic plasticity

<table>
<thead>
<tr>
<th></th>
<th>Pre-synaptic pulse ((V_G, t_G))</th>
<th>Gate current ((I_G))</th>
<th>Energy Consumption ((V_G I_G t_G))</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Excitatory</strong></td>
<td>(-5 V, 10 µs)</td>
<td>-1.15 nA</td>
<td>57.5 fJ/spike</td>
</tr>
<tr>
<td><strong>Inhibitory</strong></td>
<td>(+5 V, 10 µs)</td>
<td>1.29 nA</td>
<td>64.5 fJ/spike</td>
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Table S1 shows the energy consumed with an applied pre-synaptic voltage of \(V_G\) and \(t_G\), to modulate synaptic plasticity. Although the tunneling barrier layer was removed to enable leaky-charge characteristics, the blocking oxide layer (TEOS) suppresses gate leakage current \((I_G)\) while applying pre-synaptic spikes. When ±5 V pre-synaptic pulses were applied, the measured \(I_G\) were 1.29 nA and -1.15 nA, respectively. As a consequence, the energy consumption while modulating the synaptic plasticity was approximately 60 fJ/spike, which is comparable to the energy consumption of a biological synapse in the human brain (10 fJ/spike).
5. Spike timing dependent plasticity (STDP) according to synaptic learning rule

Figure S5. STDP synaptic learning rule. a, Schematic illustration of the applied pre- and post-synaptic spikes applied for symmetric behavior. b, Symmetric Hebbian behavior. c, Symmetric anti-Hebbian behavior can be observed when opposite polarity pre- and post- synaptic spikes were applied to the case in Figure S5a.

In the STDP synaptic learning rule, synaptic plasticity is modulated in response to the time interval ($\Delta t_{\text{interval}}$) between the pre- and post- synaptic spike ($V_{\text{pre}}$ and $V_{\text{post}}$). Figure S5a shows the waveform of an applied pre- and post-synaptic spike. To reduce the hot carrier effect induced by the high lateral electric field ($E_{\text{lateral}}$) between the source and drain, a small amplitude of 2 V ($V_D$) was used as a post-synaptic spike. $\Delta W$ is well-fitted to a Gaussian distribution, which shows a typical symmetric Hebbian and a symmetric anti-Hebbian learning behavior, as shown in Figures S5b and c.