

Ultra-low temperature synthesis of Ge-based optical materials and devices on Si using GeH₃Cl

Aixin Zhang, Matthew A. Mircovich, Dhruve A. Ringwala, Christian D. Poweleit, Manuel A. Roldan, José Menéndez, and John Kouvetakis

General experimental details of synthesis and device processing

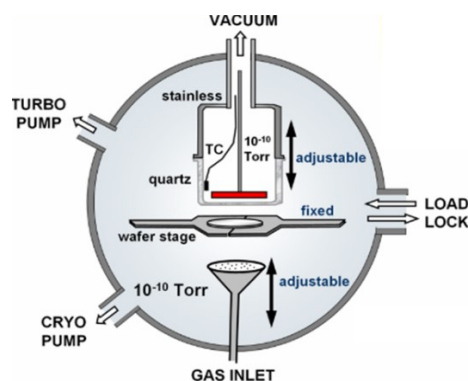


Figure 1: Schematic of GSME reactor showing the internal CVD elements of the system (J. Vac. Sci. Technol. A 39, 063411, 2021)

All chemical reagents are handled using standard dry box and high vacuum line techniques. GeH₃Cl was prepared, purified and characterized using the procedure described in Ref 21 in the main text. The yield in our hands can be enhanced up to 88% by using higher GeH₄ pressures up to 3 atmospheres in the reaction mixture. This is contained in a stainless steel reaction vessel and allowed to react with excess SnCl₄ for two days. The typical amount of GeH₃Cl produced in our experiments vary from 2.5 grams to 7 grams depending on the amount of starting materials. We note that residual SnCl₄ impurities must be completely removed by successive distillation of the crude product to fully purify GeH₃Cl. The dopant P(SiH₃)₃ compound is prepared in ~ 50 % yield by reaction of Li₃P and SiH₃Cl or SiH₃Br and characterized by gas phase IR and vapor pressure measurements. SnD₄ was produced by standard literature methods and the compound was stored in a liquid nitrogen dewar to avoid decomposition (A.R. Norman, J.R. Webster, W.L. Jolly, R.A. Gorse W.R Bornhorst, M.A. Ring Inorganic Synthesis, volume 11, pages 178-181).

Film growth synthesis procedures and methods: The Ge and GeSn depositions were conducted in a custom designed gas-source molecular epitaxy reactor (GSME). A schematic of the apparatus showing the CVD components inside the stainless steel UHV chamber is illustrated in Figure 1 (for more details see J. Vac. Sci. Technol. A 39, 063411, 2021). The wafer stage is located in the middle of the chamber in line with the load lock. The latter is differentially pumped and is used to transfer the wafers in and out of the chamber without breaking vacuum. The heater assembly is enclosed in a differentially pumped quartz jar to prevent exposure of the heating elements to the reactor ambient and chemicals during the growth experiment. The vertical position of the heater is adjusted to a distance of ~ 2 mm away from the backside of the wafer enabling efficient radiant heating of the Si substrate. The latter is placed upside

down on the sample stage and it is rotated during growth promoting better temperature uniformity of the wafer. The temperatures quoted in the paper correspond to those of the heater and are measured by a thermocouple (TC) inside the quartz cage as shown in the image. The actual substrate temperatures are typically ~ 20 °C lower. We note that under these conditions, we found that smaller size or conductive substrates are heated more efficiently than the full 4" wafers or resistive analogs. In some cases the temperatures of the heater inside the reactor is slightly modified to offset these thermal differences on the samples.

In a typical experiment the gaseous reactants are inserted into the chamber using a differentially pumped injection manifold (not shown in Figure 1) through a gas inlet tube terminating in a showerhead (shown in Figure 1). The vertical position of the latter is adjustable allowing precise control of its distance from the wafer surface. This is typically set to ~ 4 inches in the experiments conducted in the current work. UHV is achieved using a cryo/turbo pump assembly as shown in the figure, yielding typical base pressure of 10⁻¹⁰ Torr. The substrates used for all experiments were 4" Si(100) p-type wafers doped with B, exhibiting 10-20 Ωcm resistivity. Prior to growth the wafers were first RCA cleaned and then chemically etched with 5% HF/methanol solutions, rinsed with methanol, and blown dried with N₂. They were then loaded into the reactor and degassed at 400-450 °C on the wafer stage under UHV conditions. The wafers were subsequently flashed at 800-900 °C for 1 minute 3 times to prepared an epi ready surface and allowed to cool to the desired growth temperature to commence the growth experiment.

The growth temperature of Ge films was kept between 330 and 370 °C. A container with a pure GeH₃Cl liquid sample was attached to the injection manifold which was differentially pumped to 10⁻⁸ Torr. The pure room temperature vapor of the compound was then released into the chamber using a high precision leak valve. The pressure inside the chamber was raised from 10⁻¹⁰ Torr to 5×10⁻⁵ Torr by carefully increasing the amount of the flux flown, and was kept constant throughout each run by continuous pumping of the chamber contents by a turbo pump shown in the Figure. All experiments produced Ge films with mirror-like surfaces devoid of visible surface features and defects. Films grown at 330 °C exhibited a nominal thickness of 500 nm and a growth rate of ~ 2-3 nm min⁻¹ on 4" wafers, and 8 nm min⁻¹ on quadrants of these wafers. Ge films grown between 330–370°C exhibited thicknesses from 300 nm to 800 nm depending on the duration of the run. The growth rate in this case increased from 2 nm min⁻¹ at 330 °C to 9-10 nm min⁻¹ at 370 °C, irrespective of final thickness. The doped n-type Ge layers were produced at 360 °C and 5×10⁻⁵ Torr with similar growth rates as the intrinsic counterparts using a reaction mixture containing GeH₃Cl vapor and P(SiH₃)₃ vapor, 95% and 5% by volume, respectively. Active carrier concentrations of 1-2×10¹⁹/cm⁻³ were achieved as measured by IR ellipsometry.

Precursor synthesis:

The $\text{Ge}_{1-y}\text{Sn}_y$ alloys described in the paper were synthesized by reactions of GeH_3Cl and SnD_4 vapors without gaseous carriers. The substrates were 4" Si wafers incorporating 450-500 nm-thick Ge buffer layers. These virtual platforms were first wet-cleaned by dipping them in 5% HF and then flashed on the sample stage at 650 °C under UHV conditions. Separate glass vessels, one containing a pure SnD_4 gaseous sample (9 liter-Torr) and the other a pure GeH_3Cl liquid sample (2-3 grams), were attached to different ports of the injection manifold using high vacuum fittings and the entire introduction system was evacuated to 10^{-8} Torr. The GeH_3Cl vapor was then introduced first into the chamber through the manifold using a leak valve setting the pressure inside the reactor at 4×10^{-5} Torr. The SnD_4 vapor was injected immediately thereafter using a separate leak valve increasing the pressure to a total final level of 6×10^{-5} Torr. A series of growths was performed under these conditions by varying the temperature between 200 °C to 235 °C producing mirror like films in all cases. These were characterized and the results are described in the main text of the paper. The typical growth run ended when the SnD_4 supply was depleted over the course of ~ 100 minutes. Fresh SnD_4 was dispensed for each run. The same GeH_3Cl liquid supply was used from run to run.

Samples with 4-4.5 % Sn were also grown by UHV-CVD reactions using stoichiometric amounts of SnD_4 and GeH_3Cl . The operating protocols of the CVD tool, the sample preparation procedure including substrate cleaning and handling and formulation of chemical mixtures is essentially identical to those used to grow GeSn via stoichiometric reactions SnD_4 with Ge_3H_8 . Details of the approach are provided in a recent paper by Mircovich et al. ACS Appl. Electron. Mater. 2021, 3, 3451-3460 (see SI section of the reference).

Films characterization procedures: Spectroscopic ellipsometry was used to estimate layer thicknesses and doping carrier concentration using a JA Woollam IR Vase instrument with a range of 1.7 microns to 30 microns. The AFM images were obtained in tapping mode using a Bruker MultiMode 8 microscope. High resolution X-ray diffraction (XRD) was used to characterize crystallinity and determine lattice parameters and strain states. The XRD measurements were conducted using a Panalytical X'Pert Pro MRD using $\text{Cu K}\alpha_1$ radiation. The instrument is equipped with a hybrid 4-bounce monochromator and a high precision triple axis detector. High resolution TEM was performed using a JEOL ARM 200F atomic resolution microscope with 200 kV operating voltage. Bright field (BF) and medium angle annular dark field (MAADF) images in STEM mode were obtained and analyzed as described in the paper. The photoluminescence spectra were collected at room temperature using a custom system comprising of a 980 nm laser with 200 mW net output power, a chopper that provides modulation, a 1064 nm long-pass filter, a lock-in amplifier, a Horiba MicroHR spectrometer, and a liquid nitrogen-cooled InGaAs detector. Hall measurements were made using an Ecopia HMS-3000 Hall instrument equipped with a four point probe. An indium-tin eutectic sample was used to make electrical contacts to the wafer surface. Raman spectra for $\text{Ge}_{1-y}\text{Sn}_y$ films and bulk Ge were measured at room temperature using 514 nm excitation. The incident power was 1 mW and the light was focused on the sample using a 100X objective. The scattered radiation was dispersed with an Acton 0.500 m spectrometer and collected with a CCD detector. All the spectra were obtained in the "allowed" $z(x,y)z$ configuration (Porto

notation), where x,y,z are the cartesian directions in the cubic diamond lattice.

Device fabrication and measurement procedures: The n-p-i Ge diodes are grown on Ge buffered Si and are characterized as described in the main text. The samples were taken in the cleanroom and processed into photodiodes comprising circular (50-300 micron diameter) mesas etched down to the n-layer which serves as the bottom electrical contact. The top and bottom contacts comprise Cr/Au stacks in the form of ring-shaped circular pads. The device fabrication process employed here including photolithography, etching and metal contact formation was developed in previous studies. A detailed step-by-step procedure is provided by J.D. Gallagher in his Ph.D. thesis titled "The optical and electronic properties of $\text{Ge}_{1-y}\text{Sn}_y$ and $\text{Ge}_{1-x-y}\text{Si}_x\text{Sn}_y$ materials and devices for silicon-integrated optoelectronics" ASU November 2015, Appendix A, pages 171-188.

Briefly, the Ge surface was first cleaned by sonicating the samples in methanol, followed by deposition an initial SiO_2 layer by plasma-enhanced CVD of SiH_4 and N_2O . The layer serves a protection barrier for the ensuing fabrication steps. Next, photolithography using standard photoresist was employed to pattern the circular device mesas. These were defined by etching the n-i-p device stack down to the bottom n-layer using reactive-ion BCl_3 plasma. The photoresist and protective oxide were then removed using solution methods and a suitable passivating SiO_2 antireflection coating was deposited by plasma CVD. This was followed by a second lithography step to define the metal contact regions. The oxide layer in the contact areas was etched and the Cr/Au metal stack was then deposited on the n- and p-type layers by e-beam evaporation. The thickness of the Cr and Au layers in the stack were 20 nm and 200 nm, respectively. The electrical pads were finally formed by lift off. This was followed by cleaning the device surface from residual photoresist and other impurities in an oxygen plasma. Optical microscopy and SEM inspections were then made of the fabricated samples to check the definition of the mesa patterns and ensure successful lift-off for the metal contacts. Measurements of the IV curves were conducted using a conventional probe station. The responsivities of the devices were measured using a custom spectrometer system as described in main text of the paper.