

## **Pentagonal 2D Layered PdSe<sub>2</sub>-based Synaptic Device with Graphene Floating Gate**

*Eunpyo Park<sup>1,2‡</sup>, Jae Eun Seo<sup>3,4‡</sup>, Gichang Noh<sup>1</sup>, Yooyeon Jo<sup>1</sup>, Dong Yeon Woo<sup>1</sup>, In Soo Kim<sup>5</sup>,  
Jongkil Park<sup>1</sup>, Jaewook Kim<sup>1</sup>, YeonJoo Jeong<sup>1</sup>, Suyoun Lee<sup>1</sup>, Inho Kim<sup>1</sup>, Jong-Keuk Park<sup>1</sup>,  
Sangbum Kim<sup>2</sup>, Jiwon Chang<sup>3,4\*</sup> and Joon Young Kwak<sup>1,6\*</sup>*

<sup>1</sup>Center for Neuromorphic Engineering, Korea Institute of Science and Technology (KIST), Seoul 02792, Republic of Korea

<sup>2</sup>Department of Materials Science & Engineering, Seoul National University, Seoul 08826, Republic of Korea

<sup>3</sup>Department of System Semiconductor Engineering, Yonsei University, Seoul 03722, Republic of Korea

<sup>4</sup>Department of Materials Science and Engineering, Yonsei University, Seoul 03722, Republic of Korea

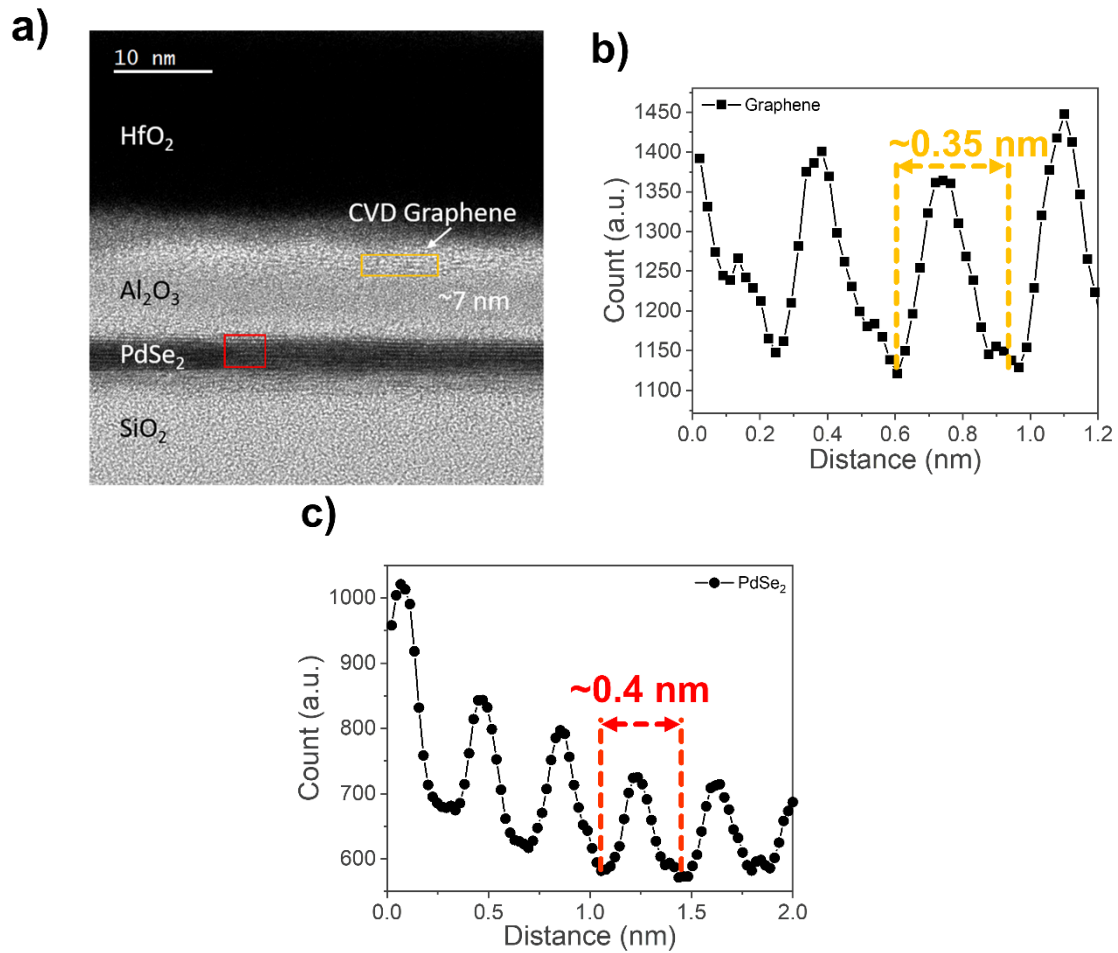
<sup>5</sup>Nanophotonics Research Center, Korea Institute of Science and Technology (KIST), Seoul 02792, Republic of Korea

<sup>6</sup>Division of Nanoscience and Technology, Korea University of Science and Technology (UST), Daejeon 34113, Republic of Korea

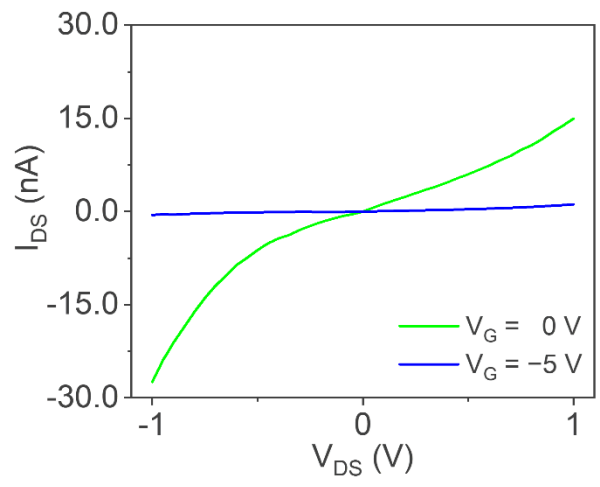
\*Correspondence to: [jiwonchang@yonsei.ac.kr](mailto:jiwonchang@yonsei.ac.kr), [jykwak@kist.re.kr](mailto:jykwak@kist.re.kr)

‡These authors contributed equally to this work.

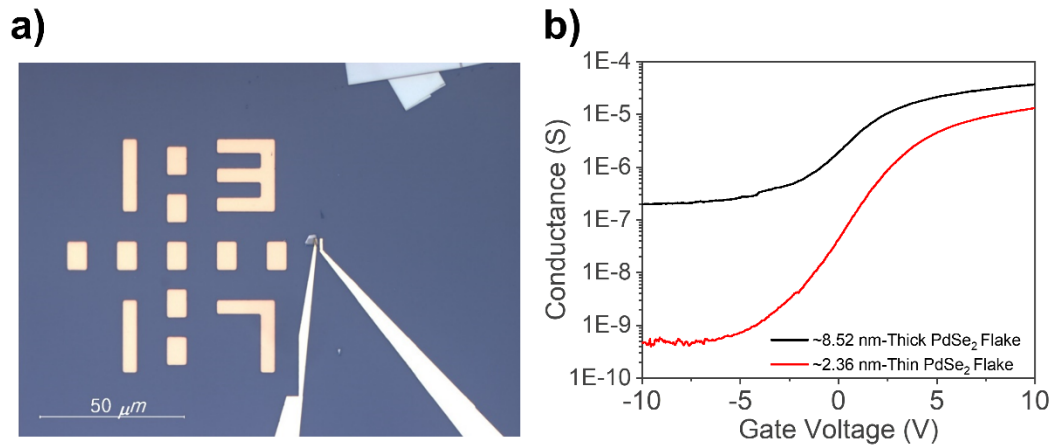
## **Supporting Information**



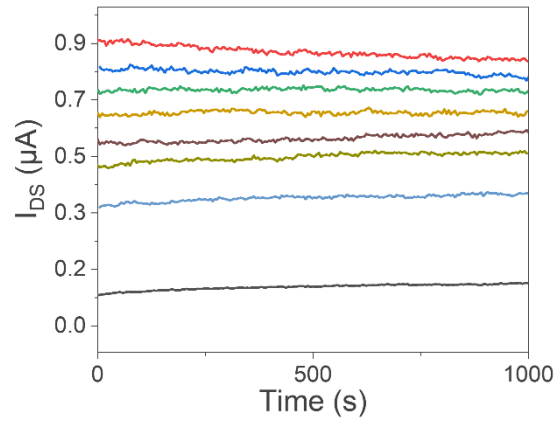
**Figure S1.** TEM cross-section view with intensity profile of graphene and PdSe<sub>2</sub>. a) TEM cross-section view image of floating gate memory based on PdSe<sub>2</sub>. b) The intensity line profile of graphene across the yellow boxed area in Fig. S1a. This shows the layer spacing around 0.35 nm.<sup>1</sup> c) The graph of intensity line profile in red boxed area in Fig. S1a. This presents the PdSe<sub>2</sub> have the interplanar spacing around 0.4 nm.<sup>2</sup>



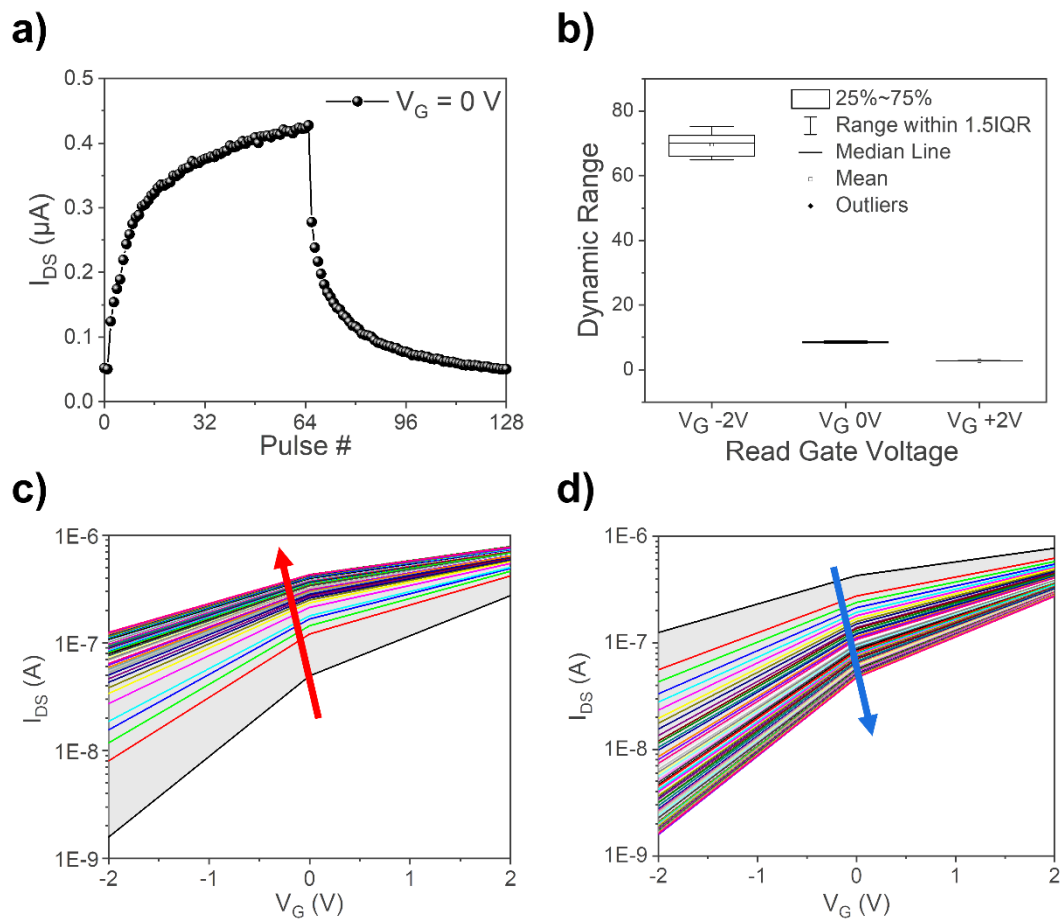
**Figure S2.** The expanded output curves of Fig. 2a at gate voltages of 0 V and -5 V, respectively.



**Figure S3.** Transfer curves of the fabricated devices with the thin (2.36 nm) and the thick (8.52 nm) PdSe<sub>2</sub> flakes, respectively. (a) Optical microscope image of the thick PdSe<sub>2</sub> flake before fabricated floating gate memory. (b) Transfer curves of floating gate memory. Black line represents the transfer curve of the thick PdSe<sub>2</sub> devices which has smaller On/Off ratio and higher off conductance than floating gate memory based on the thin PdSe<sub>2</sub> flake (red line). This result indicates that the thin PdSe<sub>2</sub> is a proper selection to fabricate the floating gate memory.



**Figure S4.** Retention characteristics during  $10^3$  s are demonstrated at PdSe<sub>2</sub> based floating gate memory. The drain currents are measured at 0 V of  $V_G$  with 1 V of  $V_{DS}$ . Three bits of states are well isolated, indicating the potential usage of PdSe<sub>2</sub> floating gate memory for multi-bit memory devices.



**Figure S5.** Dynamic range study with various gate voltages. a) A PD curve of PdSe<sub>2</sub> based floating gate memory with +13 V, 1 ms pulses. Drain-source currents ( $I_{DS}$ ) are measured at  $V_G = 0\text{ V}$  with  $V_{DS} = 1\text{ V}$ . b) Boxplot of dynamic ranges at three different  $V_G$ . 10 times of dynamic ranges were measured at each  $V_G$ . c, d) Measured  $I_{DS}$  at different  $V_G$  during weight potentiation and depression processes, respectively.

## REFERENCES

1. K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva and A. A. Firsov, *Science*, 2004, **306**, 666-669.
2. A. D. Oyedele, S. Yang, L. Liang, A. A. Puretzky, K. Wang, J. Zhang, P. Yu, P. R. Pudasaini, A. W. Ghosh, Z. Liu, C. M. Rouleau, B. G. Sumpter, M. F. Chisholm, W. Zhou, P. D. Rack, D. B. Geohegan and K. Xiao, *J. Am. Chem. Soc.*, 2017, **139**, 14090-14097.