Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.

Threshold Switching in Chalcogenide GeTe and GeTeS Thin Films Prepared via Plasma Enhanced Atomic Layer Deposition

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Supplementary information 1. ALD process development of Ge-Te, Te-Te, and Ge-S sub-cycles

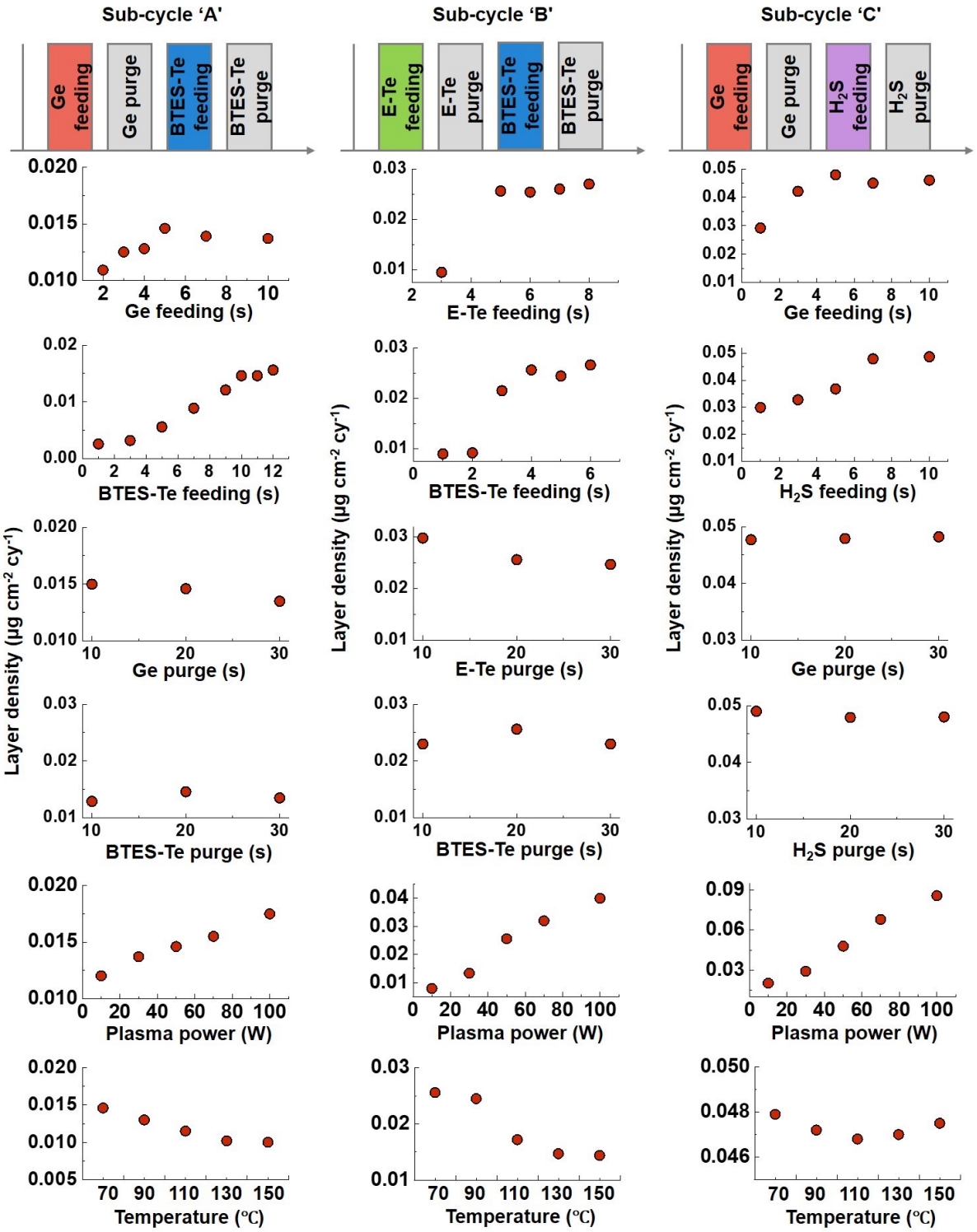

Figure S1. From the left to the right vertical panel, the detailed ALD process developments of Ge-Te, Te-Te, and Ge-S sub-cycles are shown. In each ALD process development, the ALD

windows (self-regulation region in the thickness or layer density) were confirmed by varying the precursor feeding and purging time. These ALD sub-cycles were used as a unit cycle in the ALD super-cycle for the GT and GTS thin films. The temperaure- and RF plasma power-dependent deposition behaviors are shown in the last two panels each.

Supplementary information 2. The AFM and XRD analyses results of the GT and GTS thin films

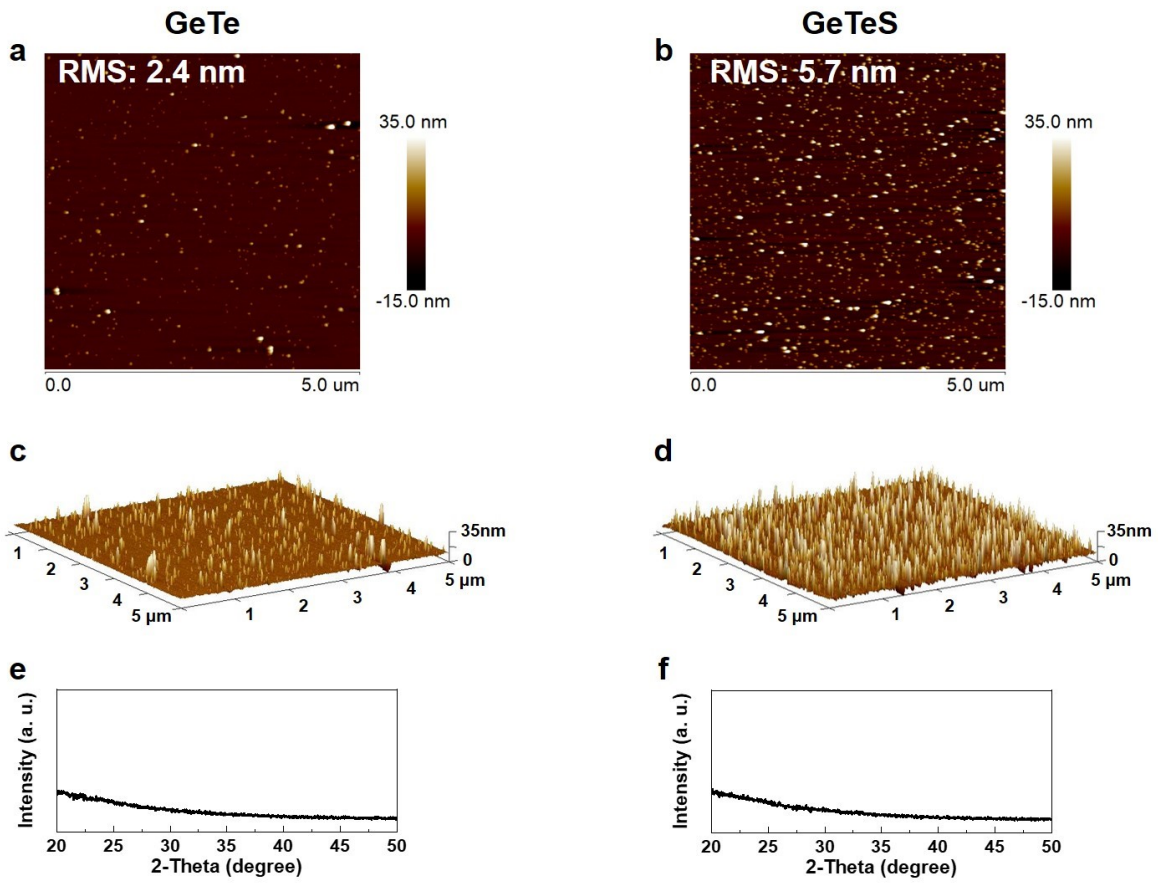

Figure S2. From the AFM analysis, the GT and GTS thin films showed the roughness values of 2.4 and 5.7 nm, respectively, which are larger values than that of bare substrate SiO_2 (0.168nm). As shown in Figures S2a, c and b, d although there are some protrusions (unknown composition) on the surface of the GT and GTS thin films, considering the thickness of each thin film is ~ 25 nm, it exhibits the endurable surface roughness of 9.6 and 22.8%. However, the additional optimization of thin film deposition process should be developed to achieve highly conformal thin film surface roughness.

The XRD analysis showed the amorphous nature of the GT and GTS thin films as shown in Figures S2e and f. As reported by the previous reports, the chalcogenide-based TS device has

an amorphous characteristic when it shows reliable electrical performance.[1] Similarly, we confirmed that our GT and GTS thin films have an amorphous characteristic in as-deposited state.

Supplementary information 3. A comparative test of Pt thin film for use as TE material in the GT-based TS device

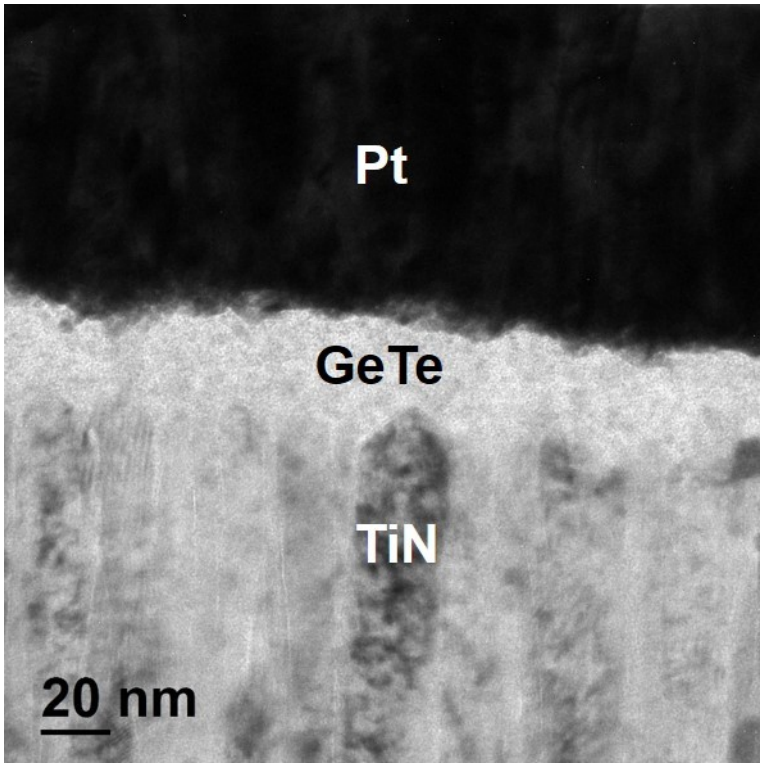

Figure S3. cross-sectional view of Pt TE / GT / TiN BE structured sample. This test was performed to confirm the reason for the interface layer formation between the TiN TE and GT (or GTS) from a material viewpoint. The GT layer does not form an interface layer with the Pt TE, whereas the TiN TE forms an interface layer with the GT and GTS layers. However, because the BEs of the TS devices also comprise a TiN layer, the reason for the formation of the interface layer could not be simply explained from the material viewpoint. It was expected that the atmospheric circumstances could affect its formation.

Supplementary information 4. Device-to-device electrical characteristic confirmation of the GT- and GTS-based TS devices

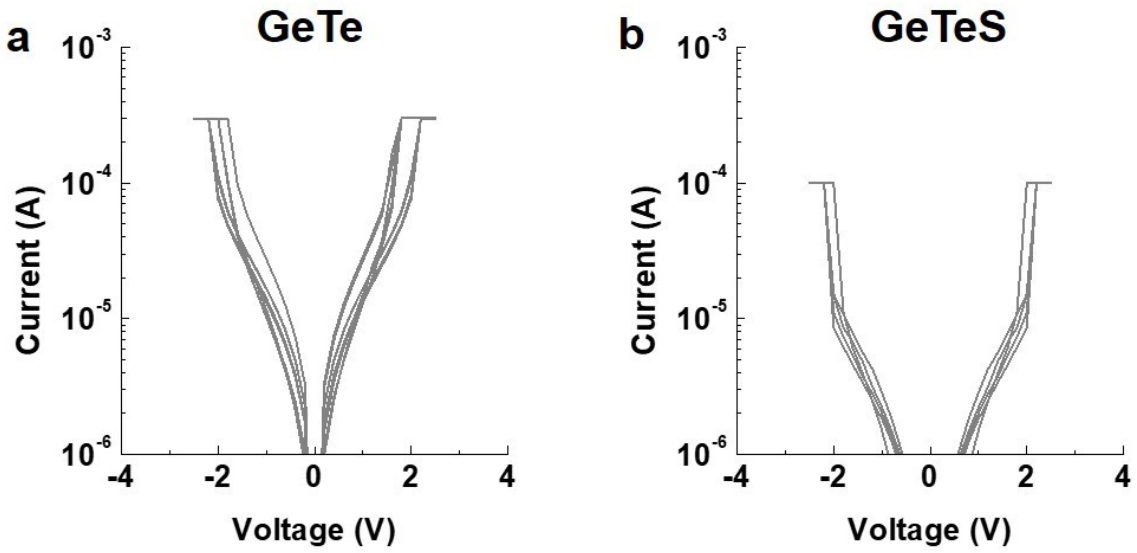

Figure S4. a and b show the DC I-V curves of 10 cycles of the GT- and GTS-based TS devices.

References

1 H. K. Seo, J. J. Ryu, S. Y. Lee, M. Park, S.-G. Park, W. Song, G. H. Kim, M. K, Yang, *Adv. Elec. Mat.*, 2022, **8**, 2200161.