

Supplementary material

Low-toxicity Chemical Solution Deposition of Ferroelectric Ca:HfO₂

Miguel Badillo,^{a,b} Sepide Taleb,^a Taraneh Mokabber,^a Jan Rieck,^b Rebeca Castanedo,^c Gerardo Torres,^c Beatriz Noheda,^{*b} and Monica Acuautla^{*a}

^a Engineering and Technology Institute Groningen (ENTEG), Faculty of Science and Engineering, University of Groningen, Nijenborgh 4, Groningen 9747AG, The Netherlands.

^b Zernike Institute for Advanced Materials (ZIAM), Faculty of Science and Engineering, University of Groningen, Nijenborgh 4, Groningen 9747AG, The Netherlands.

^c Centro de Investigación y de Estudios Avanzados del I.P.N. (CINVESTAV), Unidad Querétaro, 76230, Querétaro, México.

*m.i.acuautla.meneses@rug.nl

*b.noheda@rug.nl

1 Preparation of platinized silicon wafers

In our work, we found that the quality of the platinized substrate was crucial for successfully achieving ferroelectric thin film capacitors. Therefore, we prepared, cut, and cleaned our own substrates.

1.1 Preparation of wafer

Whole, 2" silicon wafers of (100) orientation were purchased from Siltronic. The wafers had a structure of SiO₂/Si with 90 nm/500 μm thickness. Resistivity of Si was > 200 Ω·cm. To discard any contamination with organic matter after opening of wafer bag seal, each wafer was cleaned before metallization. A UV/ozone treatment was applied for 5 minutes. Then the wafer was submerged in a pure, hot acetone bath at 45 °C for 5 minutes, followed by a pure, hot isopropanol bath at 45 °C for another 5 minutes. The wafer was immediately rinsed with pure isopropanol at room temperature and dried with dry-air pistol. Deposition of metals was done within the next hour. Prior cleaning of the wafers is unnecessary when they have been stored in sealed conditions.

1.2 Metallization and annealing of wafer

The whole wafer was coated first with 5 nm Ti layer (for adhesion), followed by 100 nm Pt layer. Both metals were deposited sequentially by e-beam machine (TEMESCAL FC2000) at pressure below 2×10⁻⁶ Torr in the NanoLab facilities at the University of Groningen. Ti was deposited at 0.1 nm/s. Pt was deposited at 0.1 nm/s until a thickness of 10 nm, and then at a rate of 0.2 nm/s to achieve a 100 nm layer. To ensure conformity and good adhesion of the layers, the whole stack was annealed in a furnace under air atmosphere for 1 hour at 400-450 °C. The temperature was raised from normal conditions at a rate of 3.7 °C/min. To achieve a well-adhered, but also uniform bottom electrode, the control of the annealing temperature is very important. Above 450 °C there is a risk for the metal layer to become rough and develop protruding Pt islands, which is detrimental for dielectric thin films. AFM imaging of the annealed Pt/Ti/SiO₂/Si wafer is recommended before further processing.

1.3 Cutting, cleaning and storage of small substrates

To obtain 8×8 mm square substrates, the metallized wafer needs to be diced. However, due to cutting, the surface runs the risk of becoming heavily contaminated with small particles. Therefore, previous to dicing, the wafer was protected with AZ 5014 E photoresist deposited by spin-coating at 4000 rpm for 60 s. The photoresist was immediately baked at 100 °C for 50 s. The wafer is then sliced into small squares. The photoresist can be exposed to normal light conditions. The substrates are then put in a glass beaker containing deionized water and ultrasonicated for 5 minutes. This helps to remove some of the debris from the cutting step. The substrates are rinsed with clean water for several times and only a minimum amount is left in the beaker. Separately, a soapy solution is prepared by perfectly dissolving a measured amount of Alconox detergent in deionized water (following the instructions from the manufacturer). The soap solution is added to the beaker with the substrates and ultrasonication is applied for 2-3 minutes. The substrates are rinsed again with deionized water several times. The Alconox soap is capable of slow etching of the photoresist layer. This helps to remove some of the small debris adhered to the substrates during cutting. To remove the photoresist layer, the substrates are submerged for a few seconds in acetone and then moved to another clean acetone bath. The second acetone bath can be heated at 45 °C for a few minutes to ensure the total removal of the photoresist. After a brief rinse with pure isopropanol, the substrates can be stored in isopropanol until deposition. However, in our case, we pursued a final RCA cleaning step. After rinsing in water several times to get rid of organic solvents, the substrates are put in a clean beaker with 5 volume parts of water. One part of ammonia solution (around 25 % purity) is added and the mixture is heated to 75 °C on a hot plate. Once hot, one part of H₂O₂ solution (around 30 % purity) is poured in and the temperature is recovered to 70-75 °C. About a minute later, the substrates are submerged in the mixture. Immediate, intense bubbling of the Pt surfaces follows. The temperature is kept for around 10-15 minutes. Then the substrates are removed, rinsed with deionized water, rinsed after with pure isopropanol and finally stored in hermetic glass containers with isopropanol. This way, the substrates can be kept clean for several weeks. Just before their use, the substrates are rinsed once more with isopropanol and dried with dry-air or nitrogen. Most likely, not all of the above procedures are needed, but they have helped us to achieve good ferroelectric, low leakage capacitors.

2 Rapid thermal annealing processing

The annealing process, depicted in Fig. S 1, has been divided into 5 steps: 1) Heat ramp (1.39 °C/s) to pre-conditioning of the samples. 2) Conditioning of the samples at 150 °C for 5 minutes. The idea behind is to prepare the samples and the RTA system for rapid response to temperature change. 3) Rapid heat ramp to achieve high annealing temperature. 4) Holding time of the annealing temperature. 5) Natural cool down of the system and the samples.

In Fig. S 1 all steps, except step 5, are tightly controlled. The rate of step 5 depends on the natural cool down of the system, which in turn depends on the temperature and the holding time. It would be interesting to study the effect of controlled cool down of the samples, as well as the control of the gas atmosphere at different steps during the thermal processing.

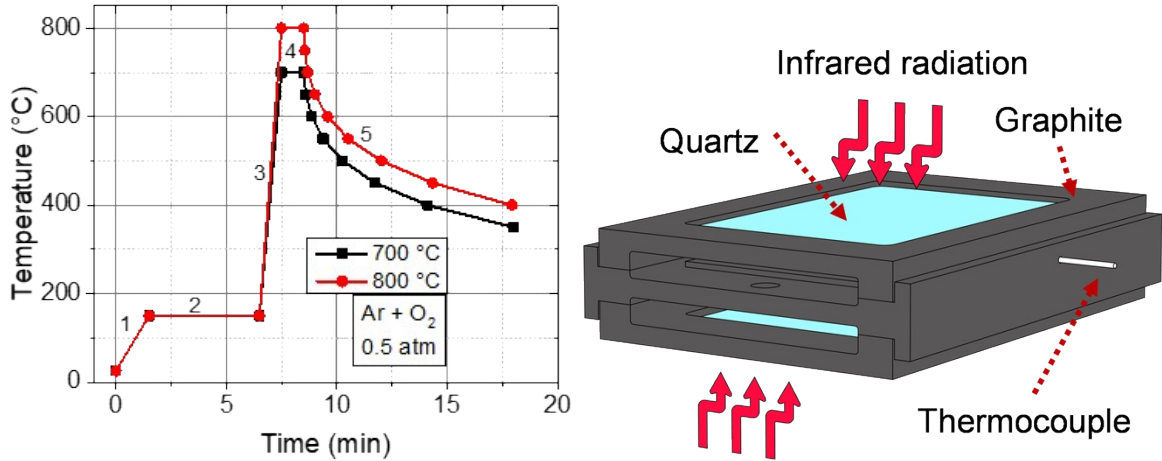


Fig. S 1: Typical rapid thermal annealing ramp procedure for the Ca:HfO₂ films and compact view of the RTA annealing device.

3 Leaky HfO₂ ferroelectrics

In Fig. S 2, the fatigued responses of 54 nm thick Ca:HfO₂ films annealed at 700 °C for 90 s (a and b), and annealed at 800 °C for 60 s are shown (c and d). The scales have been modified to show the effects in larger detail. For the film annealed at 700 °C for 90 s, the initially narrow polarization loop opens up with field cycling (Fig. S 2 a). The transient current plot, Fig. S 2 b), shows that the opening is due to both, small switching currents of the ferroelectric and leakage currents at fields above 1 MV/cm. If leakage is not disregarded, an apparent P_r of 8 $\mu\text{C}/\text{cm}^2$ is found for the film at 4.0×10^5 cycles. However, it is evident that the true ferroelectric response is minimal. This film in particular can be thought of as a mostly dielectric layer with a leaky behavior. The situation becomes a bit more complicated for the 54 nm Ca:HfO₂ films annealed at 800 °C for 60 s. In Fig. S 2 b), the initial polarization loop is open, and its shape resembles more that of a ferroelectric material. Indeed, the current-electric field graph shows relatively strong switching peaks at 10^4 cycles. Nevertheless, the polarization loop opens up even more and it seems to increase for 1.5×10^5 and 4.0×10^5 cycles. In some papers, these types of unsaturated polarization loops are mistakenly regarded as evidence of high ferroelectricity in HfO₂ based films. However, when attention is drawn to the current-electric field loops (Fig. S 2 d), it is found that the switching currents are actually weaker, and that leakage is relatively significant. For our Ca:HfO₂ films, leakage is relatively small, but it still causes the value of P_r to increase artificially. What is more, in some papers the current plots are not shown, and polarization figures are taken as the unique evidence for ferroelectricity. If leakage in the film is high, then high P_r values are obtained, but the values cannot be entirely trusted. Therefore, polarization and currents plots should be included in the papers. Else, leakage compensation methods must be adopted. At least for chemical solution deposition methods, high leakage can come from undecomposed organic compounds remaining in the film structure. However, this can also be associated with poor quality of the electrodes and/or poor filtration of the precursor solutions. Thus, special care is needed.

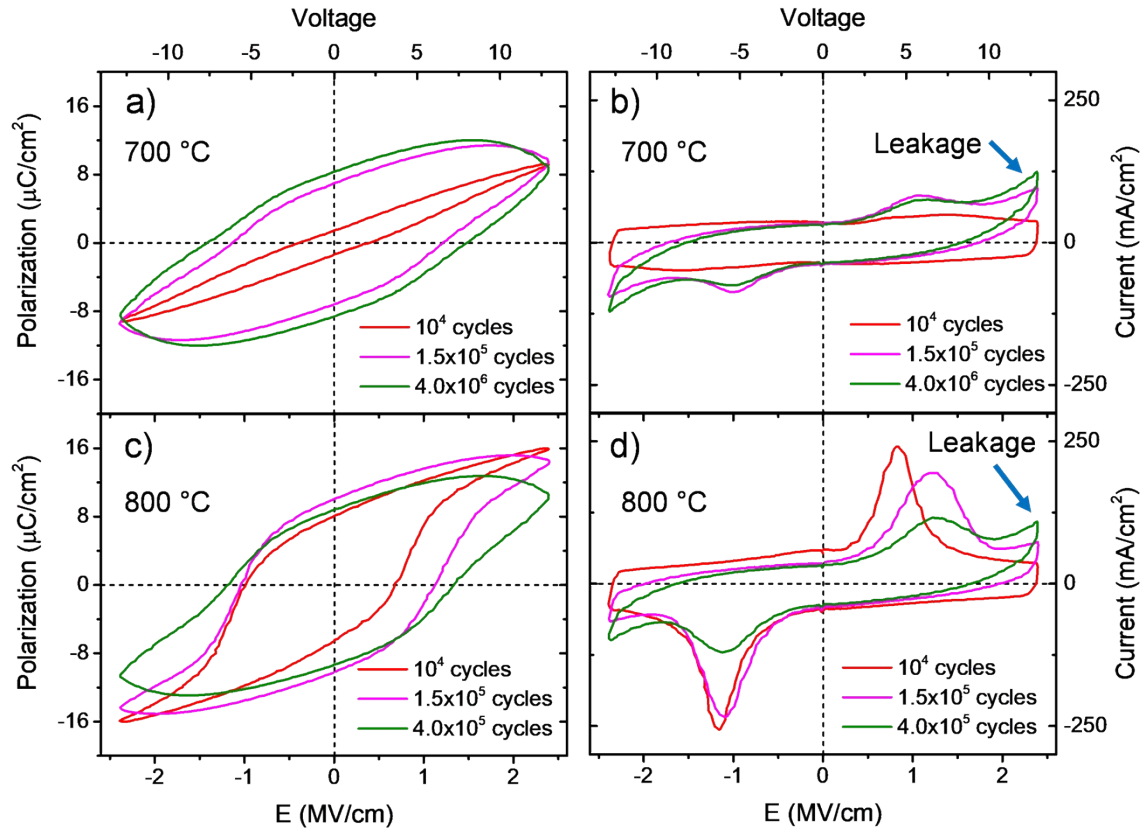


Fig. S 2: Polarization and current vs. electric field strength for 54 nm Ca:HfO₂ films annealed at 700 °C for 90 s (a and b), and 54 nm Ca:HfO₂ films annealed at 800 °C for 60 s (c and d). The films were fatigued at 1 kHz for an increasing number of cycles at 2.78 MV/cm. Top Pt electrodes with 200 μm diameter were used.