Electronic Supplementary Material (ESI) for Lab on a Chip.
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Supplementary information

Integrated membrane-free thermal flow sensor for silicon-on-glass microfluidics

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Silicon microfluidic chip technology

The fabrication starts with megasonic cleaning for particle removal of the silicon wafer. Piranha solution was used for organic contamination removal followed by 18.2 MOhm·cm deionized water rinse and drying in a nitrogen atmosphere. After cleaning, the wafer was treated with concentrated HMDS in a vacuum vapor primer at 120°C for 90 s for adhesion promotion, spin-coated with SPR220 photoresist, and soft-baked on a contact hotplate at 115°C for 90 s before laser lithography of the channel and through silicon vias. A post-exposure bake was performed on a contact hotplate at 115°C for 90 s to reduce standing wave effects and to assist the chemical reaction that occurs during the

exposure. After that, the photoresist was developed in MF-CD-26 at 21°C for 180 s. The silicon oxide mask was patterned by reactive ion etching (RIE) in a 1:2 CHF_3/Ar gas mixture at 5 mTorr gas pressure to create a 1 μm deep stair-step in the masking layer. Contaminants were removed by O_2 plasma treatment at 600 W for 2 min. The photoresist was then removed with NMP at 80°C in 30 min followed by IPA at 80°C bath and deionized water rinse (Fig. 2a, step 1).

The same lithography process was used to pattern the vias. The only difference is that the oxide mask was etched down to bare silicon using the same RIE process to form a SiO_2 masking layer for further silicon deep reactive ion etching (DRIE) (Fig. 2a, step 2). At first, 600 cycles of the DRIE process were conducted to etch the vias to a depth of 475 μm, leaving 50 μm of silicon at the bottom of the vias to be etched later. Each cycle comprised three steps: passivation polymer deposition in C_4F_8 at 20 mTorr, polymer breakthrough in SF_6 at 30 mTorr, and silicon etching in SF_6 and O_2 gas mixture at 40 mTorr (Fig. 2a, step 3). Subsequently, the oxide mask was thinned by 1 μm in the RIE process in CHF_3/Ar gas mixture so that the silicon surface became exposed for the subsequent DRIE process.

The DRIE process was the same as the aforementioned one, but the gas pressure was lowered to 20 mTorr to enhance the channel profile. The process included 160 DRIE cycles to etch a 50 μm deep channel. At this point, vias and microfluidic channels were fully etched. The remaining SiO_2 was removed with BOE at 21°C in 1 h, after that the wafer was rinsed with deionized water and dried in a nitrogen stream (Fig. 2a, steps 4-5).

Sensing elements technology

Next, the glass wafer was cleaned in a Piranha solution for removing residual organic contaminants. The glass wafer was then rinsed with deionized water and dried in a nitrogen stream. After cleaning, the glass wafer was anodically bonded to the silicon wafer from the previous step to seal the channels (Fig. 2a, step 6). Electrical circuits which include the sensing elements and heaters were fabricated using a lift-off process. As a first step, sacrificial layers of a lift-off resist LOR 5A and a positive photoresist SPR955 were spin-coated. LOR 5A was spin-coated on the glass wafer surface and soft-baked on a contact hotplate at 190°C for 300 s prior to SPR955 spin-coating.

SPR 955 was soft-baked on a contact hotplate at 100°C for 90 s. Then, an electrical circuit pattern was formed in the photoresist using laser photolithography. Post exposure bake was performed on a contact hotplate at 115°C for 90 s to reduce standing wave effects and to assist the chemical reaction that occurs during the exposure. After that, the photoresist was developed in MF-CD-26 at 21°C for 120 s. To improve surface adhesion characteristics and remove contaminants, the wafer was treated in oxygen plasma at 300 W for 240 sec. Nickel sensing elements were deposited on a patterned photoresist on the glass wafer using a 10 kW electron beam evaporator at a base pressure below 3×10–8 Torr from the nickel pellets. The films were grown at a rate of 2 Å/s measured with a quartz monitor at an approximate distance of 30 cm from the source to the substrate. The thickness was varied in the range of 80-180 nm. Following this, the sacrificial LOR5A was dissolved in a NMP solution at 80°C in 3 h. The remaining metal particles were removed with isopropyl alcohol using a 2-step 80 kHz ultrasonic bath process. The steps lasted 2 min and 1 min, respectively, and 30% ultrasonic power was used. The wafer was then dried in a nitrogen stream (Fig. 2a, steps 7-8).

Furthermore, to passivate the electrical circuits, the same lithography step sequence was performed, but the contact pads were covered with the resist layers. The silicon dioxide passivation layer was deposited by electron beam evaporation, as described for the nickel process. The film was grown at a rate of 5 Å/s with a thickness of 350 nm. The sacrificial resist layer was dissolved in NMP solution (the same cleaning process was repeated) (Fig. 2a, steps 9-10).

As the final step of fabrication, the wafer was diced into chips with the use of SPR220 as a protective layer. The resist and other contaminants from each chip were removed using an ultrasonic bath with ethyl lactate solution, IPA, and deionized water consequently. Then, all MTFS chips were dried in a nitrogen stream. The electronic interface between the chip and the PCB was organized using Al/Si wire bonding. For chip-fluid interface formation, the microfluidic chip was sandwiched between two parts of the manifold using seal rings for tightness (Fig. 2a, steps 11-12).

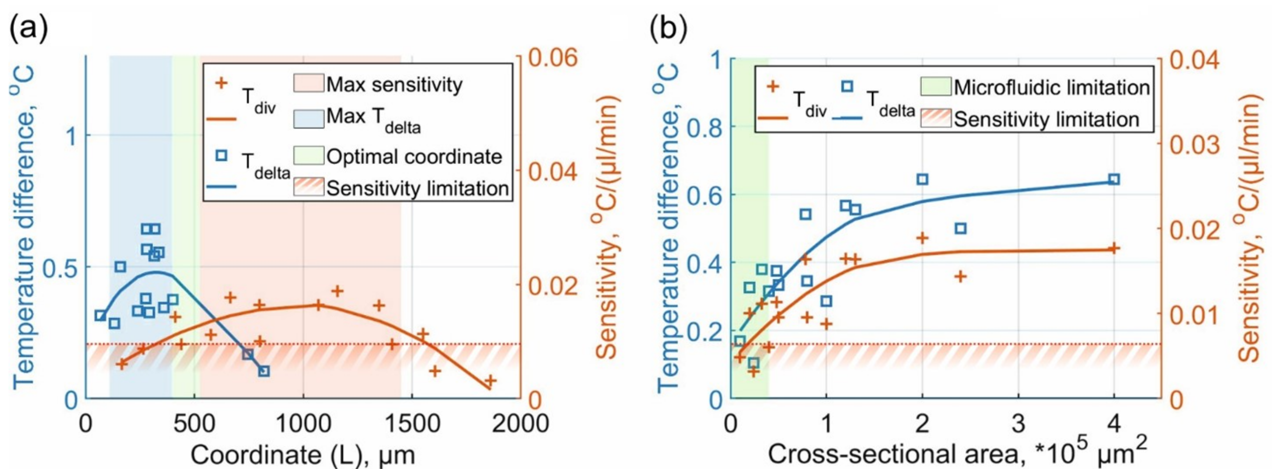

Figure S1 – simulation results for MTFS with 150 µm thick glass wafer: graphs of the temperature difference between the upstream and downstream calorimetric sensors and the sensitivity of the MTFS, (a) determining the coordinate **L** of the calorimetric sensors; (f) determining the channel dimensions to meet both «microfluidic» and «sensitivity» limitations.

Table S1 – Simulation full parameter list

Parameter	Value	Description
chip_x	10 [mm]	chip length
chip_y	5 [mm]	chip width
si_z	525 [µm]	silicon thickness
gl_z	100/150 [µm]	glass thickness (variable)
ch_y	200/400/650/1000/2000 [µm]	channel width (variable)
ch_z	50/120/200 [µm]	channel depth (variable)
h_x	40 [µm]	heater length
h_y	220 [µm]	heater width
dt	20 [K]	heating the heater
K	1 [W/(m^2*K)]	thermal conductivity
flow	1/8/17/33/50/67/84 [µl/min]	water flow (variable)

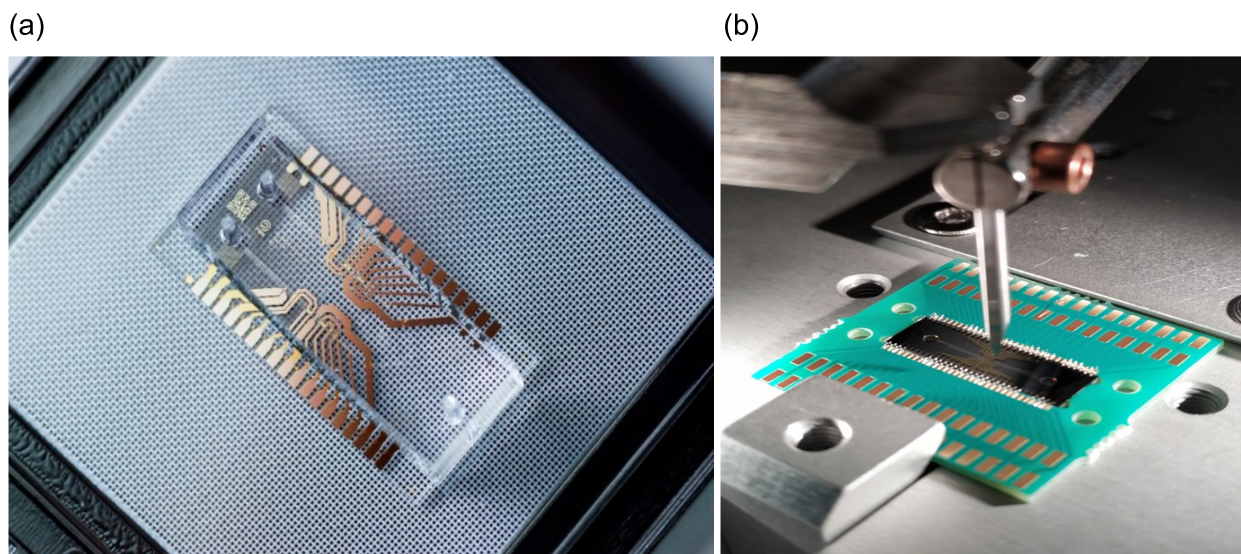

Figure S2 – (a) dilution chip with two independent MTFSs; (b) LOC-integrated MTFS during wire bonding process.

Table S2 - Comparison of MTFS with leading commercial sensors

	Reference thermal FS	**Reference Coriolis FS**	**Experimental MTFS**
Range, µl/min	2-80	0-66.7	2-30
Accuracy, % of MV	5	0.2	5
Near zero accuracy, µl/min	< 2.4	< 0.2	< 0.4
Internal volume, µl	5	13	0.07
Response time T1, s:	1.15	0.40	1.05

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from F_{min} to 90% F_{max}			
Response time T2, s: from F_{max} to 10% F_{min}	0.85	0.32	0.75

The developed MTFS has been tested at various working temperatures in the range of 22-28 ˚C. We recorded the reference flow rate (F), MTFS signal (S), resistance of the additional on-chip temperature sensor (R), and interpolated 3D data with a calibration surface. The whole experiment consisted of 8 slow stepped passes and took more than 6 hours of continuous operation. As seen in Fig. S3a, the ambient temperature does affect the measured signal, but the absolute error (Abs, µL/min) caused by this effect can be minimized by calibrating the sensor with a 3D surface, taking into account the resistance Rref of the additional on-chip thermal sensor, as it correlates well with the ambient temperature (Fig. S3bc).

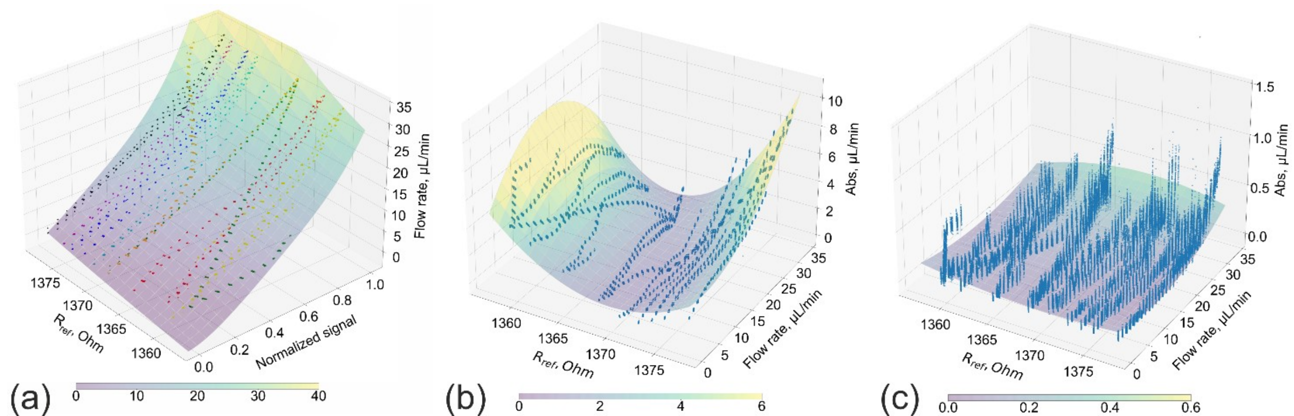

Fig. S3 (a) experimental data interpolated with calibration surface; (b) absolute error without taking into account reference sensor resistance; (c) absolute error for 3D calibration surface.