Electronic Supplementary Material (ESI) for Materials Horizons.

Supporting Information

Achieving reinforcement learning in three-active-terminal neuromorphic device based on 2D vdW ferroelectric material

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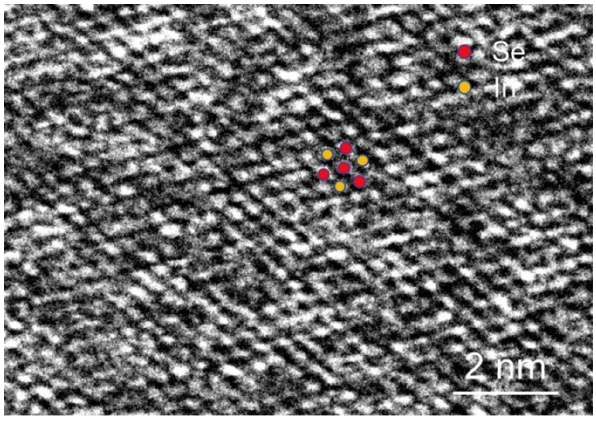


Figure S1. Top-view high-resolution TEM of the α-In_2Se_3 nanosheet with 3R structure in this work, which shows its hexagonal symmetry.

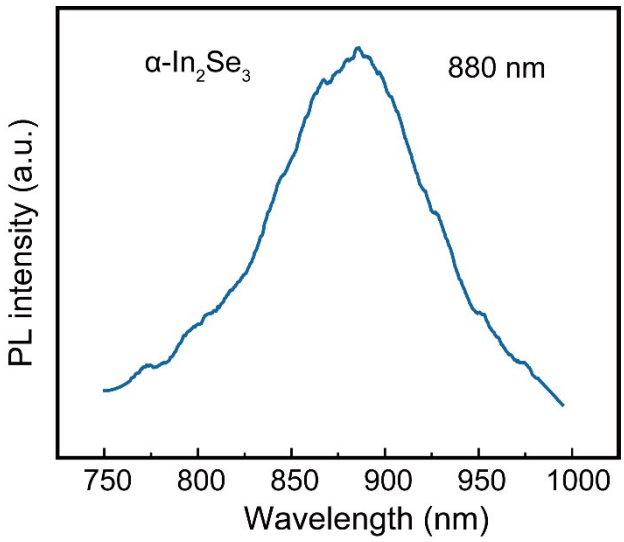


Figure S2. PL spectra of α-In_2Se_3 nanosheet on Si/SiO_2 substrate under 532 nm laser are measured. The peak location of 880 nm indicates the semiconductor nature of the material.

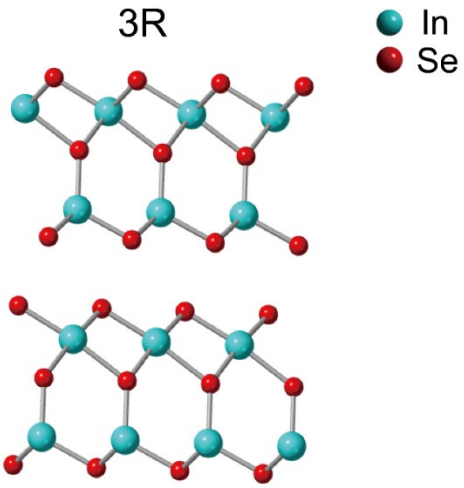


Figure S3. The crystal structure of α-In_2Se_3 with rhombohedral (3R) stacking mode. The ferroelectricity can be attributed to the central Se atom's lateral movement.

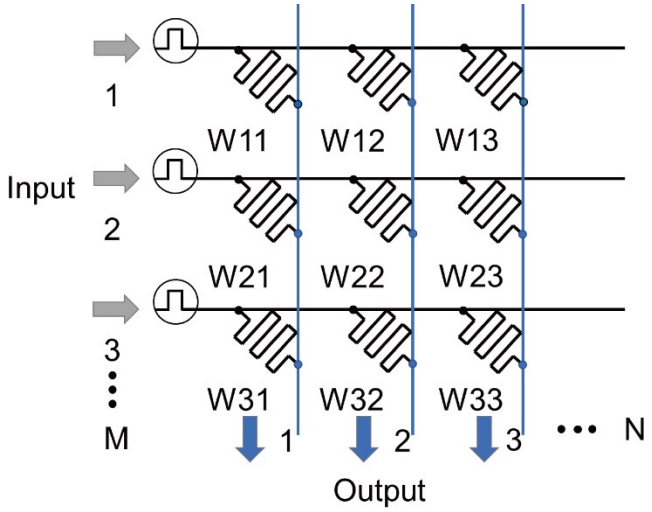


Figure S4. The principle of crossbar based on our device, where the conductance of the channel is defined as the weight of the synapses.

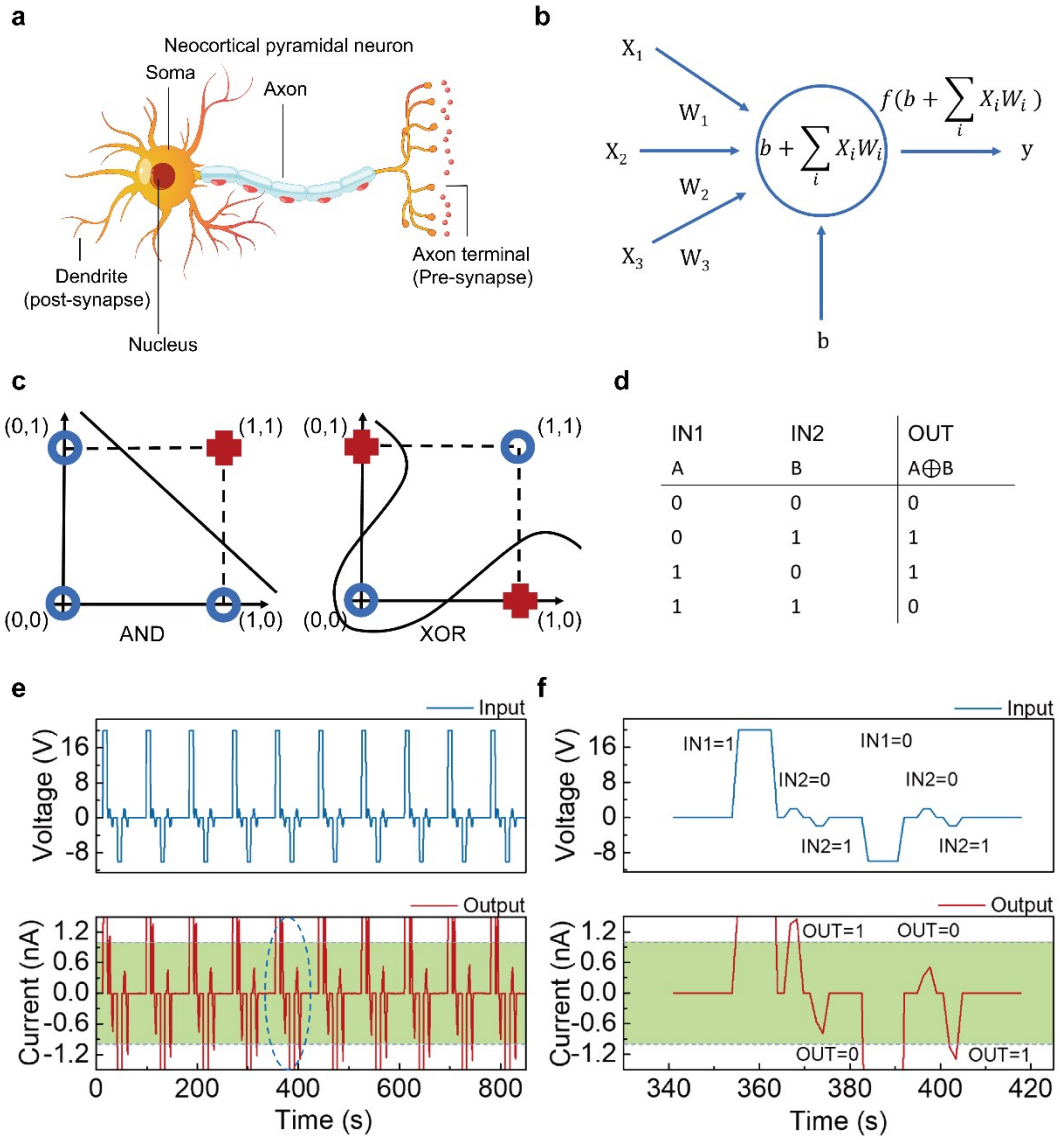
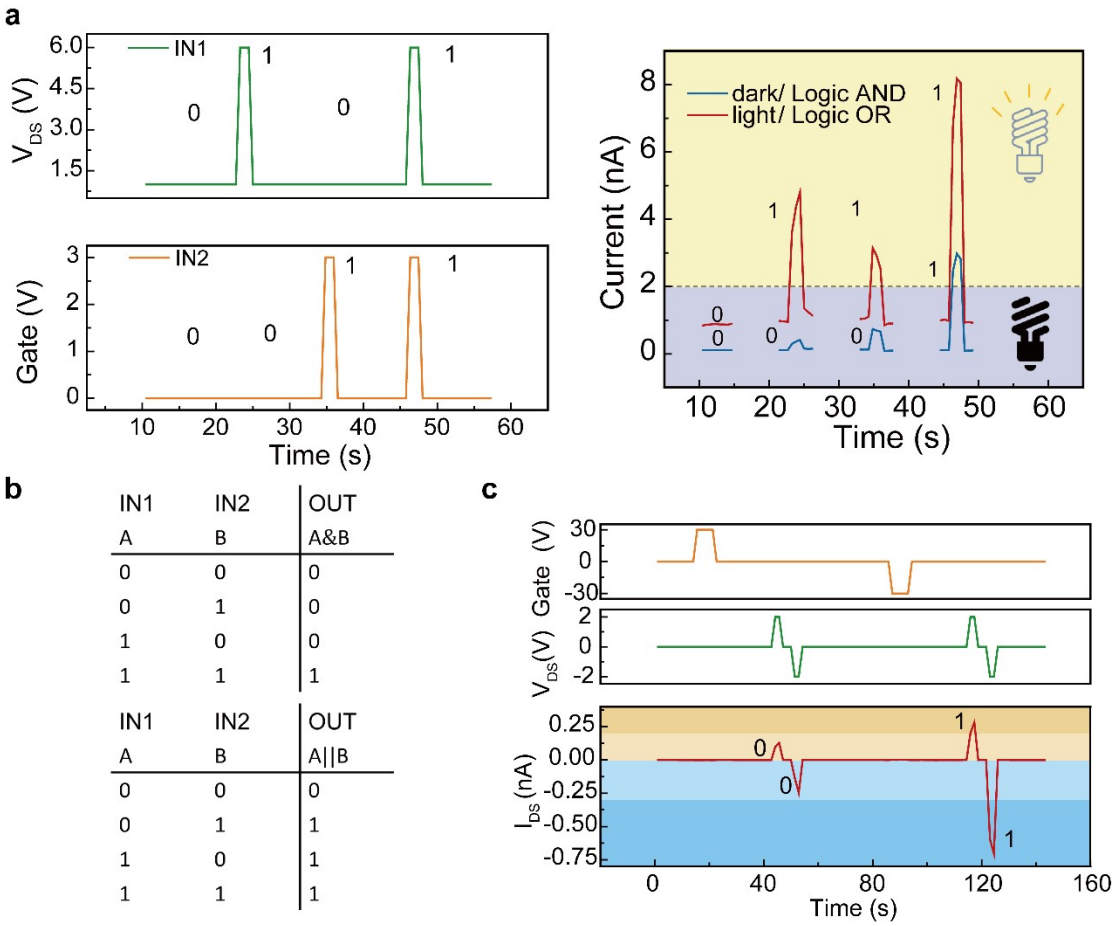


Figure S5. The XOR logic function is operated in a single artificial neuromorphic device. a) Schematic diagram of neocortical pyramidal neurons in brain. b) Perceptron's working mechanism, which shows that a single neuron can only perform linearly separable logic. c) AND logic gate is used as an example to demonstrate the linearly separable logic where a straight line can be found to separate the cross from the circle, in contrast, XOR logic (linearly nonseparable) requires a curved line. d) Truth table of XOR logic gate. e) Demonstration of 10 cycles to execute the XOR logic. In top panel, the drain voltage represents the input, and the drain current represents the output in lower panel. f) Fifth cycle is chosen as an example to demonstrate the details.



b

IN1	IN2	OUT
A	B	A&B
0	0	0
0	1	0
1	0	0
1	1	1

IN1	IN2	OUT
A	B	A||B
0	0	0
0	1	1
1	0	1
1	1	1

Figure S6. The linearly separable logics are performed including AND, OR and NOT logic gates. a) Two panels on the left represent the input IN1 and IN2. The panel on the right depicts that the device can perform OR logic under illumination, while in the dark the device is switched to AND mode. b) Truth table of AND, OR logic gate. c) Gate voltage is defined as the input and the V_{DS} is used to read the output (I_{DS}) to demonstrate the NOT logic.

Note:

Due to the additional degrees of freedom provided by ferroelectricity to modulate the device, beyond the abundant synaptic behaviors, logic functions are also implemented in our devices, as shown in the Figure S5 and Figure S6.

Figure S5a is a schematic diagram of biological neuron's structure, which consists of dendrites, nucleus, soma, axon, axon terminal, etc. For a neuron, there are two states in terms of excitation and non-excitation, which can be regarded as 0 and 1, respectively. The gap between the dendrites and the axon terminals of other neurons is called a synapse, the weight of the synapse implies the degree of impact that other neurons can impose. When signals such as neurotransmitters and electrical stimuli, are input through the dendrites, soma will respond to them in a synchronized manner. If the sum of all inputs exceeds a certain threshold, the excitatory signal will be transmitted to other neurons through the axon terminal. The artificial neuron is an analogue of its biological counterpart, which is used for supervised learning of binary classifiers, the basic principle is shown in Figure S5b. The inputs (X_i) are firstly multiplied by their associated weights (W_i), and then the multiplied values as well as the constant b are added to generate a sum, where b is considered as a bias to shifts the sum away from the origin. Finally, the activation function will map the sum value to a single binary output value (0 or 1) to mimic the states of excitation and non-excitation in biological neuron. In other words, because Equation 1 is a linear function, when the sum value is higher than a certain threshold, the artificial neuron will output 1, and vice versa 0 is output. The logic gates which are linearly separable, such as AND, OR and NOT are shown in Figure S5c, where the blue circle means output 0, the red cross means output 1, and the axes indicate inputs. Here, the AND logic gate is taken as an example, from the figure, it can be seen that the outputs 0 and 1 are separated linearly by at least one straight line in the plane. In other words, 0 is located at one side of the line and 1 is

located on the other side. However, one curved line is needed for the XOR logic gate. The truth table of XOR is shown in the Figure S5d. This means that a traditional single artificial neuron is not capable of performing XOR gate.

$$y = f(b + \sum_i X_i W_i) \quad (1)$$

The 'stateful' logic was first proposed by Stewart et al. and implemented in resistive memory based on the principle of sequential logic, where the device can both store logical values and perform logical functions. In contrast to combinational logic, the output of sequential logic not only depends on the current input, but also reflects previous input level in device, which requires several steps to perform. In order to implement the XOR function, we make use of ferroelectricity exhibited in α-In_2Se_3 and sequences of signals are applied to the source and drain electrodes of the device. The logic function needs to start from input IN1 to define the state of device, then IN2 plays the role of operating XOR logic and realizing a nondestructive read-out which is defined as OUT. Figure S5e depicts 10 repeatable cycles of executing XOR function, which demonstrate the reliability of our artificial neuromorphic transistors. As an example, the fifth cycle is selected as shown in Figure S5f. A 20 V voltage is considered as 1, while -10 V is considered as 0 for IN1. The 0 and 1 of IN2 are defined as 2 V and -2 V, respectively. Additionally, the current of IN2 is employed as an output, with a high current above the threshold (1 nA) corresponding to a "1" and a low current below the threshold corresponding to a "0". When 20 V is imposed on the device (IN1=1), the ferroelectric domain is aligned by the external electric field, the IN2=0 and 1 will lead to OUT=1 and 0, respectively. After a -10 V voltage applied, the ferroelectric polarity of α-In_2Se_3 is reversed, and the opposite output result can be obtained. The results indicate that the XOR function can be successfully performed in a single artificial

neuromorphic transistor based on 2D ferroelectric material with repeatable and reliable performance. In contrast with the conventional design based on CMOS which generally requires six devices, no doubt that our method provides a great potential to significantly reduce the size of logic circuit.

In addition to linearly nonseparable logic, linearly separable logic such as AND, OR and NOT logic gates are also implemented in our proposed device. Unlike conventional insulating oxide ferroelectric materials with wide energy band, the semiconducting nature and 1.4 eV band gap allow it to operate as the FET channel and the device's performance can be modulated by illumination. **Figure S6a** demonstrates the implementation of AND and OR logic gates, whose outputs are photoswitchable based on the combinational logic principle. Here, a 6 V and 0 V of V_{DS} is defined as 1 and 0 for IN1, respectively, while applying 3 V of gate voltage or not are considered as 1 or 0 for IN2. A 1 V bias voltage of V_{DS} is set to read output. For clearly distinguished, the AND logic function is drawn by the blue line, while the red line represents the OR logic gate. The threshold for the two types of logic mentioned above is determined as 2 nA. In dark, the AND logic function is performed, and the output of current is higher than the threshold only if both values of IN1 and IN2 are 1. Under illumination, due to the help of photogenerated carriers, only one of them inputs 1, an output value of 1 will be obtained. Compared to the case in dark, the photocurrent induced by V_{DS} is higher than that of gate voltage under illumination, which suggests the channel voltage is more favorable for separating photogenerated carriers. The truth tables of OR and AND logic are shown in Figure S6b. The Figure S6c displays the operation of NOT logic gate, where 30 V gate voltage is defined as 1, -30 V is defined as 0, and 2 V of V_{DS} is applied to read the output value. When a 1 of gate terminal is input, an output value of 0 is obtained, conversely, if a 0 is input, a 1 is obtained, thus achieving the NOT logic in

the device. It is worth noting that the equivalent function will be performed if the read voltage is set to -2 V. The implementation of the NOT logic gate can be attributed to the ability of the OOP ferroelectricity to modulate the channel conductance.