Supporting Information

Low-Power and High-Speed HfLaO-based FE-TFTs for Artificial Synapse and Reconfigurable Logic Applications

Yongkai Liu[1,2], Tianyu Wang[1,2*], Kangli Xu[1,2], Zhenhai Li[1,2], Jiajie Yu[1,2], Jialin Meng[1,2], Hao Zhu[1,2], Qingqing Sun[1,2], David Wei Zhang[1,2], and Lin Chen[1,2*]

[1]School of Microelectronics, Fudan University, Shanghai 200433, P. R. China;

[2]Zhangjiang Fudan International Innovation Center, Shanghai 201203, China;

**Email: tywang@fudan.edu.cn; linchen@fudan.edu.cn*

The supporting information file includes:

to eight devices.

Table S1. Comparison of this work with current state of artificial ferroelectric synaptic devices in terms of operating speed (Pulse Width).

Table S2. The comparison of this work with other reported devices in terms of synaptic properties.

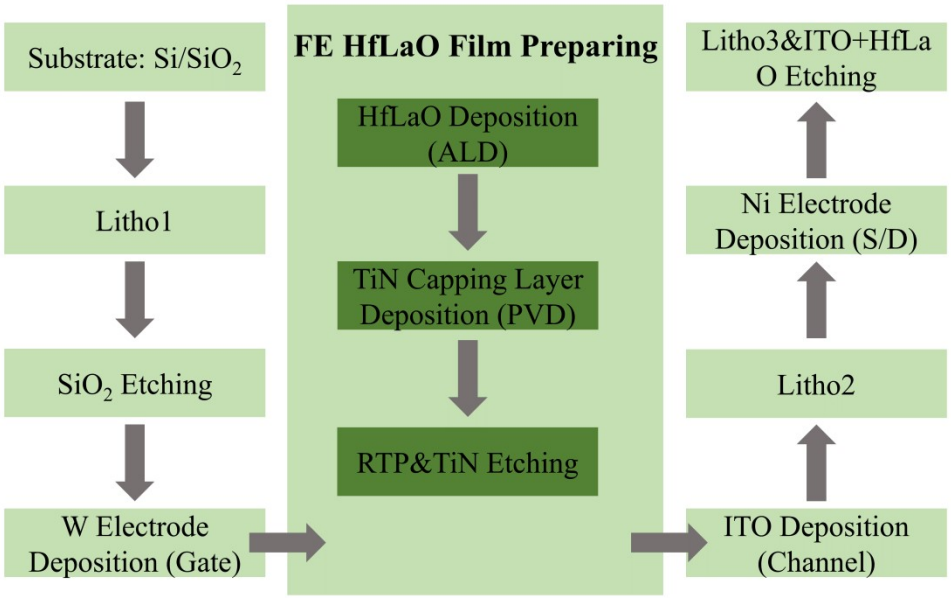

Figure S1. Fe-TFT fabrication process diagram.

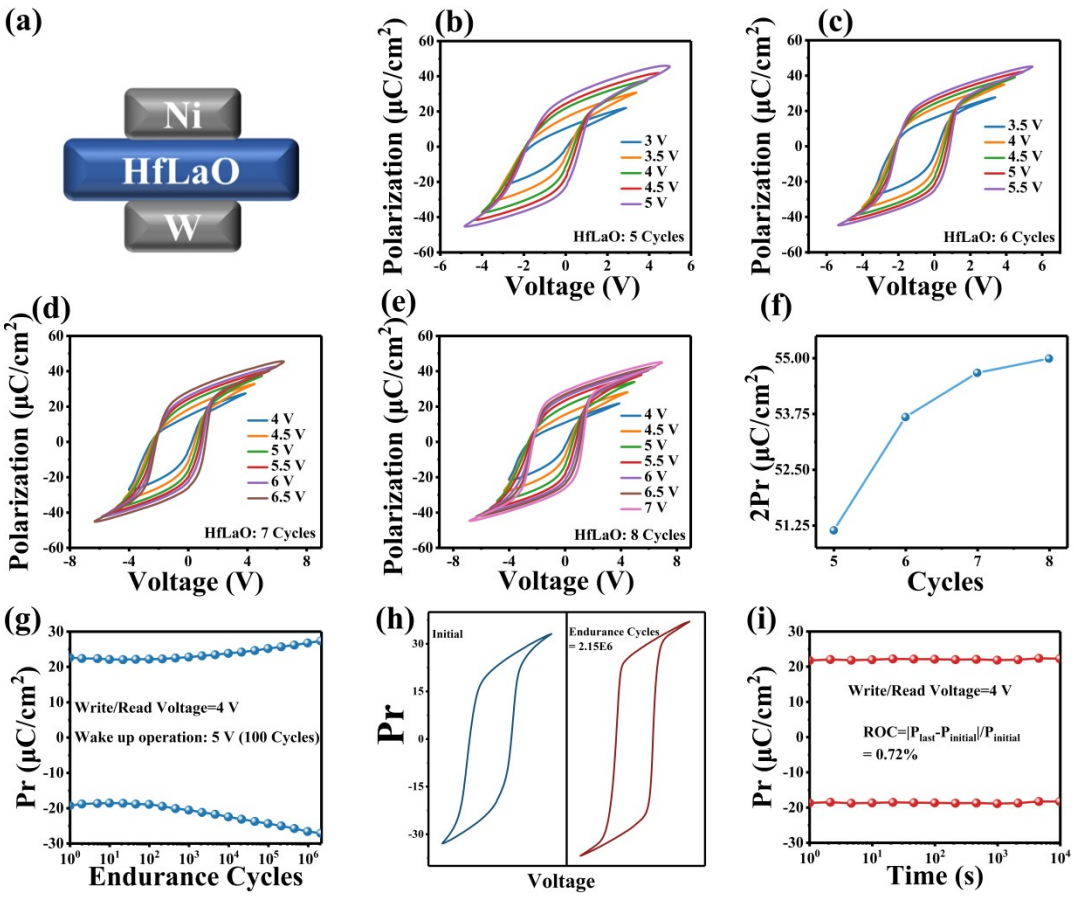

Figure S2. (a) The schematic diagram of ferroelectric capacitor device. (b)-(e) The P-E curves of HfLaO films with different ALD growth cycles. (f) Relationship between 2Pr and ALD growth cycles. (g) Endurance tests of the ferroelectric capacitor device with HfLaO films grown at 8 cycles. (h) P-V curve graphs of initial and final states extracted during endurance testing. (i) Plot of remnant polarization strength vs. retention time.

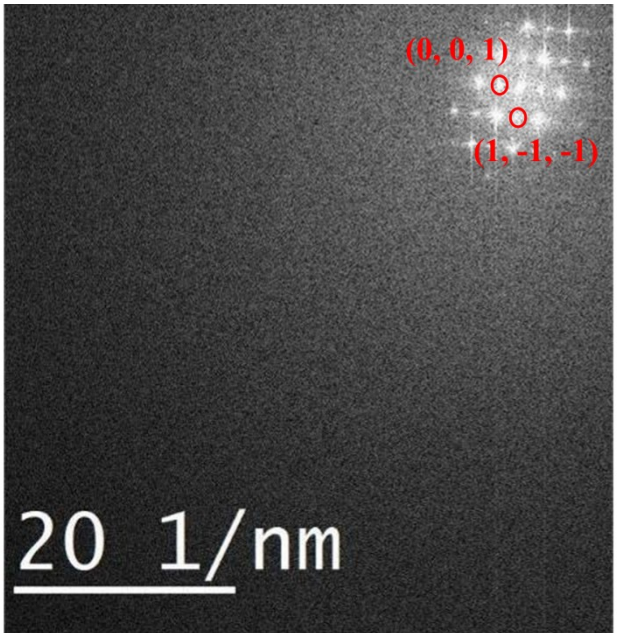

Figure S3. The fast fourier transform pattern of the HfLaO film.

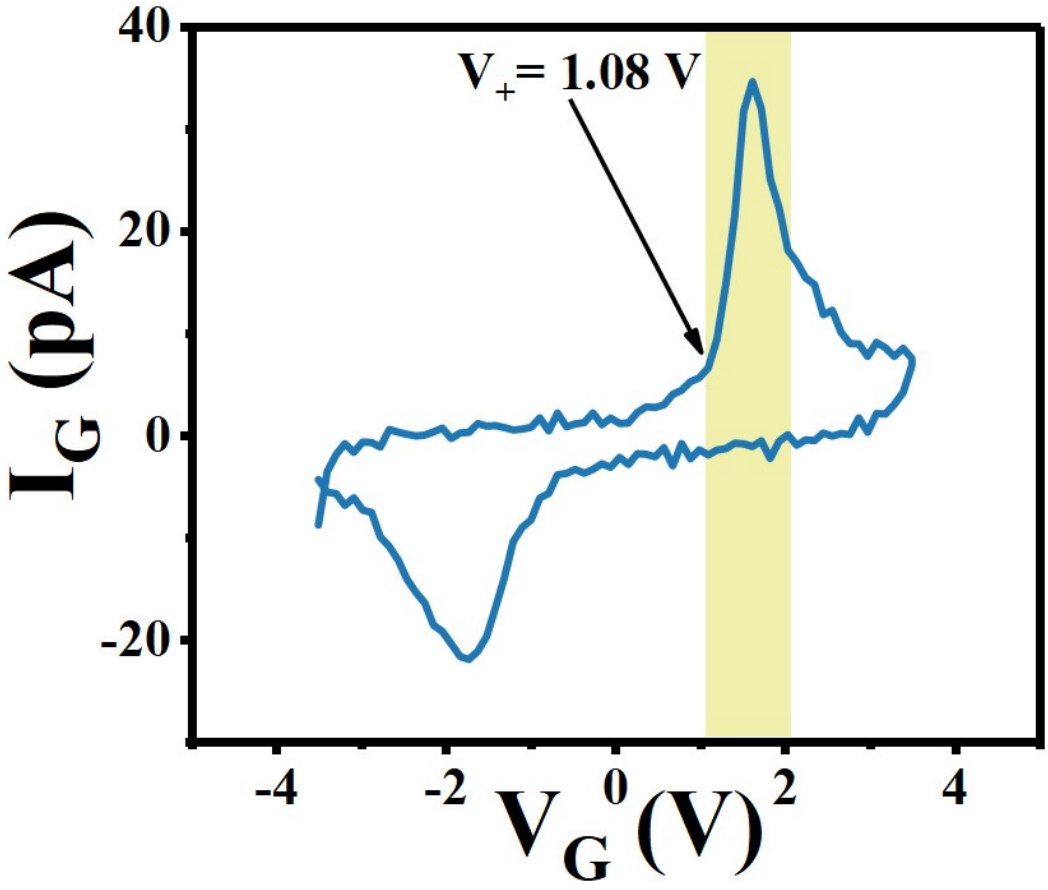

Figure S4. Relationship between I_G and V_G.

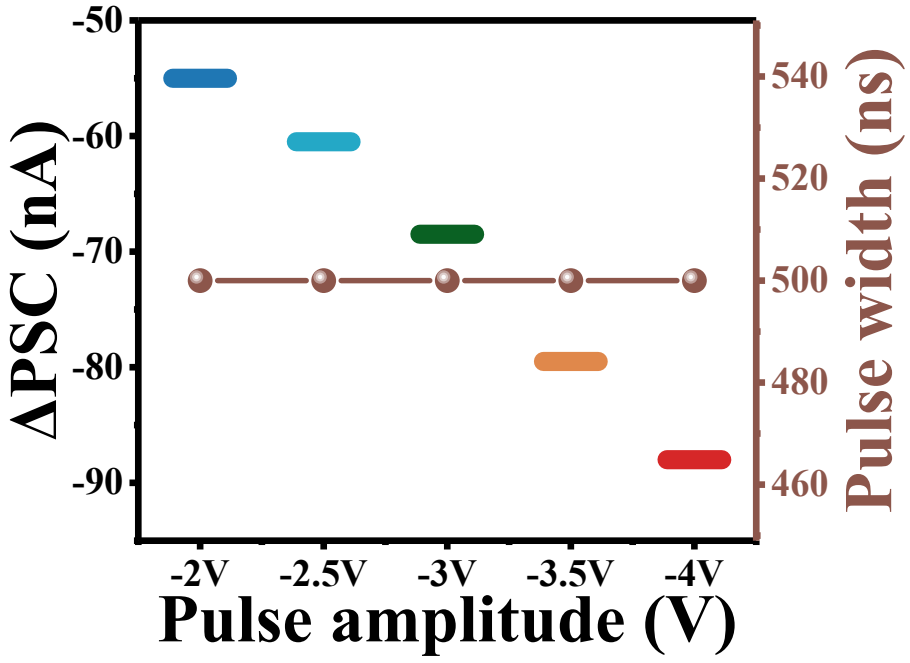

Figure S5. Plot of ΔPSC excited by gate pulses with different negative pulse amplitudes.

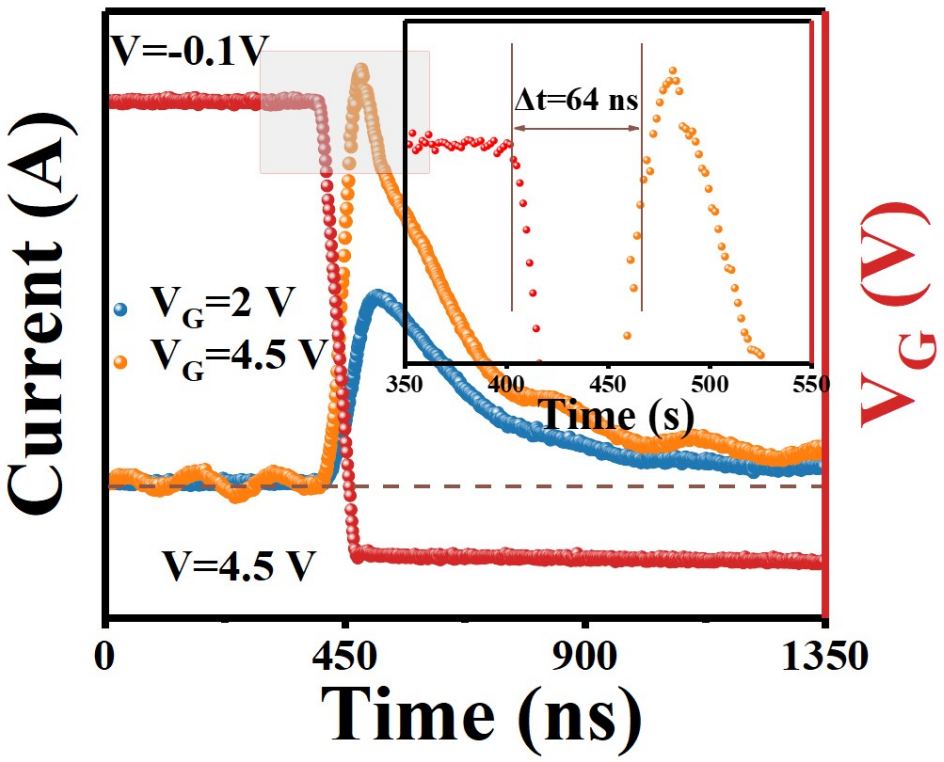

Figure S6. The current variation in the FeTFT when the pulse is applied.

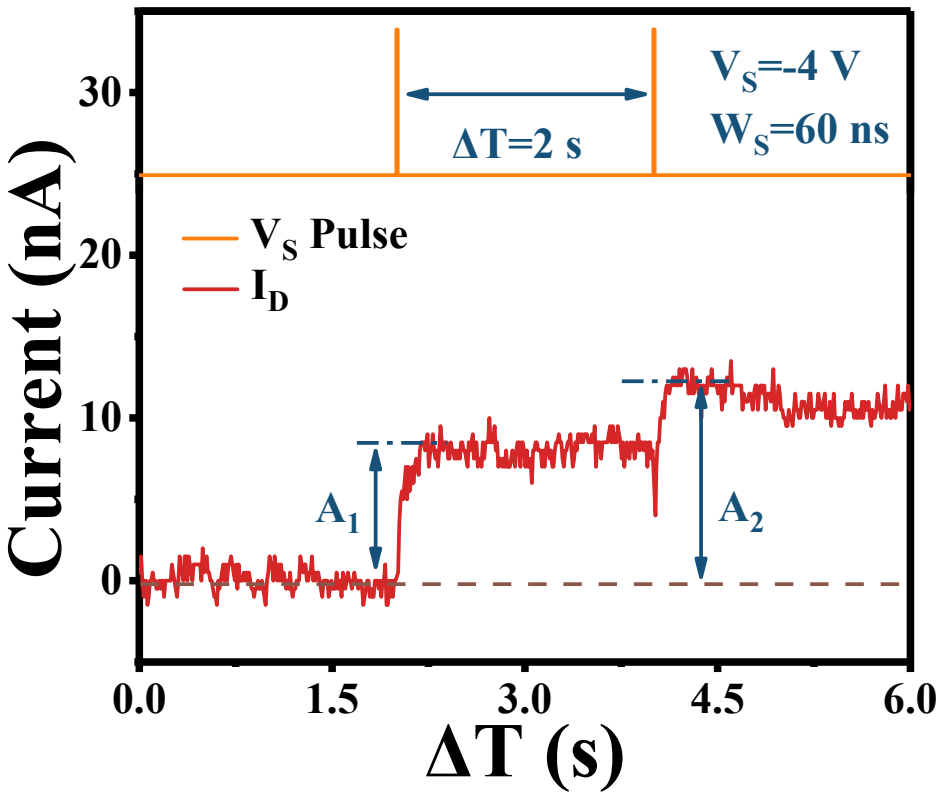

Figure S7. The PPF process is simulated by varying the time interval between two identical pulses.

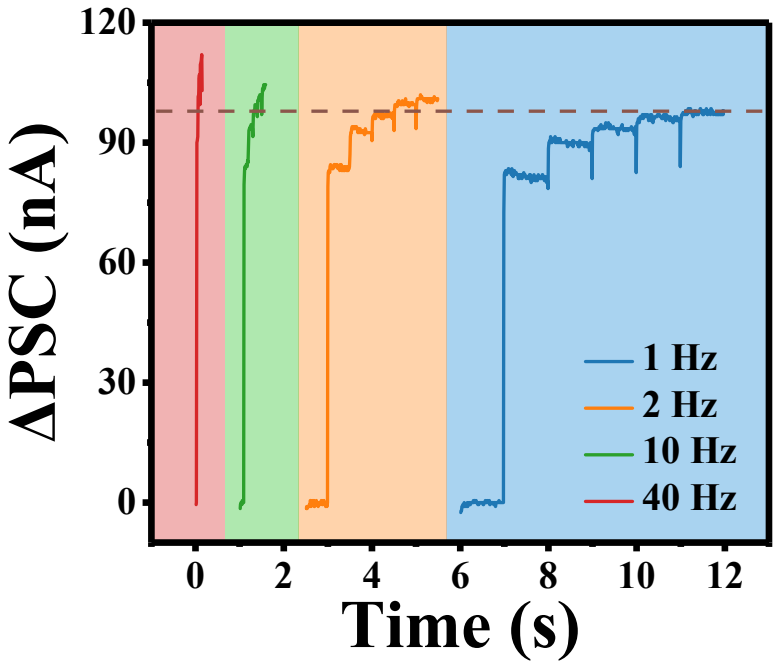

Figure S8. Relationship between ΔPSC and the frequency of pulses.

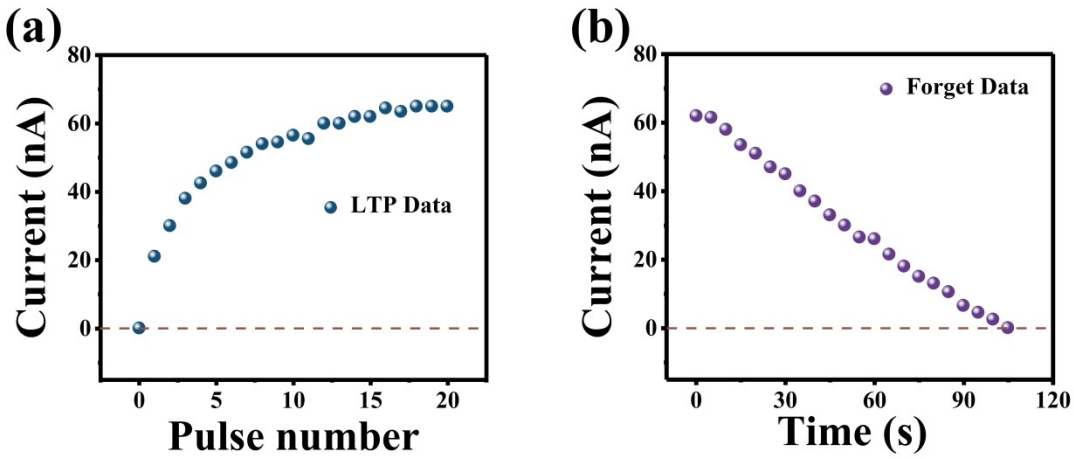

Figure S9. LTP and Forget behaviour testings of Fe-TFT device.

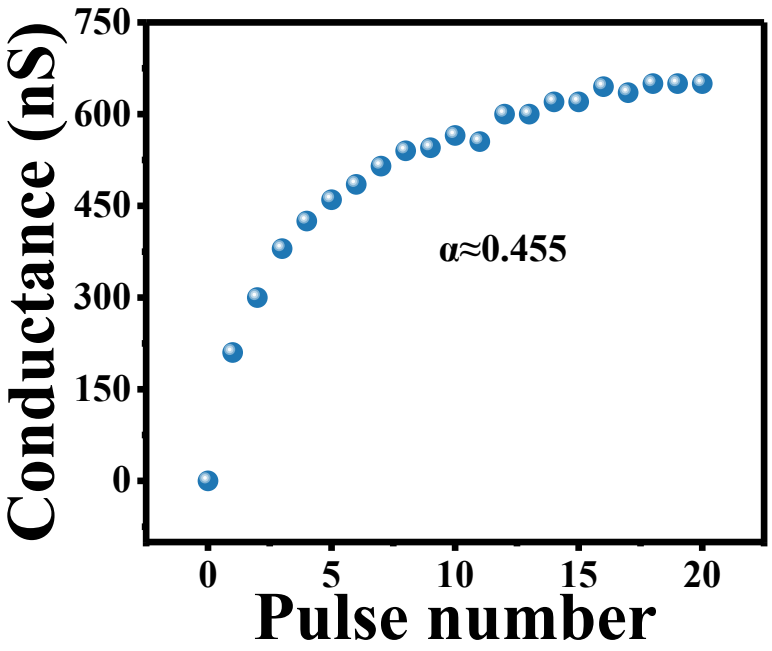

Figure S10. Change diagram of FeTFT conductance during LTP process.

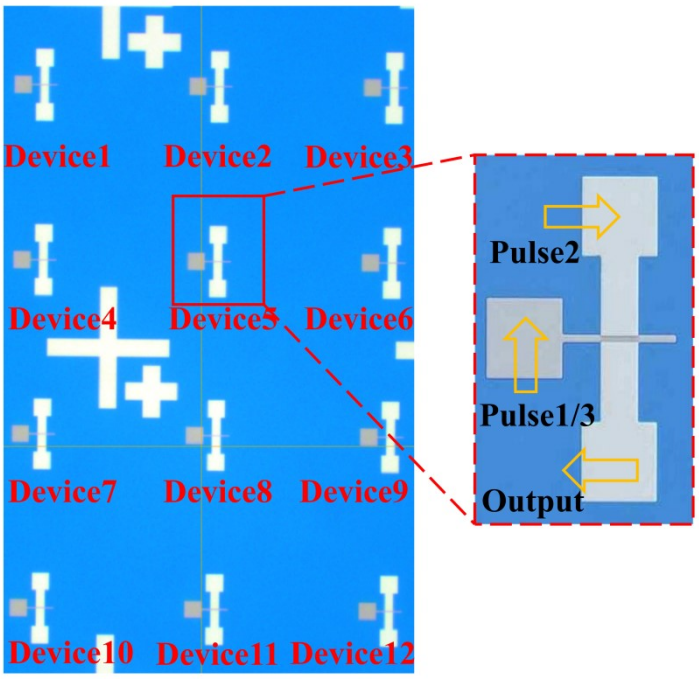

Figure S11. Array diagram of 3×4 devices.

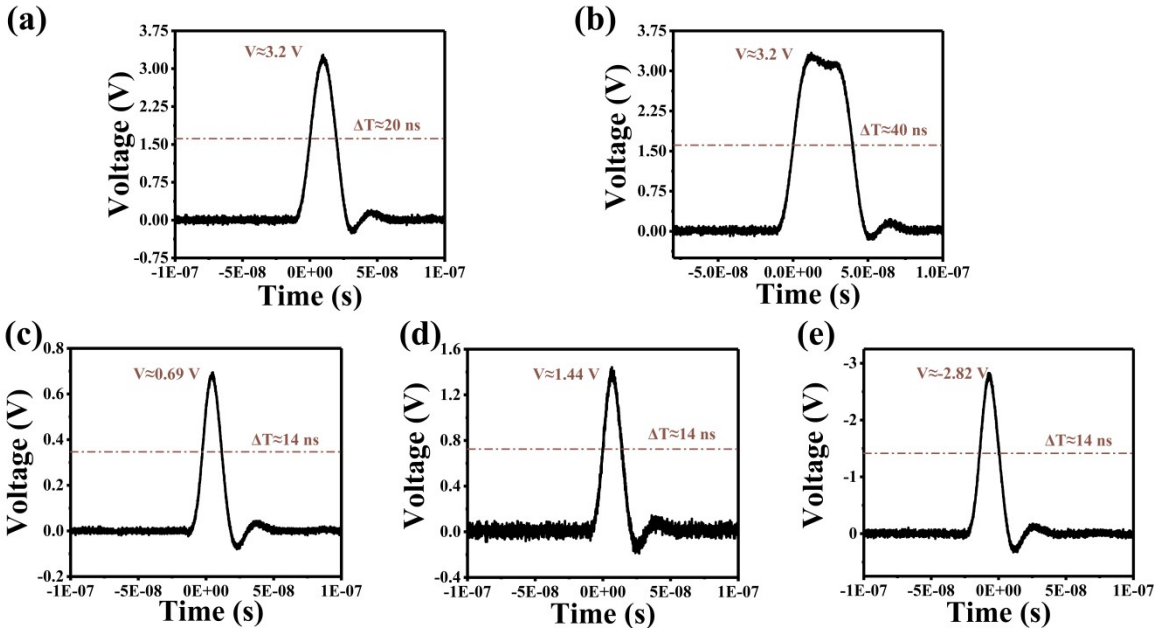

Figure S12. Shape diagram of partial pulses used in this work.

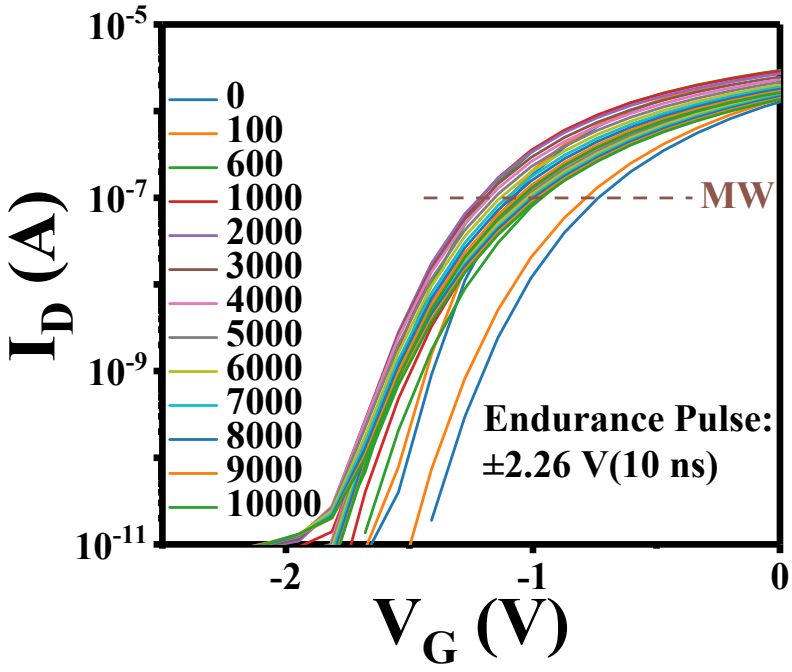

Figure S13. I_D-V_G diagram after applying different numbers of pulses.

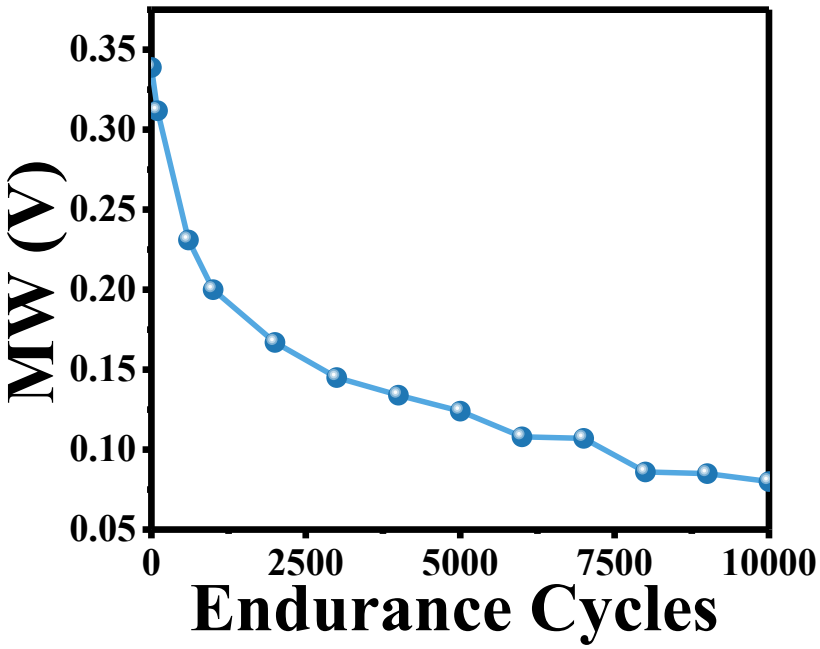

Figure S14. The relationship between memory window and endurance cycles.

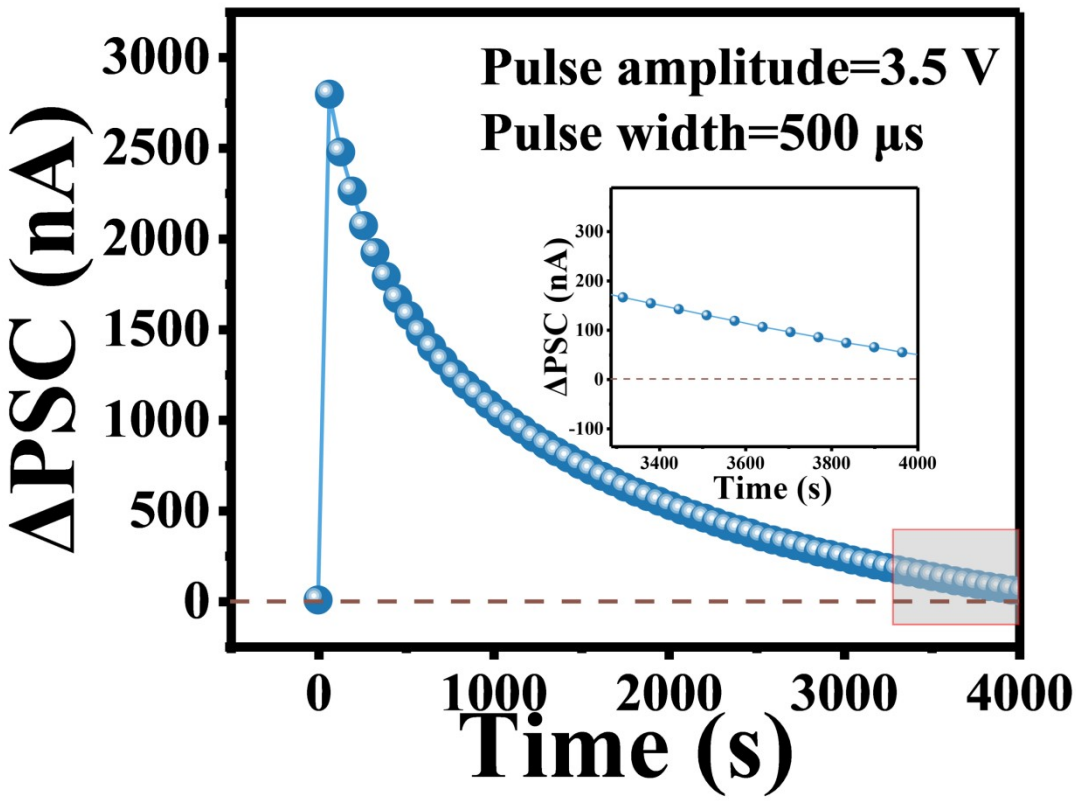

Figure S15. Decay of the ΔPSC as a function of time measured after the stimulation of V = 3.5 V, t =500 µs.

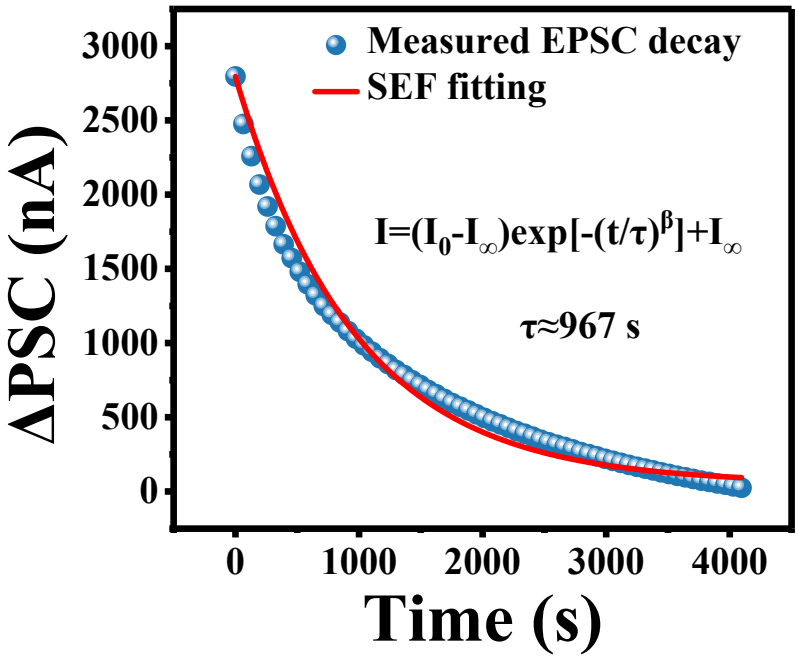

Figure S16. The forgetting curve was fitted by the formula.

Endurance and retention characteristics of FeTFTs

Figure S13 shows the I_D-V_G figure of the prepared FeTFT during the endurance process. It can be seen that as the endurance cycles gradually increase, the memory window (MW) gradually decreases, which is due to the trapping of charges [18]. Even after 10^4 endurance cycles, the device still exhibits a counterclockwise MW (Fig. S14). The retention characteristics of FeTFT are characterized by fitting a forgetting curve. As shown in Fig. S15, the forgetting curve under the action of more intense pulses was fitted by the following Formula:

$$I=(I_0-I_\infty)\exp[-(t/\tau)^\beta]+I_\infty \quad (1)$$

where τ is the retention time, I_0 is the triggered EPSC at the end of the synaptic spike, I_∞ is the final value of the decay current and β is the stretch index ranging between 0 and 1. A good fitting curve of the decay of EPSC triggered by presynaptic spike (3.5 V, 500 μs) is obtained, as shown in Figure S16. τ is estimated to be 967s.

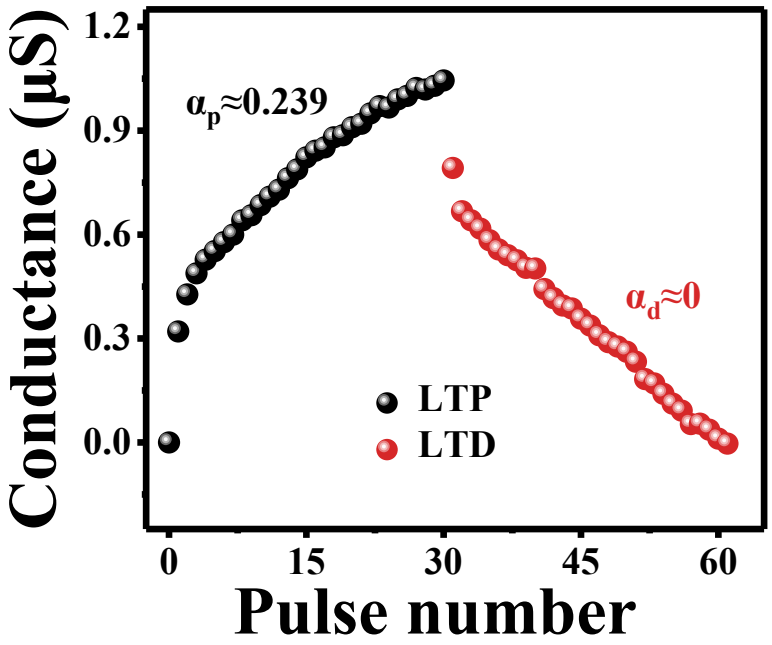

Figure S17. Change diagram of FeTFT conductance during LTP/LTD process.

Asymmetry and linearity in weight update

When continuous pulses are applied, the device's conductance increases, with the maximum dynamic range being 1.045 μS (Figure S17). Asymmetry and linearity are important criteria for measuring synaptic devices. To calculate the non-linearity of LTP and LTD curves, the changes in G with the number of pulses is evaluated by the following equations:

$$G_p = B(1-e^{-P/A_P}) + G_{min} \quad (1)$$

$$G_d = -B(1-e^{(P-P_{max})/A_d}) + G_{max} \quad (2)$$

$$B = \frac{(G_{max} - G_{min})}{(1-e^{-P_{max}/A_{P,d}})} \quad (3)$$

$$\alpha_{P,d} = \frac{1.726}{(A_{P,d} + 0.162)} \quad (4)$$

where G_p is the G of potentiation, G_d is the G of depression, P_{max} is the maximum number of

pulses, and α represents the non-linearity factor in the conductance modulation during LTP and LTD processes [7,19]. It can be observed that the non-linearity of the LTP and LTD processes is $\alpha_p \approx 0.239$ and $\alpha_d \approx 0$, indicating a good linearity of the obtained LTP and LTD processes. In addition, the asymmetry of the LTP and LTD processes can be described by $|\alpha_P - \alpha_d|$. The calculated value of asymmetry is 0.239.

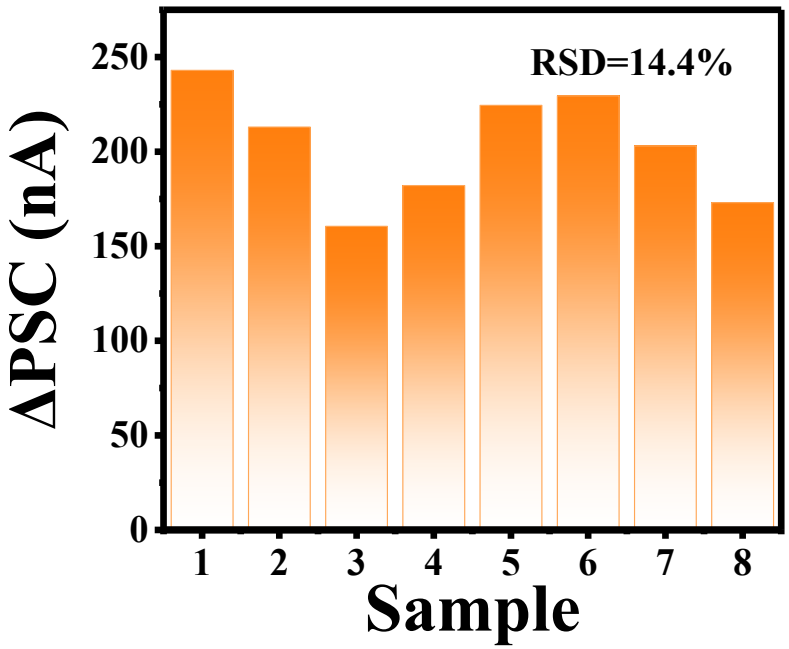

Figure S18. Statistical diagram of ΔPSC after applying the same stimulus to eight devices.

Synaptic Structure	FE Layer	Channel	Pulse Voltage (V)	Pulse Width (ns)	Ref.
FeFET	HZO	Si	-0.2	1000	1
FE-SBFET	HZO	Si	-2	20	2
Ge FE NWFET	HZO	Ge	-5	50	3
JL FE FinFET	HZO	Si	3.7	1000	4
SL FeFET	HZO	IWO	3.5	100	5
Fe-TFTs	HZO	GeSn	-4	100	6
FeFET	HZO	Si	3.7	20	7
FeFET	HZO	Si	3	100	8
MFMFIS FET	HSO	Si	5.5	50	9
FeFET	HZO	Si	3	100	10
Fe-TFT	**HLO**	**ITO**	**2.26**	**14**	**This Work**

Table S1. Comparison of this work with current state of artificial ferroelectric synaptic devices in terms of operating speed (Pulse Width).

Device	Asymmetry $\lvert \alpha_p - \alpha_d \rvert$	Nonlinearity α_p/α_d	uniformity	ΔG	Endurance	τ_{Forget} (Pulse conditon)	Energy/spike	τ_{PPF} (Pulse conditon)	reference
FeT-TFT	1	-1.27/-2.27	-	2.61 nS	10000	-	-	-	11
FeTFT	0.62	-3.37/-3.99	-	13.4 nS	10000	-	-	-	12
FeFET	0.29	1.75/1.46	-	~59 μS	-	-	-	-	7
Ge FE Nanowire pFET	2.97	1.22/-1.75	-	Few hundreds uS	>2500	-	-	-	3
SL FeTFT	0.86	-0.7/-1.56	-	~6 μS	-	-	-	-	5
IZO-FET	-	-	-	-	-	15ms (1V, 10ms)	-	-	13
FEMOD	0.19	-0.07/0.12	α: <4%	-	$>10^5$	-	<1fJ	2.3μs(1V,1μs)	14
FGOST	-	-	-	-	-	2.29s(20V,300ms)	-	589ms(20V,300ms)	15
NiO-based memristor	-	-	-	-	-	68s(2V,10ms)	-	-	16
MoS_2 FET	3.07	0.5/3.57	-	-	-	-	≈7.3fJ	-	17
FeTFT	**0.239**	**0.239/0**	**RSD=14.4%**	**1.045 μS**	**10000**	**967s(3.5V, 500μs)**	**93.1 aJ**	**1.58s(2V,100ns)**	**This work**

Table S2. The comparison of this work with other reported devices in terms of synaptic properties.

REFERANCES

1 F. Xi, Y. Han, M. Liu, J.H. Bae, A. Tiedemann, D. Gruetzmacher and Q.-T. Zhao, *ACS Appl. Mater. Interfaces* 2021, **13**, 32005-32012.

2 F. Xi, Y. Han, A. Tiedemann, D. Grutzmacher and Q.T. Zhao, *2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC)* 2021, 291-294.

3 W. Chung, M. Si and P.D. Ye, *2018 IEEE International Electron Devices Meeting (IEDM)* 2018, 15.2.1-15.2.4.

4 M. Seo, M.H. Kang, S.B. Jeon, H. Bae, J. Hur, B.C. Jang, S. Yun, S. Cho, W.K. Kim, M.S. Kim, K.M. Hwang, S. Hong, S.Y. Choi and Y.K. Choi, *IEEE Electr. Device L.* 2018, **39**, 1445-1448.

5 K.A. Aabrar, J. Gomez, S.G. Kirtania, M.S. Jose, Y. Luo, P.G. Ravikumar, P.V. Ravindran, H. Ye, S. Banerjee, S. Dutta, A.I. Khan, S. Yu and S. Datta, *2021 IEEE International Electron Devices Meeting (IEDM)* 2021, 19.6.1-19.6.4.

6 C.-P. Chou, Y.-X. Lin, Y.-K. Huang, C.-Y. Chan and Y.-H. Wu, *ACS Appl. Mater. Interfaces* 2020, **12**, 1014-1023.

7 M. Jerry, P.Y. Chen, J. Zhang, P. Sharma, K. Ni, S. Yu and S. Datta, *2017 IEEE International Electron Devices Meeting (IEDM)* 2017, 6.2.1-6.2.4.

8 B. Zeng, C. Liu, S. Dai, P. Zhou, K. Bao, S. Zheng, Q. Peng, J. Xiang, J. Gao, J. Zhao, M. Liao and Y. Zhou, *Adv. Funct. Mater.* 2021, **31**, 2011077.

9 T. Ali, K. Seidel, K. Kuhnel, M. Rudolph, M. Czernohorsky, K. Mertens, R. Hoffmann, K. Zimmermann, U. Muehle, J. Muehle, J.V. Houdt and L.M. Eng, *2020 IEEE Symposium on VLSI Technology* 2020, 1-2.

10 M. Tang, X. Zhan, S. Wu, M. Bai, Y. Feng, G. Zhao, J. Wu, J. Chai, H. Xu, X. Wang and J. Chen, *IEEE Electr. Device L.* 2022, **43**, 1555-1558.

11 W. C.-Y. Ma, C.-J. Su, K.-H. Kao, T.-C. Cho, J.-Q. Guo, C.-J. Wu, P.-Y. Wu and J.-Y. Hung. *ECS J. Solid State Sci. Technol.* 2023, **12**, 055006.

12 W. Cheng-Yu, C.-J. Su, Y.-J. Lee, K.-H. Kao, T.-H. Chang, J.-C. Chang, P.-H. Wu, C.-L. Yen and J.-H. Lin. *Semicond. Sci. Technol.* 2022, **37**, 045003.

13 L. Q. Zhu, H. Xiao, Y. H. Liu, C. J. Wan, Y. Shi and Q. Wan. *Appl. Phys. Lett.* 2015, **107**, 143502.

14 F. Xi, A. Grenmyr, J. Zhang, Y. Han, J. H. Bae, D. Grutzmacher and Q.-T. Zhao. *Adv. Electron. Mater.* 2023, **9**, 2201155.

15 E. Li, W. Lin, Y. Yan, H. Yang, X. Wang, Q. Chen, D. Lv, G. Chen, H. Chen and T. Guo. *ACS Appl. Mater. Interfaces* 2019, **11**, 46008-46016.

16 S. G. Hu, Y. Liu, T. P. Chen, Z. Liu, Q. Yu, L. J. Deng, Y. Yin and S. Hosaka. *Appl. Phys. Lett.* 2013, **103**, 133701.

17 C. He, J. Tang, D.-S. Shang, J. Tang, Y. Xi, S. Wang, N. Li, Q. Zhang, J.-K. Lu, Z. Wei, Q. Wang, C. Shen, J. Li, S. Shen, J. Shen, R. Yang, D. Shi, H. Wu, S. Wang and G. Zhang. *ACS Appl. Mater. Interfaces* 2020, 12, (10), 11945-11954.

18 W. Xiao, C. Liu, Y. Peng, S. Zheng, Q. Feng, C. Zhang, J. Zhang, Y. Hao, M. Liao and Y. Zhou. *Nanoscale Res. Lett.* 2019, **14**, 254.

19 K. C. Kwon, Y. Zhang, L. Wang, W. Yu, X. Wang, I.-H. Park, H. S. Choi, T. Ma, Z. Zhu, B. Tian, C. Su and K. P. Loh. *ACS Nano* 2020, **14**, 7628-7638.