Supplementary Information

Linear Conductance Update Improvement of CMOS-Compatible Second-Order Memristors for Fast and Energy-Efficient Training of Neural Network Using a Memristor Crossbar Array

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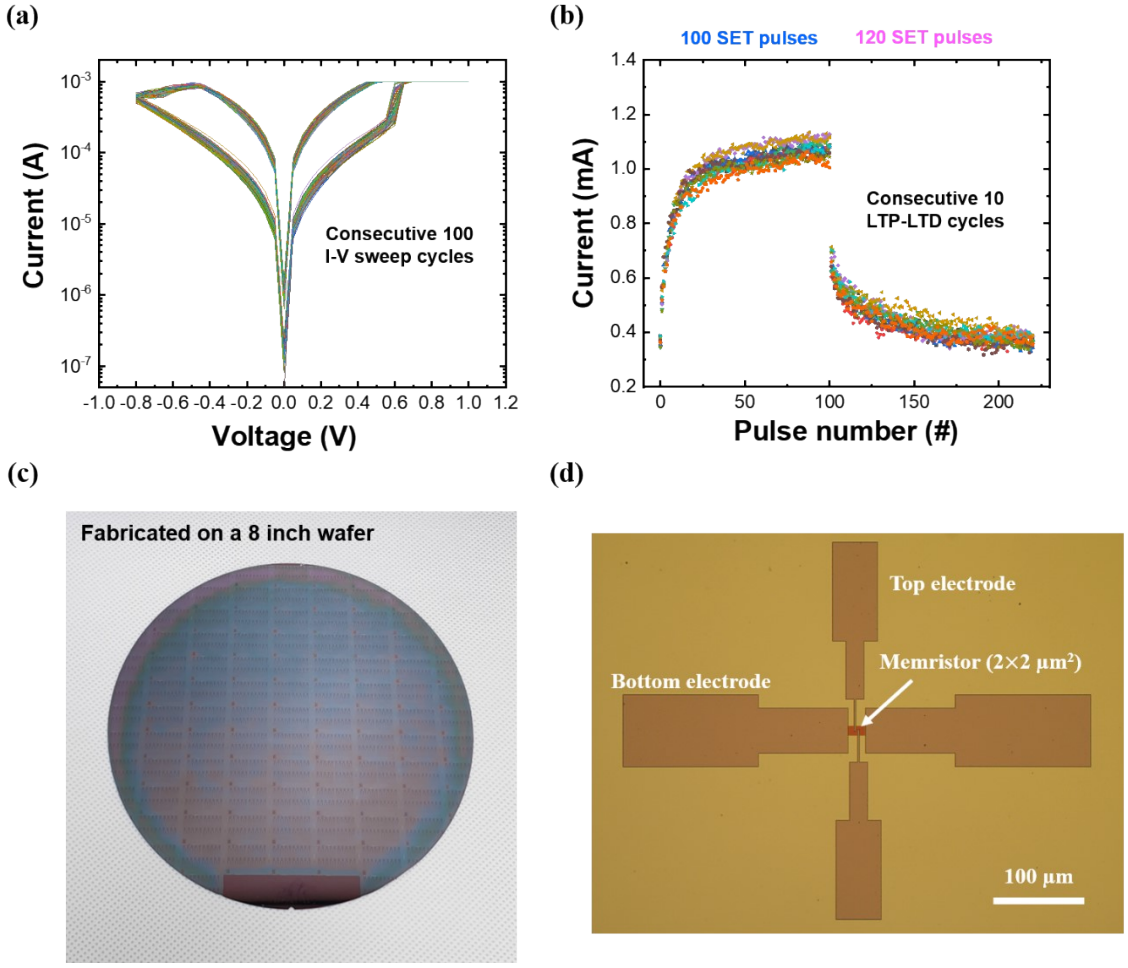

Fig. S1 Reversible and stable resistive switching characteristics of the CMOS-compatible HfO_2 memristor. (a) Consecutive 100 I-V sweep curves and (b) Consecutive 10 long-term potentiation (LTP)-long-term depression (LTD) curves of the fabricated memristor. The LTP-LTD curve is measured with consecutive 100 SET pulses (0.7 V, 1 μs) followed by consecutive 120 RESET pulses (− 0.8 V, 1 μs), and read pulses (0.2 V, 50 μs) among each SET and RESET pulse. (c) An optical image of an eight-inch wafer after fabricating the fully CMOS-compatible HfO_2 memristor. (d) An optical image of the memristor device fabricated on the wafer.

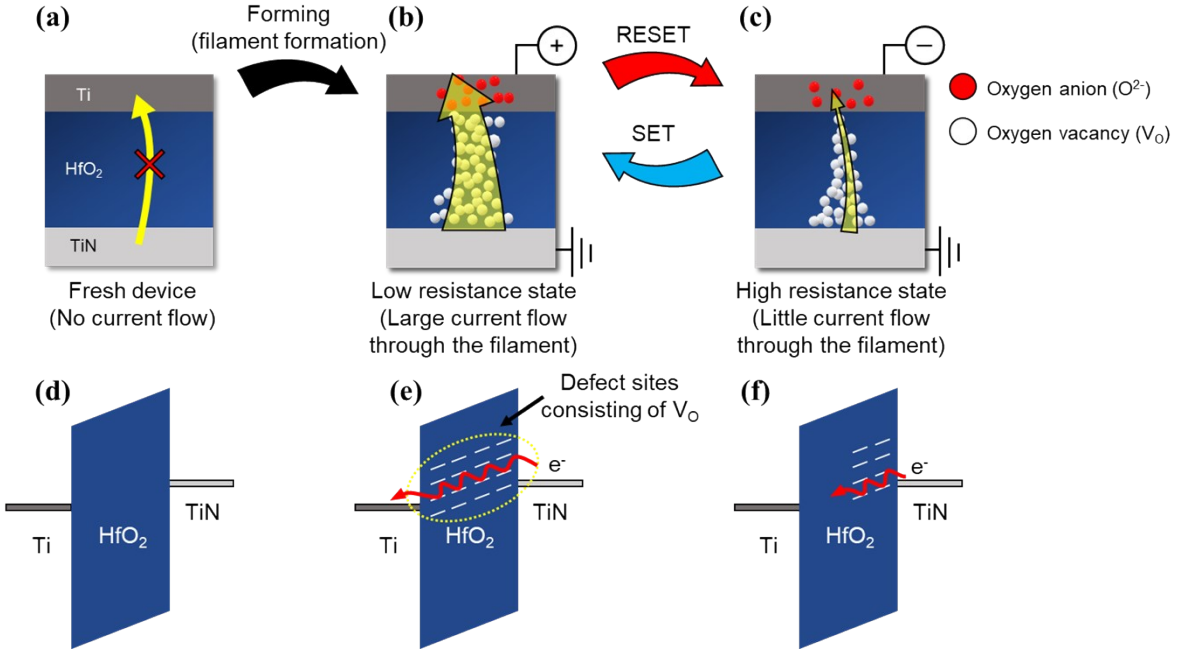

Fig. S2 Mechanisms of the resistive switching in the HfO_2 memristor. (a-c) Illustrations of the HfO_2 memristor before forming (a), after forming (b), and after reset programming (c). Basically, the growth and rupture of the conductive oxygen vacancy filament induce the resistive switching of the device. (b-d) Corresponding energy-band diagram of the HfO_2 memristor at each state in (a), (b), and (c), respectively. Before forming the filament, because there are few defect sites in the HfO_2 layer, the device has a very high resistance state. The forming process makes the oxygen anions in the HfO_2 layer move into the top electrode, and generates oxygen vacancy filament. As shown in (e), the oxygen vacancy works as a defect site in the HfO_2 layer, and conducts current by allowing electrons to flow between the top and bottom electrodes. However, the reset process makes the oxygen anions fill the defect sites, and rupture the conductive filament. Therefore, the electron flow between the electrodes is interrupted, and the device shows a high resistance state.

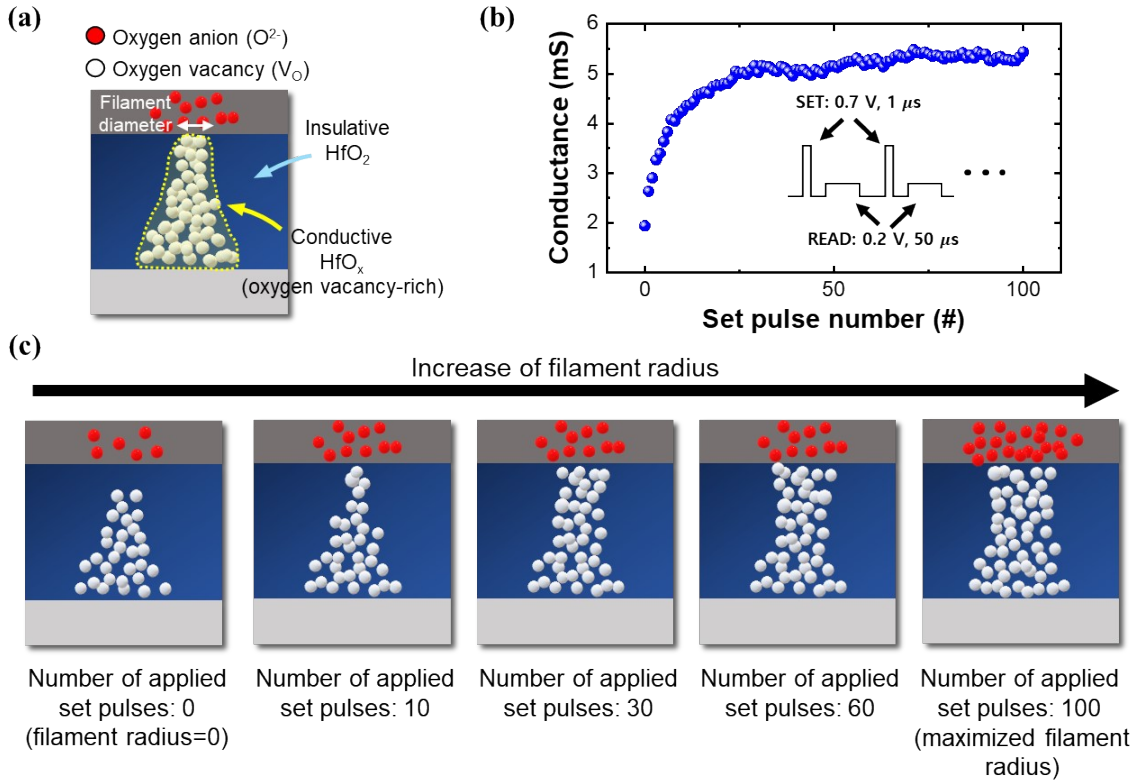

Fig. S3 Effects of the filament diameter on the device conductance as a first-state variable. (a) An Illustration of an oxygen vacancy filament after forming the device. When a positive voltage bias is applied to the top electrode while grounding the bottom electrode, oxygen anions in the HfO_2 layer are moved to the top electrode. This process generates oxygen vacancies in the HfO_2 layer and makes a conductive oxygen vacancy filament. The stoichiometry of the filament is represented as HfO_x (oxygen vacancy-rich region), and the oxygen vacancies work as hopping sites of electrons and easily conduct electrical current. (b and c) The device conductance curve according to the applied set pulses. As more set pulses are applied, more oxygen vacancies are generated, which enlarges the filament diameter. The enlarged filament diameter has a larger contact area to the top and bottom electrodes, and therefore, the device conductance increase as the filament diameter increases.

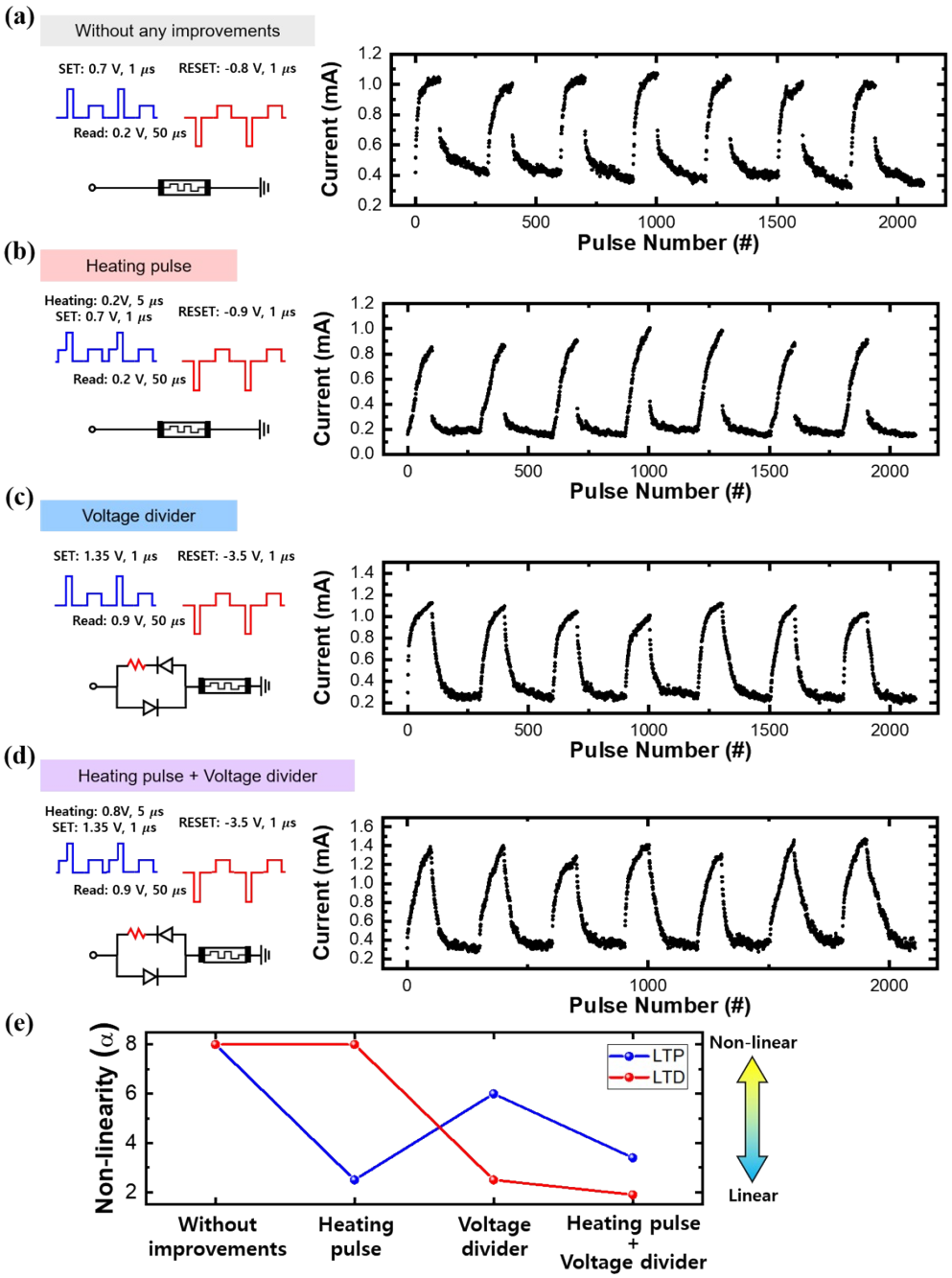

Fig. S4 Consecutive LTP-LTD curves with and without the improvements, and extracted non-linearity values. The memristor is tested under intensive SET and RESET pulses to observe the LTP-LTD curves during several cycles of LTP-LTD, and the non-linearity is extracted from the average curves for each case. The non-linearity is extracted by matching the experimental curve to the model (1),

$$G = \left(\left(G_{LRS}^{\alpha} - G_{HRS}^{\alpha}\right) \times w + G_{HRS}^{\alpha}\right)^{1/\alpha} \quad (1)$$

where G_{LRS}, G_{HRS}, w, and α are low resistance state conductance, high resistance state conductance, internal variable (normalized pulse number), and non-linearity, respectively. If the α close to the 1, then the device shows linear conductance update[1].

(a) The memristor without the improvements (no heating pulse and no voltage divider) shows highly non-linear and asymmetric potentiation and depression. (b) The memristor with heating pulse but without voltage divider shows linear potentiation but still showing non-linear and abrupt depression. (c) The memristor with a voltage divider but without heating pulse shows gradual and linear depression but shows non-linear potentiation. (d) The memristor with the improvements (with heating pulse and voltage divider) shows linear and symmetric update characteristics for both of the potentiation and the depression processes. (e) The non-linearity values from each case, showing the heating pulse and the voltage divider effectively remedy the non-linear conductance update of potentiation and depression, respectively.

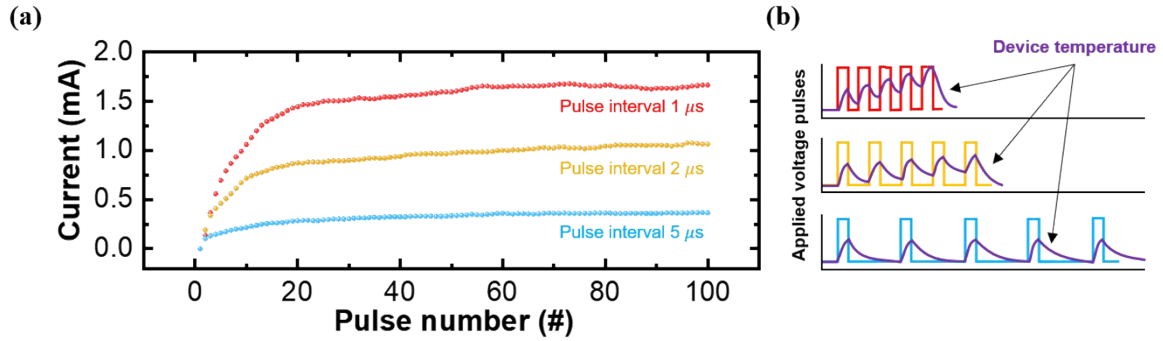

Fig. S5 Demonstration of second-order memristor effect in the HfO_2 memristor. (a) Memristor current output during the consecutive 100 SET pulses (0.6 V, 1 μs) with different pulse intervals (1, 2, and 5 μs). (b) An illustration that represent the applied voltage pulses and the device temperature at the same time from the three pulse interval cases in (a).

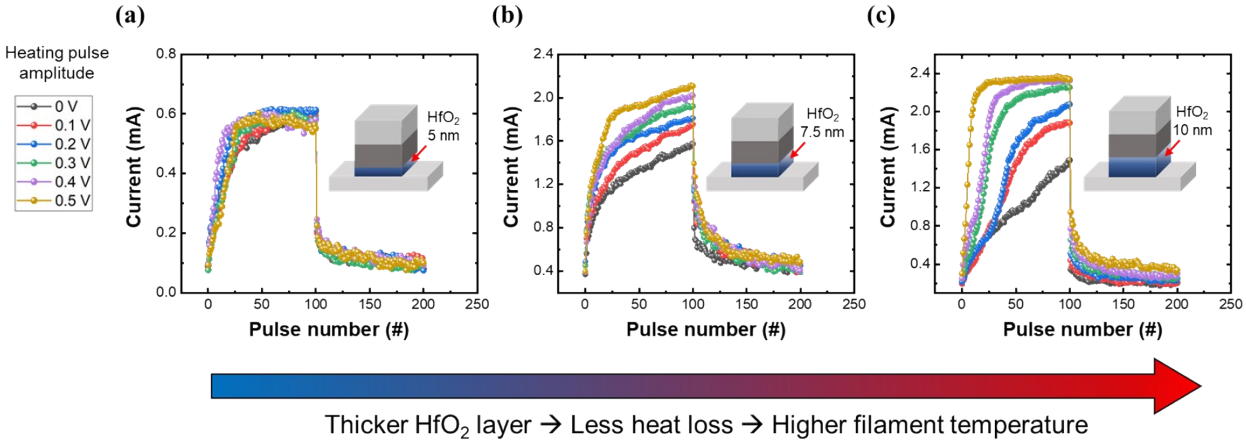

Fig. S6 LTP-LTD results with various heating pulse amplitudes and HfO_2 layer thicknesses. The LTP-LTD curves are obtained from three different HfO_2 memristor devices having different HfO_2 layer thicknesses (5, 7.5, and 10 nm for (a), (b), and (c), respectively). Various heating pulse amplitudes from 0 to 0.5 V with 0.1 V intervals are utilized for each device to analyze the optimal range of the heating pulse amplitude. The heating pulse effect is enhanced as the HfO_2 layer thickness increases because the thicker oxide prevents the generated Joule heat from escaping from the device, which induces a stronger heating pulse effect. In addition, the larger heating pulse amplitude induces a higher on/off ratio, but the potentiation non-linearity becomes significant as the heating pulse exceeds 0.5 V for (b) and 0.3 V for (c). The utilized pulses for (a), (b), and (c), are as follows: set pulse (0.65 V, 1 μs), reset pulse (-0.85 V, 2 μs) for (a), set pulse (0.75 V, 1 μs), reset pulse (-0.9 V, 2 μs) for (b), set pulse (0.75 V, 1 μs), reset pulse (-0.9 V, 4 μs) for (c). The heating pulse (0 ~ 0.5 V, 5 μs) and read pulse (0.2 V, 50 μs) are the same for every case.

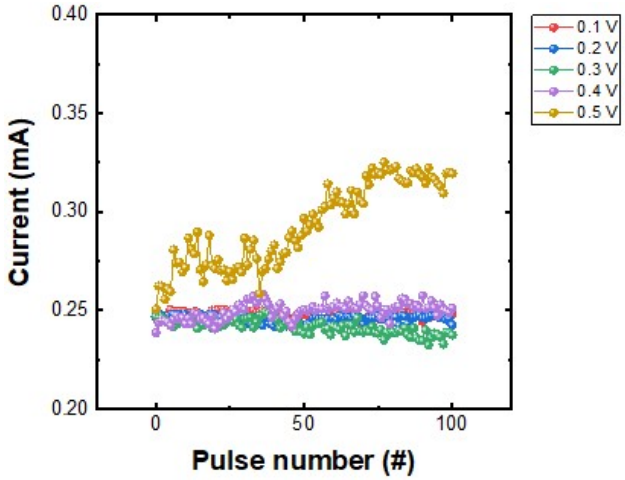

Fig. S7 Conductance versus applied pulse number curve. To find the maximum amplitude of the heating pulse that does not change the device conductance but generates the Joule heating, the 7.5 nm HfO_2 device conductance is measured by applying consecutive heating pulses without set and reset pulses. The heating pulse amplitude lower than 0.4 V does not change the device conductance, but the 0.5 V heating pulse clearly increases the device conductance. The 0.5 V heating pulse not only generates the Joule heat but also directly changes the device conductance, and therefore, the device potentiation non-linearity becomes significant for 0.5 V heating pulse case in the Figure S6b.

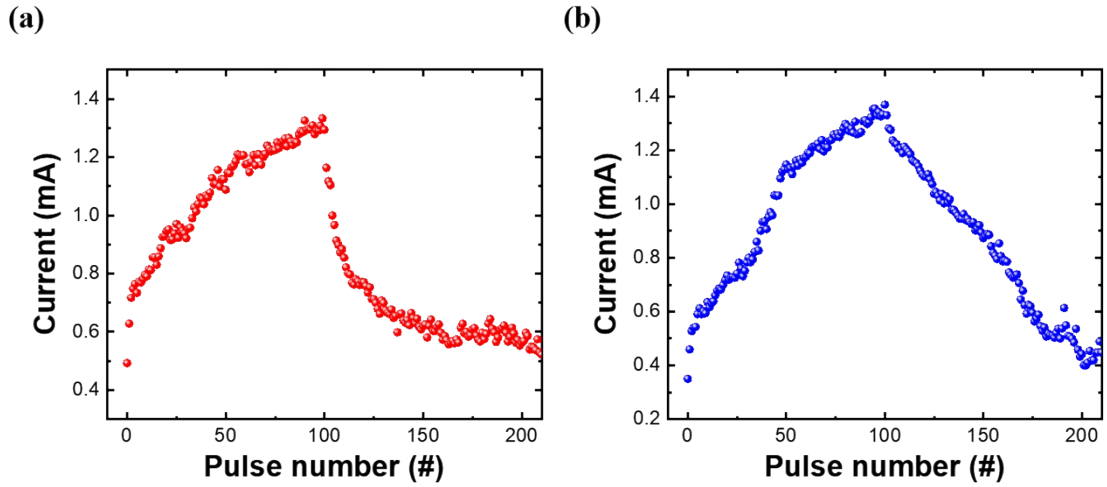

Fig. S8 Effect of the series resistance to the depression linearity. (a) The LTP-LTD curve of the memristor with voltage divider composed of a 560 Ω resistor and two PN diodes, showing the non-linearity is little bit mitigated but still significant in the depression region. Here, SET pulse (1.4 V, 1 μs) and RESET pulse (− 3.2 V, 1 μs) are used with read pulse (0.9 V, 50 μs). (b) The LTP-LTD curve of the memristor with voltage divider, but with a larger (680 Ω) resistor, showing the depression linearity is completely mitigated. Here, SET pulse (1.4 V, 1 μs) and RESET pulse (− 3.4 V, 1 μs) are used with read pulse (0.9 V, 50 μs).

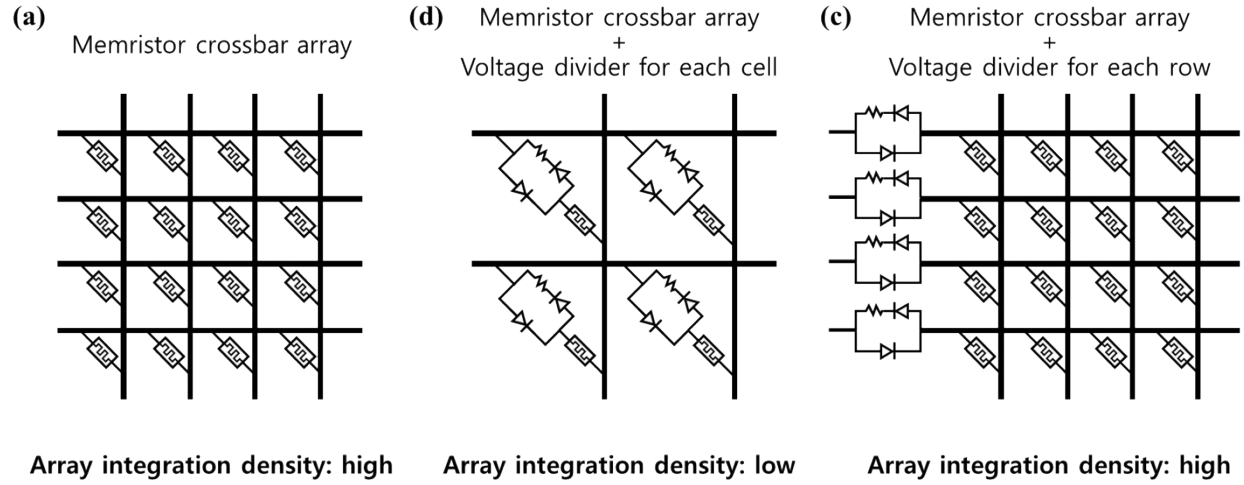

Fig. S9 Illustrations for memristor crossbar array design with the voltage divider. (a) A memristor crossbar array without voltage divider circuits. In this case, each memristor requires only a small area. Therefore, the array integration density is high, but with a low linear conductance update. (b) A memristor crossbar array when each memristor cell has the voltage divider. Because the voltage divider consisting of two diodes and a resistor is fabricated for every single cell, the required area for each cell is extremely large and the array integration density becomes low. (c) A memristor crossbar array when the voltage divider is assigned for each row wire. Because memristors in the same row share a single voltage divider, voltage dividers as much as the number of row wires are required instead of the number of memristors in a crossbar array. Therefore, each memristor requires a small area and the array integration density is high.

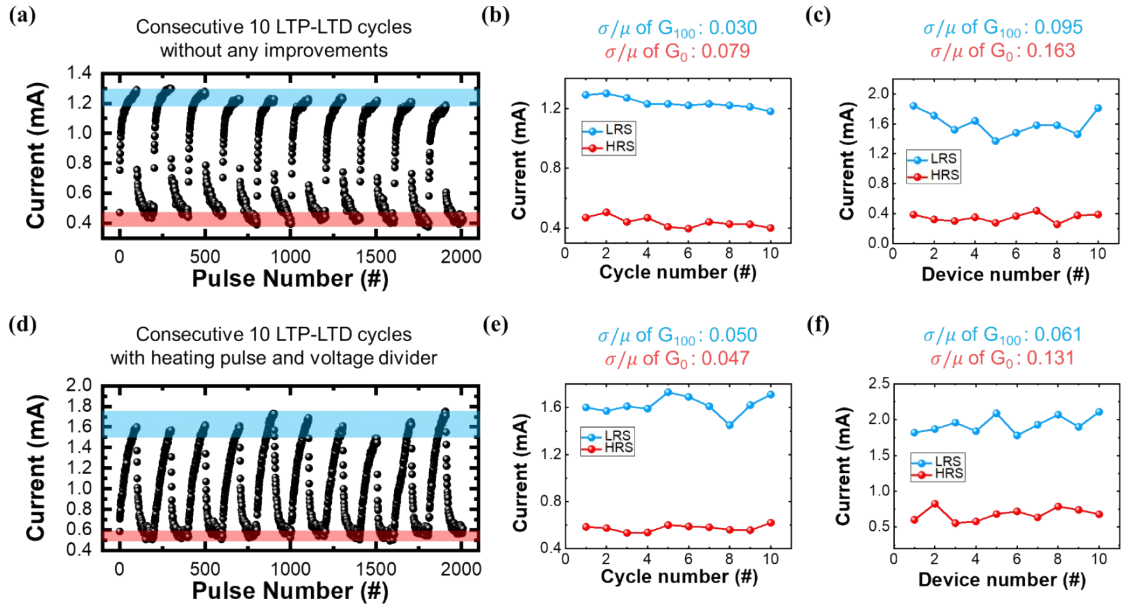

Fig. S10 Cycle-to-cycle and device-to-device variations for the HfO_2 memristor and effects of the heating pulse and voltage divider on variations. (a) 10 cycles of LTP-LTD with consecutive 100 set pulses followed by 100 reset pulses to analyze the cycle-to-cycle variation. (b) Distribution of the HRS and LRS and the variation coefficients (σ/μ) for HRS and LRS in (a). G_0 and G_{100} represent the conductance of the memristor after 0 and 100 set pulses, respectively, are applied. (c) Distribution of HRS and LRS and σ/μ from randomly selected 10 devices to analyze the device-to-device variation, exhibiting that the device-to-device variation is more significant than the cycle-to-cycle variation. (d) The 10 cycles of LTP-LTD measured from the HfO_2 memristor with the heating pulse and voltage divider. (e) Distribution of the HRS and LRS and σ/μ for HRS and LRS in (d), showing that the heating pulse and voltage divider have little effect on the cycle-to-cycle variation. (f) Distribution of HRS and LRS and σ/μ from randomly selected 10 devices and with the heating pulse and voltage divider, to analyze the effect of the heating pulse and voltage divider on the device-to-device variation. The results show that the device-to-device variation with the heating pulse and voltage divider is similar to the device-to-device variation without any improvement, demonstrating that the developed method barely affects the cycle-to-cycle and device-to-device variations of the HfO_2 memristor.

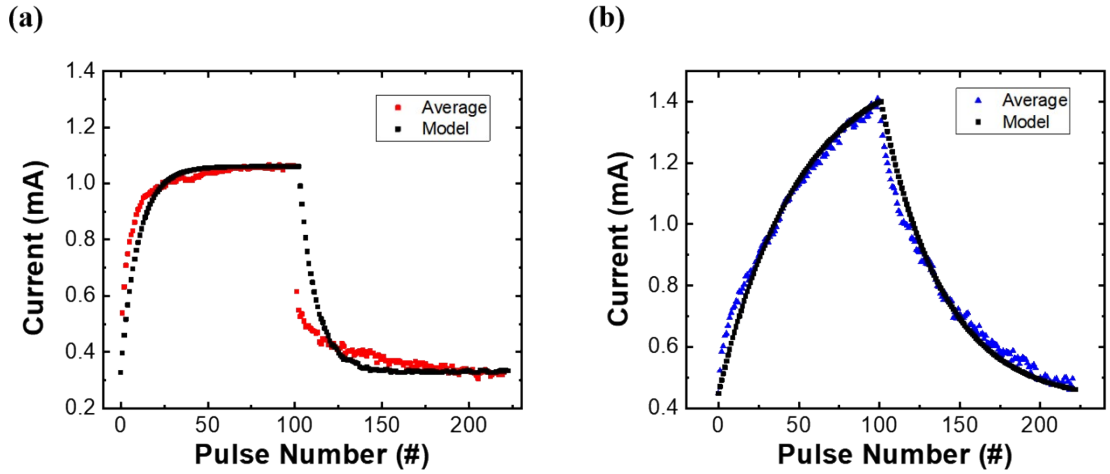

Fig. S11 LTP-LTD modeling to simulate the memristor-based neural network. The average LTP-LTD curve of the experimental data from (a) the memristor without any improvement (without the heating pulses and voltage divider) and (b) the memristor with improvements (with the heating pulse and voltage divider), and the modeled LTP-LTD curves for the simulation. The model in (a) shows a much more gradual slope in the depression curve compared to the experimental data due to the model's limitation to represent the severe non-linearity of the catastrophic depression.

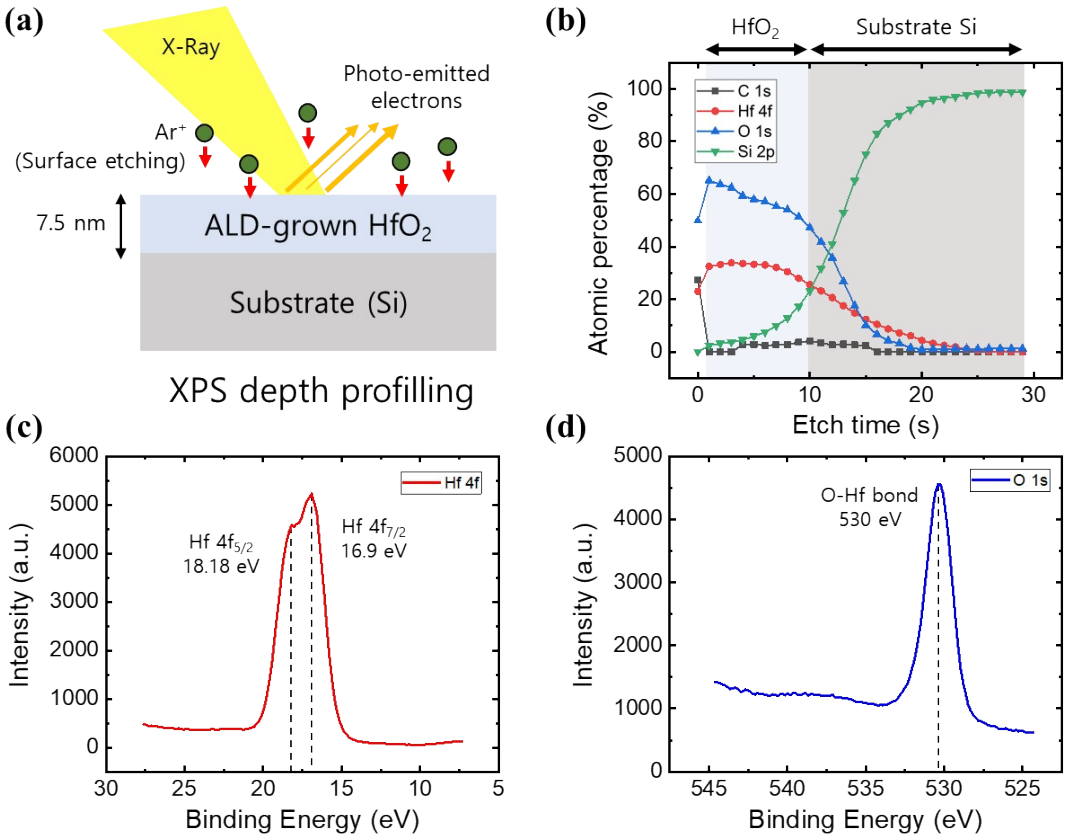

Fig. S12 X-ray Photoelectron Spectroscopy (XPS) depth-profile results of the ALD-deposited HfO_2 layer. (a) An illustration of the XPS analysis on the 7.5 nm of ALD-deposited HfO_2 film on the Si substrate. By sputtering the surface during the analysis, the depth-profile information of the sample is obtained. (b) The atomic percentage curve of some elements (C, Hf, O, and Si) according to the etch time or the depth from the surface. The ratio between Hf and O maintains 1:2 in the HfO_2 layer, demonstrating that the deposited hafnium oxide film possesses a stoichiometric HfO_2 structure. (c and d) The spectra of the Hf 4f and O 1s showing the peak energy at 18.18 and 16.9 eV for Hf and 530 eV for O. The obtained peaks agree with various reported peak information of the HfO_2, supporting that the stoichiometric HfO_2 film is deposited through the ALD process instead of a non-stoichiometric HfO_x compound[2–4].

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