Supplementary information

High Current Treated-Passivated Graphene (CTPG) towards stable Nanoelectronic and Spintronic Circuits

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1. Estimation of charged impurity concentration and trapped charge density from Dirac curves

Electrical transport measurements were carried out in a high-vacuum environment using a room-temperature setup with a Keithley current source and a nanovoltmeter. Gate voltage was applied using a Keithley 2400 source meter. The estimation of charged impurity density was based on the equation $\sigma(n) = Ce\left|\frac{n}{n_{imp}}\right| + \sigma_{res}$, where C = 5 × 10^{15} $V^{-1}s^{-1}$, n represents the carrier density, e is the electronic charge, σ_{res} is the residual conductivity, and $\sigma = \left(\frac{2e^2}{h}\right)\left(\frac{1}{R_{ch}}\right)$, where h is the Planck constant, and R_{ch} represents channel resistance. The mobility of the charge carriers is extracted from the slope of a transfer curve (Fig. S1 and S2) using the following equation $\mu = \frac{\Delta\sigma}{\Delta V_G} \frac{L_{ch}}{W_{ch} e C_g}$, where V_G is the applied gate voltage, L_{ch} and W_{ch} are the length and width of the graphene channel. The gate-dependent characteristics for graphene and graphene covered with AlO_x at each step of the current treatment are shown in Figures S1 and S2. The presence of a trapped charge density ($n_{trap} = \Delta V_{DP}\, C_g/2e$ in the charge trapping effect, where ΔV_{DP} indicating the change in Dirac point in hysteresis of Dirac curves, C_g representing the gate capacitance, and e denoting the electronic charge) was observed in all samples compared to the actual shift in the Dirac point due to the top oxide layers[1,2].

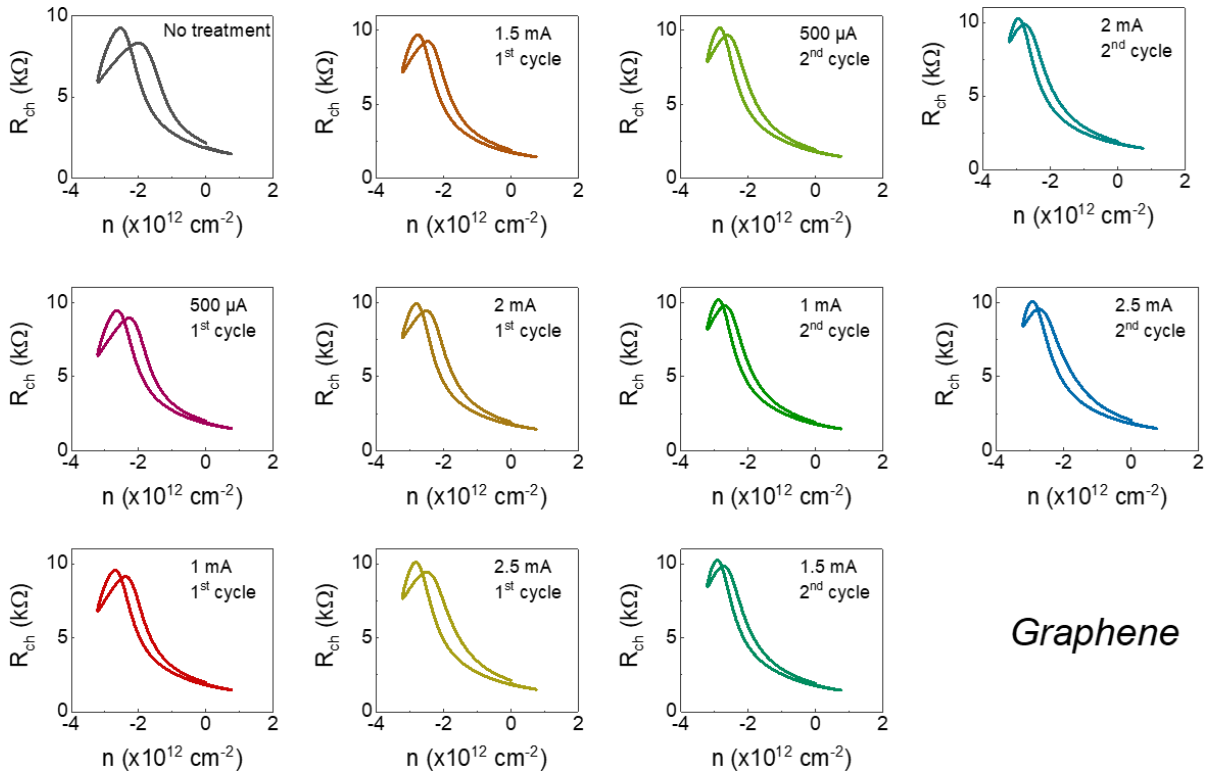

Figure S1. Back-gate voltage dependent four-probe channel resistance measurements on bare graphene devices: Channel resistance (R_{ch}) vs carriers concentration (n) for bare graphene devices after different values of high-current treatment (shown in the legend).

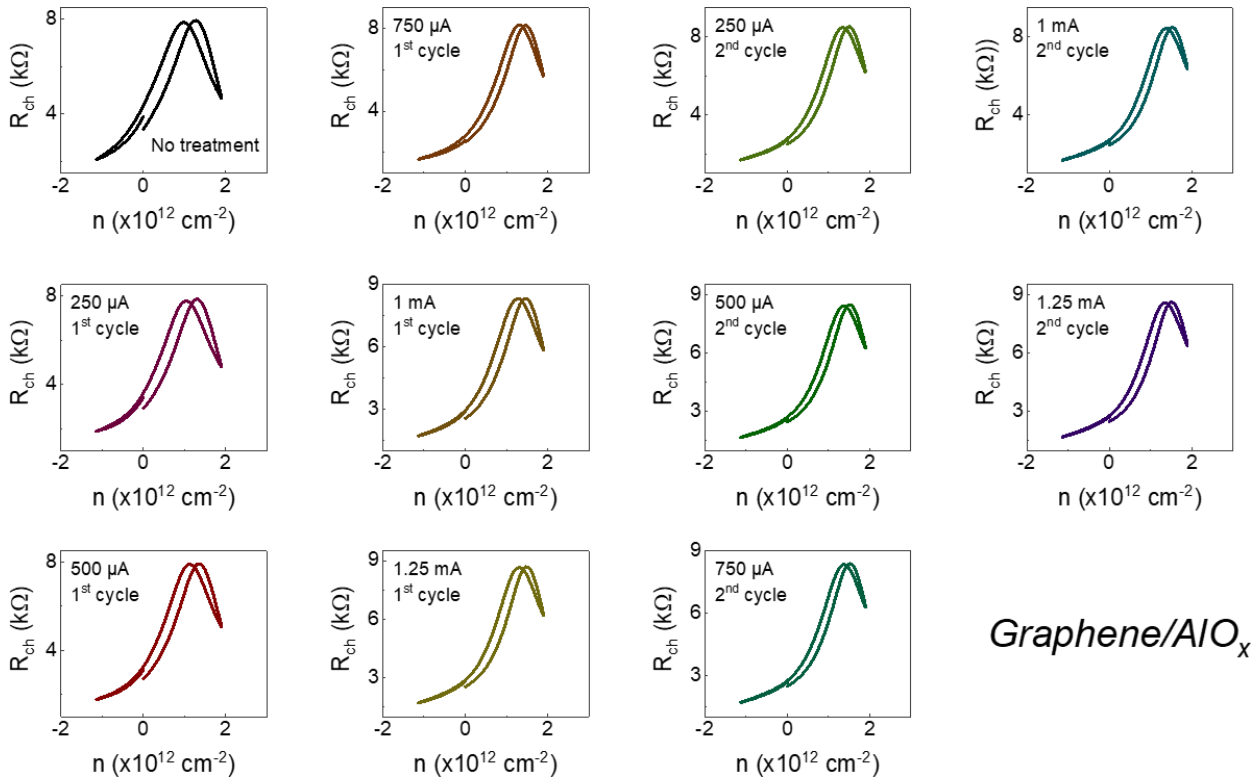

Figure S2. Back-gate voltage dependent four-probe channel resistance measurements on AlO_x-passivated graphene devices: Channel resistance (R_{ch}) vs carriers concentration (n) for AlO_x-passivated graphene devices after different values of high-current treatment (shown in the legend).

2. Reproducibly obtained enhanced mobility in Graphene/AlO_x

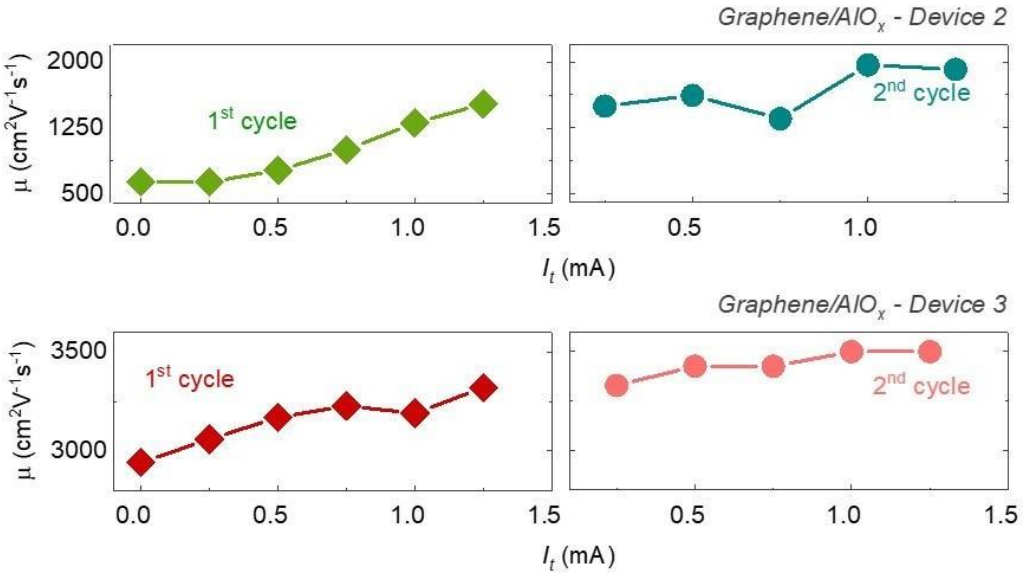

Figure S3. Field effect mobility of graphene/AlO_x before treatment (0 mA) and after each step (15 minutes at 0.5 mA, 1 mA, 1.5 mA, 2 mA, 2.5 mA) of current treatment in 2 cleaning cycles for Devices number 2 and 3 on separate chips.

3. Spatially resolved Raman spectroscopy mapping of Graphene and Graphene/AlO_x devices with treated and untreated areas

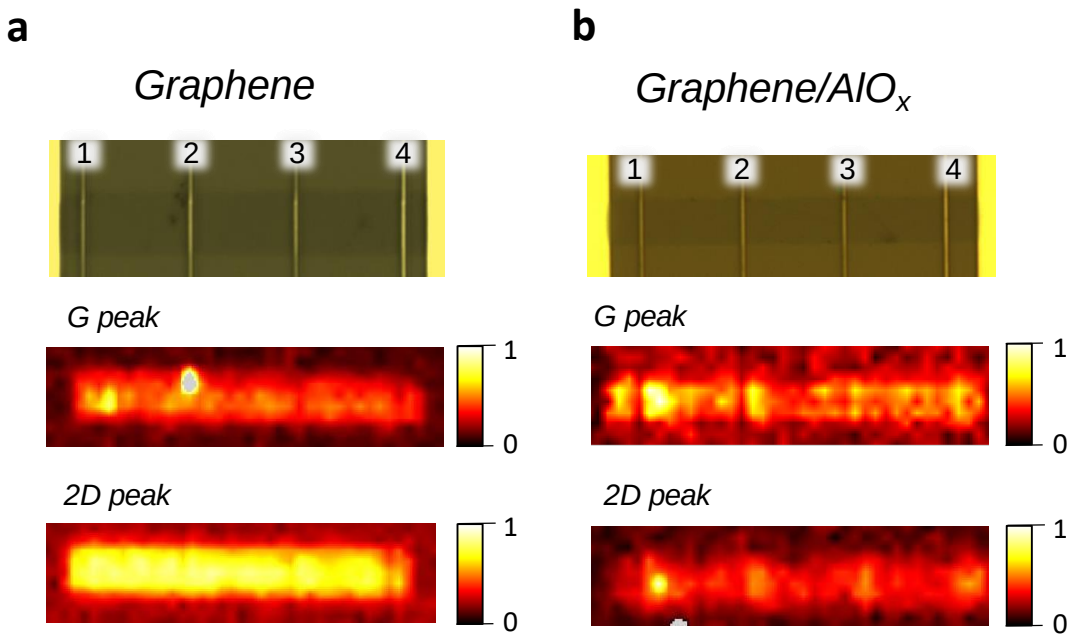

Figure S4. Spatially resolved Raman spectroscopy mapping of (a) Graphene and (b) Graphene/AlO_x-based devices, the channel between contact 1 and 2 not treated, between 3-4 treated. Raman G peak and 2D peak intensities map of the channel normalized to the maximum of the corresponding peak.

4. Surface morphology analysis of AlO_x-passivated graphene-based device with treated and untreated areas

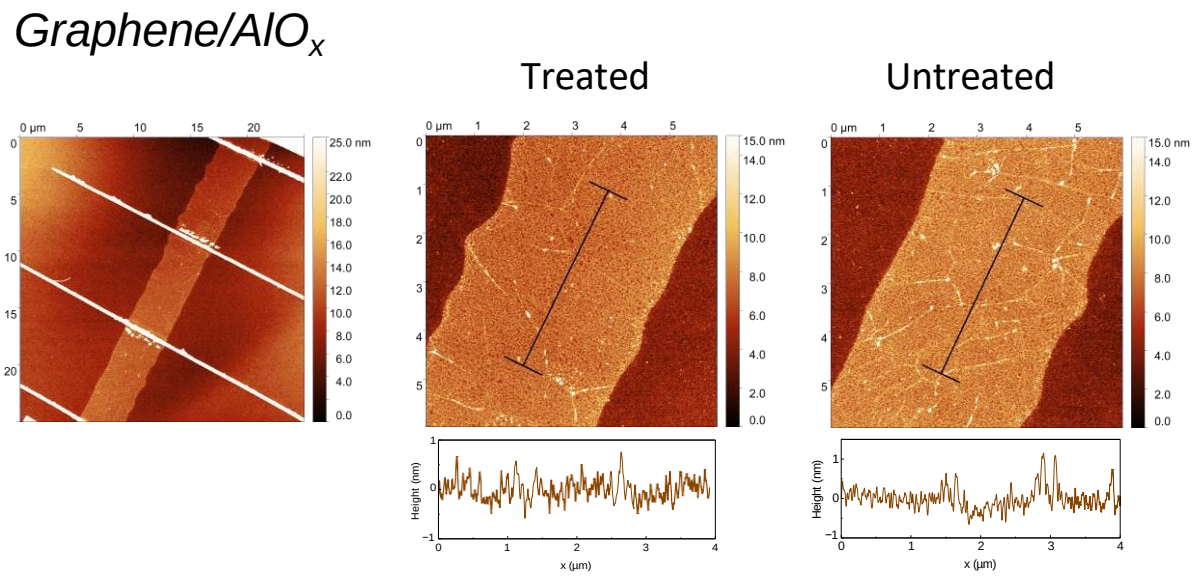

Figure S5. Atomic force microscopy (AFM) images of graphene/AlO_x devices after the current cleaning process on the right side. The corresponding black lines show a roughness profile with extracted root mean square (RMS) roughnesses.

To get insights into the characteristics and behavior of the device in nanoscale, we measured surface roughness, identified nanoscale features, and evaluated the impact of fabrication and current treatment processes. To examine the topography of graphene|AlO_x devices under ambient conditions, we employed AFM in ScanAsyst Air mode with a scan rate of 1.00 Hz, and scanning electron microscopy (SEM) images. To address potential AFM artifacts such as creep/scanning drift and tilt, we applied Gwyddion's scan line rectification (align rows) and data leveling (plane level)

tools for image correction. With sub-nanometer roughness in all passivated regions (untreated and treated), our findings indicate that the graphene/AlO_x devices have no significant topographical alterations in treated compared to untreated regions. From SEM images, the film appeared to adhere well to the substrate, displaying a compact structure. Importantly, no new features such as cracks or pinholes were observed after treatment, indicating the absence of other phases or structural changes.

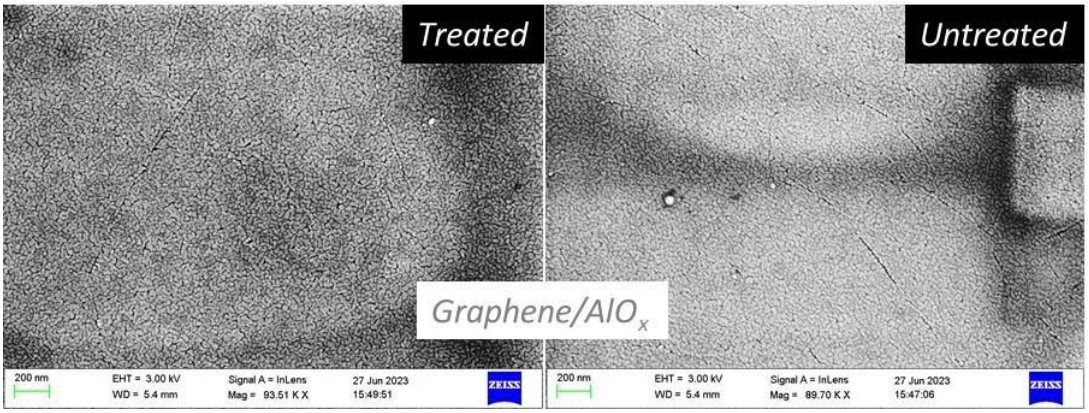

Figure S6. SEM images of graphene/AlO_x devices for untreated and current treated regions.

References

1 J. H. Chen, C. Jang, S. Adam, M. S. Fuhrer, E. D. Williams and M. Ishigami, *Nat. Phys.*, 2008, **4**, 377–381.

2 G. Kalon, Y. Jun Shin, V. Giang Truong, A. Kalitsov and H. Yang, *Appl. Phys. Lett.*, 2011, **99**, 1–4.