Electronic Supplementary Information (ESI)

Reliability effects of lateral filament confinement by nanoscaling the oxide in memristive devices

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			Lateral Oxide					
			Encapsulation in a	Smallest Lateral	Immediate Filament			
Authors	Reference	Year	Diffusion Barrier?	Oxide Dimension	Surrounding	Device Design	Film Stack	Electrode Overlap
P. Stasner et al.	This study		Yes	10 nm	SiN	Sidewall technology	Ta/TaOx/Pt	10 x 150 nm²
Doevenspeck et al.	10	2021	Yes	60 nm*	Oxide	Pillar	Ta/TaOx/unknown	Ø60 nm²
Y. Hayakawa et al.	30	2015	Yes	100 - 200 nm	Oxide	Pillar	TaN/TaOx/TaOy/Ir	Ø20 nm²
X. Sheng et al.	35	2019	No	Unscaled	Oxide	Electrode cross-bar	Ta/TaOx/Pt	25 x 25 nm ²
MJ. Lee et al.	36	2011	No	Unscaled	Oxide	Electrode cross-bar	TaOy/TaOx/Pt	30 x 30 nm ²
Y.Y. Chen et al.	37	2012	No	40 nm*	Oxide	Electrode cross-bar	Hf/HfOx/TiN	40 x 40 nm²
C.Y. Chen et al.	38	2014	No	20 nm*	Oxide	Electrode cross-bar	Ta/TaOx/TiN	20 x 20 nm²
B. Govoreanu et al.	39	2011	No	Unscaled	Oxide	Electrode cross-bar	Hf/HfOx/TiN	40 x 40 nm²
J. Niu et al.	40	2016	No	Unscaled	Oxide	Electrode cross-bar	Ti/HfOx/Pt	20 x 20 nm ²
W.C. Chien et al.	41	2010	Yes	60 nm	Oxide	Via	W/WOx/TiN	Ø 60 nm
W.C. Chien et al.	42	2011	Yes	40 nm	Oxide	Via	W/WOx/TiN	Ø 40 nm
MC. Hsieh et al.	43	2013	Unknown	Unknown	Oxide	Via	Ta/TaN/TaON/Cu	Ø 30 nm
O. Golonzka et al.	44	2019	Unknown	Unknown	Oxide	Via	Ta/TaOx/unknown	Ø 100 nm
B. Govoreanu et al.	45	2011	Unknown	30 nm	Oxide	Electrode cross-bar	Hf/HfOx/TiN	$10 \times 10 \text{ nm}^2$
G. S. Kar et al.	46	2012	Unknown	30 nm	Oxide	Electrode cross-bar	Hf/HfOx/TiN	< 20 x 20 nm ²
KS. Li et al.	47	2014	No	Unscaled	Oxide	Sidewall technology	TiN/HfOx/TiOx/TiN	< 1 x 3 nm ²
S. Pi et al.	48	2019	No	Unscaled	Oxide	Sidewall technology	Pt/TiOx/HfOx/Pt	2 x 2 nm²
E. Cha et al.	49	2013	No	Unscaled	Oxide	3D-via-integration	Ta/TaOx/TiN	10 nm x Ø200 nm
M. Yu et al.	50	2016	Yes	50 nm	Oxide	3D-via-integration	Ta/TaOx/Pt	50 nm x Øunknown
HY. Chen et al.	51	2013	No	Unscaled	Oxide	3D-via-integration	TiN/HfOx/Pt	5 nm x Ø1 μm

Fig. S1: Tabular overview of the literature on nano-scaled memristive devices. '*' marks values that are inferred, but not directly reported in the reference. For examining the immediate lateral filament surrounding, it was assumed that the filament is located in the device center with a filament diameter of 10 nm. In this work, the filament is directly embedded in SiN due to lateral oxide scaling to 10 nm.



Fig. S2: AFM depth profile scan across a planarized 2.4 μm wide trench. The pronounced height dip of 2 nm originates from higher material removal rate around the 10 nm electrode fins lining the circumference of the trench. Undesirable CMP-dishing with excessive removal of insulating material from the trench center is prevented.



Fig. S3: I-V sweeps of a reference micro-device. The parametrized 50 x 50 (CC, V_{reset,stop}) control parameter conditions are grouped into a coarser 6 x 6 grid for better visibility. V_{reset,stop} values increase from left to right along a given row. Current compliance values increase from bottom to top along a given column. Current axis limits of each row are adjusted according to CC-value.



Fig. S4: I-V sweeps of an oxide nano-fin device. The parametrized 50 x 50 (CC, V_{reset,stop}) control parameter conditions are grouped into a coarser 6 x 6 grid for better visibility. V_{reset,stop} values increase from left to right along a given row. Current compliance values increase from bottom to top along a given column. Current axis limits of each row are adjusted according to CC-value. Higher applied reset voltages are needed for successful resets due to voltage drop across nano-scaled electrodes. The I-V sweeps are less variable than the reference micro-device.



Fig. S5: Comparison of the extracted median resistance states after RESET-sweep from all 2,500 control parameter conditions for the reference micro-device and the oxide nano-fin device. Resetstop-voltages of > 1.6 V are needed for successful RESET of the nano-fin device. However, the microdevice needs higher reset-stop-voltages than the nano-fin to reach comparably high HRS.



Fig. S6: The histogram of current jumps for the nano-fin (orange) overlaps with the reference devices when including traces with worse signal-to-noise ratios (SNR). Shown here are the best 50 % traces in regards to SNR.



Fig. S7: The current-normalized power spectral density (PSD) of the nano-fin (orange) continuously approaches the reference devices for traces with worse SNR. Shown here are the best 50 % traces in regards to SNR.



Fig. S8: Schematic illustration of (a) an unconfined reference filament in a large oxide volume (purple) and (b) a confined filament in a small oxide volume that is laterally encapsulated in both dimensions by a diffusion barrier (green). The filaments are depicted as an accumulation of oxygen vacancies (gray spheres). The unconfined filament is larger as it is not laterally restricted. On the contrary, the confined filament is smaller due to its lateral boundary from the surrounding diffusion barrier.





Fig. S9: Schematic illustration comparing the oxygen vacancy (gray) distributions in an unconfined (a) and confined (b) filament. The oxygen vacancies form the filament and enable the conduction of current between the ohmic and the active electrode in our simulation. Lateral confinement by a surrounding diffusion barrier (green) results in a thinner filament. For the same resistance state, the thin confined filament has a higher oxygen vacancy concentration and a smaller gap between filament and the active electrode.



Fig. S10: Equidistant measurement time steps of the source-measure-unit compared with the eventdriven time steps of the KMC simulation. Each KMC time step contains one vacancy diffusion instance with a respective current amplitude change. The measured time steps superimpose the current change of several vacancy diffusion instances occurring in the given time frame.