Supporting Information

Physical Reservoirs based on MoS_2-HZO Integrated Ferroelectric Field-effect Transistors for Reservoir Computing Systems

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S1. Demonstration of 1D-FeFET array

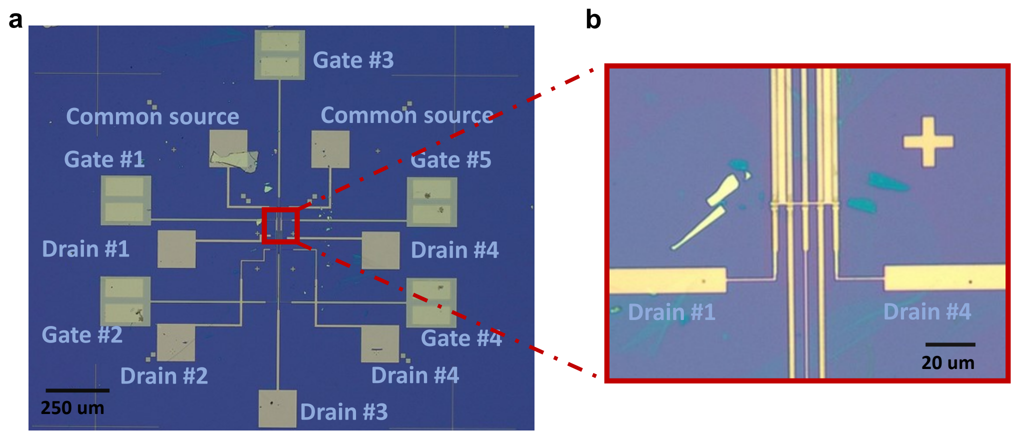

Fig. S1 (a) Microscopic image of the device array utilized in this study, with a scale bar of 250 µm. (b) Zoomed-in view highlighting the flake isolation.

S2. EDX results of MoS_2-HZO FeFETs

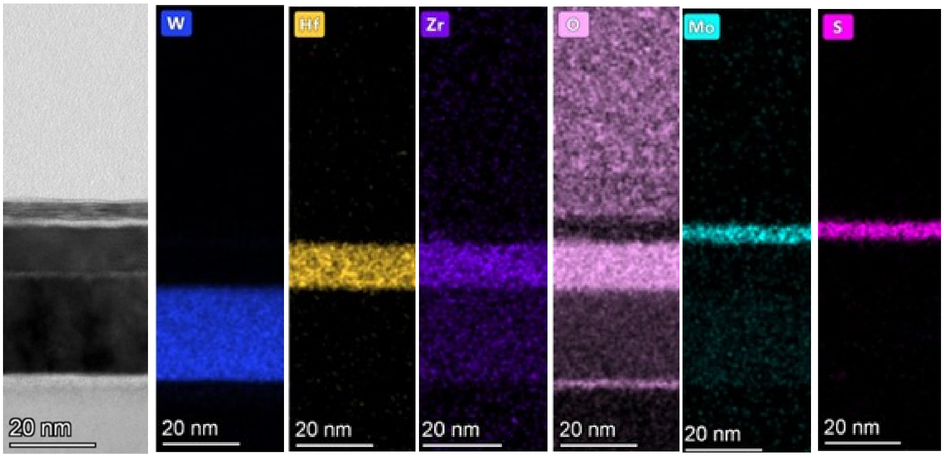

Fig. S2 EDX map comprises W, Hf, Zr, O, Mo, and S elements.

S3. FORC measurement schedule

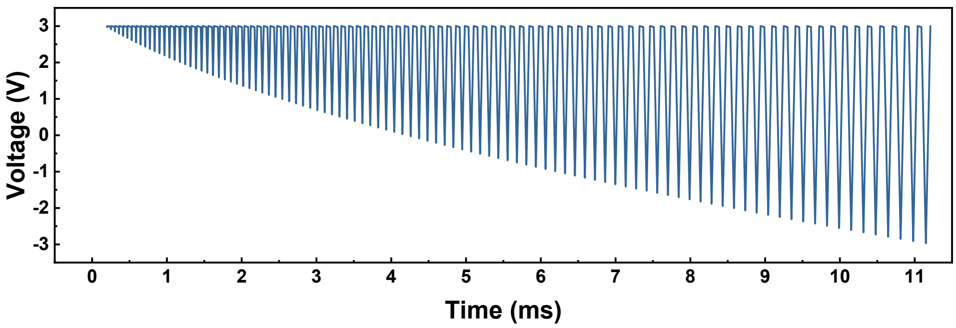

Fig. S3 Electric field for the FORC measurement using MFM capacitor. The reversal electric field (E_r) changes from 3.0 to -3.0 V with a step of -0.01 V, and the external field descends from 3.0 V to E_r, and then ascends to 3.0 V.

S4. Switching current for the NLS model fitting

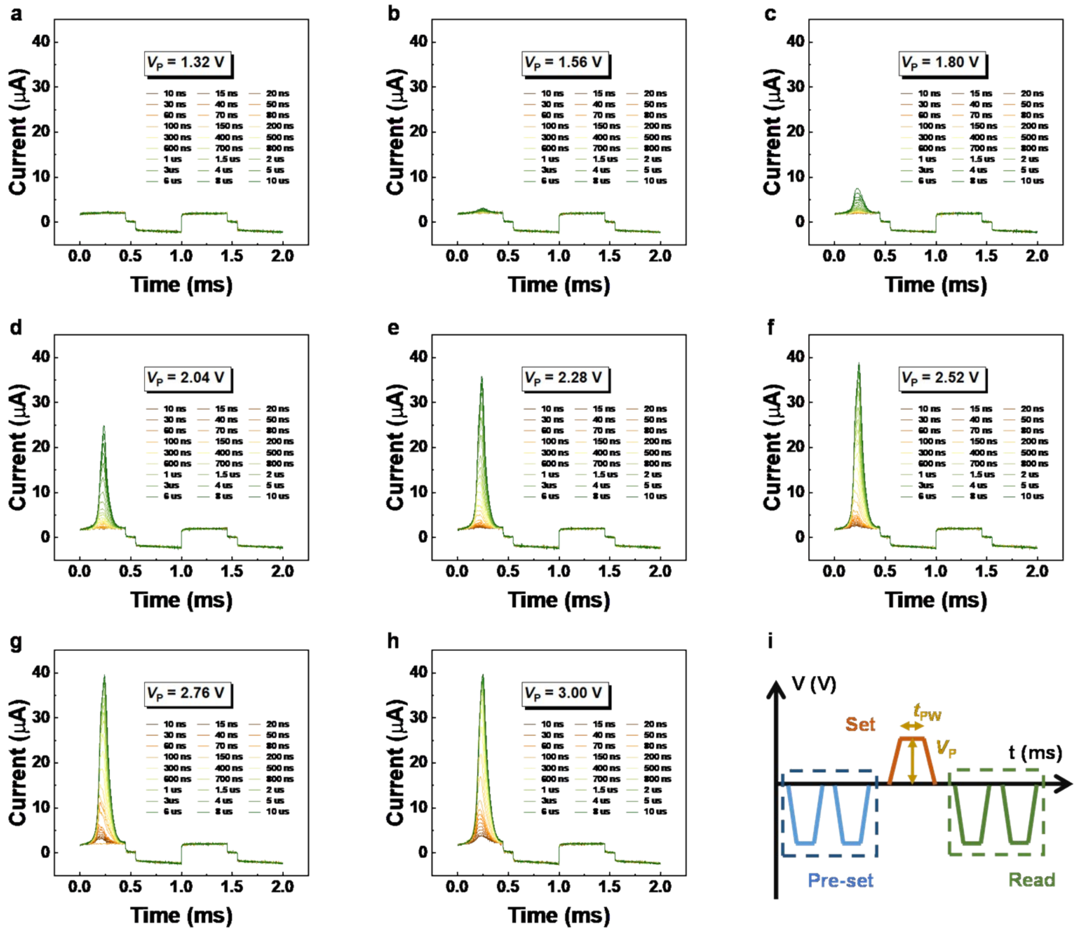

Fig. S4. Switching current at different program voltage (V_P) with varying programming duration (t_P). (a) - (h) The V_P changes from 1.32 to 3.00 V, with a step of 0.24 V, and the t_P varies from 10 ns to 10 μs for each V_P. (i) Illustration of the switching current measurement setup.

S5. Deconvolution of varied results with different ozone pulse time

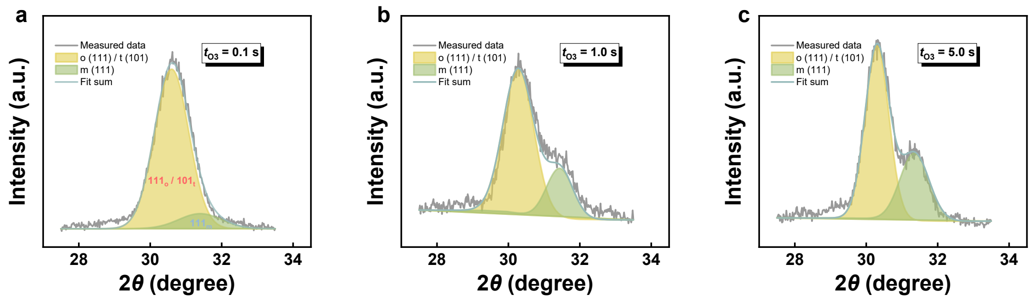

Fig. S5 Deconvoluted XRD results in the 2θ range of 27.5°-33.5° varied from t_{O3} of a) 0.1 s, b) 1.0 s, and c) 5.0 s.

S6. Long accumulation of response currents

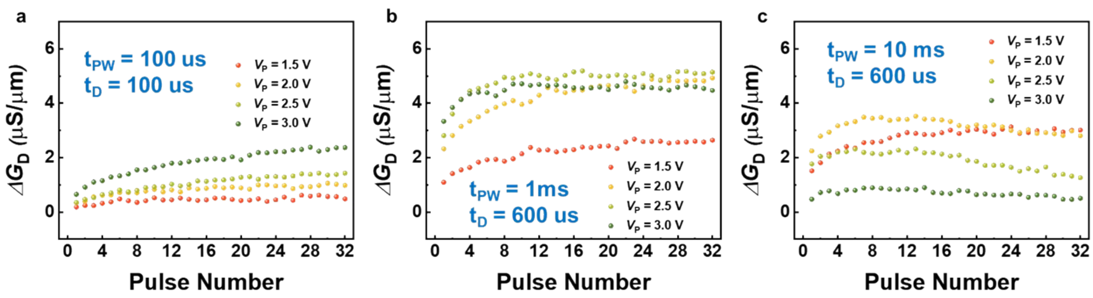

Fig. S6 Synaptic behavior by modulation of the conductance states with the pulse trains. Identical programming bias (V_P) is introduced from 1.5 V to 3 V for all the input pulse scheme. The read voltage (V_R) of 0.5 V with V_D = 0.5 V is fixed to all the input pulse trains. (a) t_{PW} = 100 µs, t_D = 100 µs (b) t_{PW} = 1 ms, t_D = 600 µs and (c) t_{PW} = 10 ms , t_D = 600 µs.

One can observe that when we apply a short program pulse width (t_{PW}), the conductance difference (ΔG_D) significantly increase with higher programming gate bias (V_P). These observations indicating that more dipolar switching in the HZO ferroelectric layer under larger voltage. On the other hand, when we further increase the t_{PW}, the ΔG_D will not be directly proportional to the magnitude of V_P, which can be attributed to the serious trapping effect reduce the current. When we further increase the t_{PW}, the electron trapping become seriously which led the ΔG_D smaller. This experimental result is consistent with previous reports [1–4] that the ferroelectric response is faster than the trapping response.

S7. Critical Role of Interfacial Layer Al_2O_3

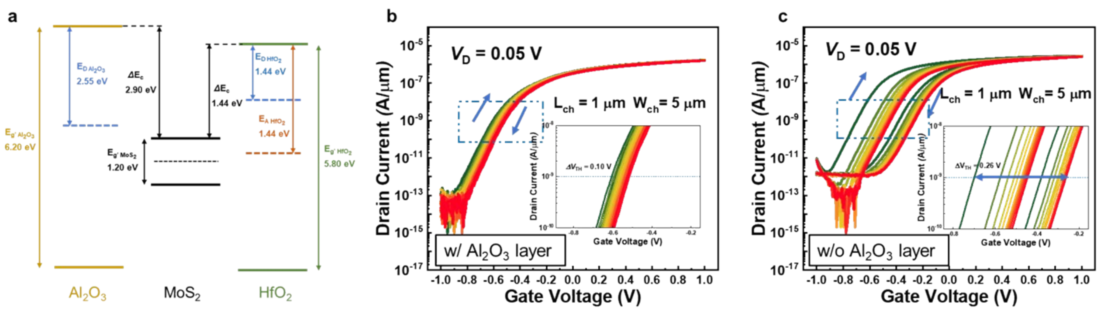

Fig. S7. (a) Energy band diagrams showing the band alignment of few-layer MoS_2 to the high-k dielectric layer of Al_2O_3 and HfO_2.[5–7] The accurate value of bandgaps, defect levels and band offsets were reported by several previous reports which extracted from the experiments. Transfer characteristics with f = 0.5 Hz at V_D = 50 mV and V_G from -1.0 V to 1.0 V for MoS_2 FETs (b) with and (c) without 2 nm Al_2O_3 interface layer on 10 nm HZO layer.

The transistor performance will be affected by the interfacial interaction between MoS_2 and the high-k dielectric layer. In this work, we use a thin Al_2O_3 layer (~2 nm) works as the interfacial layer between MoS_2 and the ferroelectric HZO layer to minimize the detrimental charge trapping effect. As shown in the depicted energy band diagrams (**Fig. S7a**), the acceptor-like traps (dark red) of HfO_2 are adjacent to the MoS_2 intrinsic Fermi level which energetically favorable to charge trapping effect. Compared with HfO_2, the oxide defect states in the energy band of Al_2O_3 shows the energy difference with the conduction band of MoS_2 which lead the detrimental charge trapping difficult and will lower the oxide trap density. Therefore, the depicted energy band diagrams confirm that the Al_2O_3 align well with the MoS_2 so that suitable for the transistors.

Subsequently, the MoS_2 FETs with or without Al_2O_3 interface layer are fabricated to verify the aforementioned deduce. Note that all the process except the Al_2O_3 deposition was conducted together for these two samples. Then the same measurement scheme at V_D of 50 mV and the sweeping frequency (f) of 0.5 Hz was used for the devices. One can observe that the extracted clockwise hysteresis ΔV_{TH} from the device with Al_2O_3 interface layer is much smaller (~0.10V), while the ΔV_{TH} is 0.26 V of the device without Al_2O_3 over the same voltage range. Therefore, we have validated that address the interfacial interaction between MoS_2 and the high-k dielectric layer by Al_2O_3 interface layer is suitability.

S8. MoS_2 FETs with pure Al_2O_3 gate stack

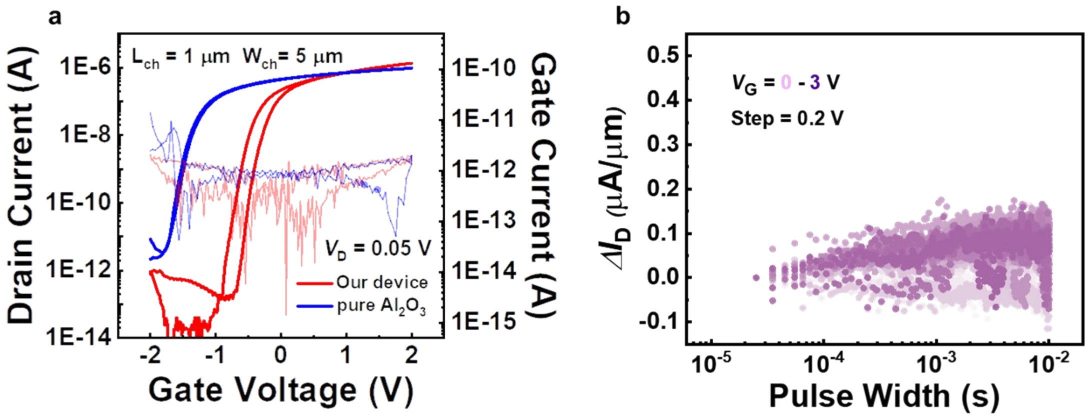

Fig. S8. (a) Transfer characteristics and gate leakage current at V_D = 50 mV and V_G from -2.0 V to 2.0 V for MoS_2 FETs using 12 nm pure Al_2O_3 or 2 nm Al_2O_3 stacks with 10nm HZO layer with *f* of 0.50 Hz. (b) The dynamic voltage response under a 3.0 V input pulse trains with t_{PW} = 100 μs and t_D = 100 μs.

It is evident that the device based on pure Al_2O_3 shows a considerably smaller transient drain current compared to the HZO-based device, as shown in Fig. 2e. It confirms that the dynamic behavior observed is attributed to the ferroelectric HZO rather than the interfacial layer Al_2O_3. Furthermore, the smaller V_{TH} in our device can be attributed to enhanced electrical control.

S9. CV characteristics of the HZO/Al_2O_3 capacitor

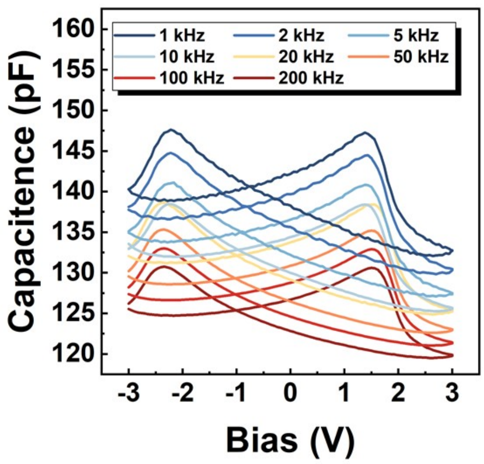

Fig. S9. The frequency-dependent capacitance-voltage (CV) characteristics of HZO/Al_2O_3 capacitor in similar MFM structure as in Fig. 1f. The thicknesses of HZO and Al_2O_3 are 10 nm and 2 nm, respectively.

References

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