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Electronic Supplementary Information

Two-dimensional MoSi$_2$As$_4$-based field-effect transistors integrating switching and gas sensing functions

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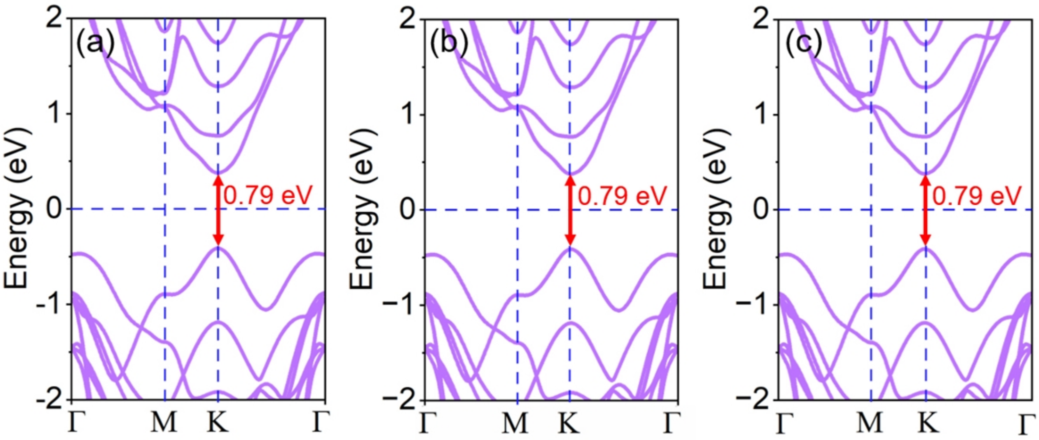

Figure S1. The band structure of monolayer MoSi$_2$As$_4$ with the *k*-point samplings of (a) $33 \times 1 \times 33$, (b) $35 \times 1 \times 35$, and (c) $37 \times 1 \times 37$, respectively.

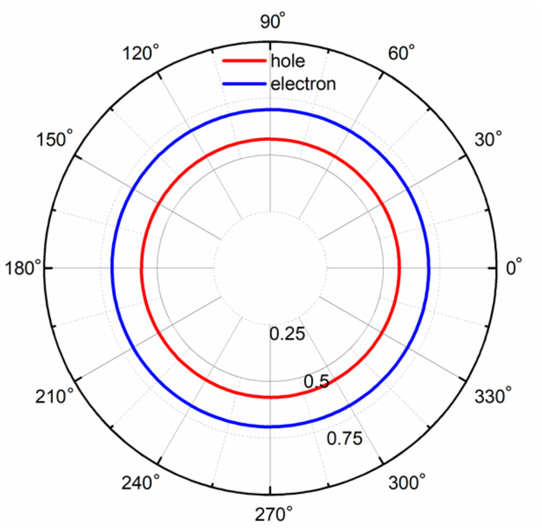

Figure S2. Polar plot of the electron and hole effective mass for the $MoSi_2As_4$ monolayer; 0° and 90° represent the zigzag and armchair directions, respectively.

Table S1. The effective mass (m^*) and carrier mobility (μ) of the monolayer $MoSi_2As_4$. m_0 is the electron mass.

	Carrier type	m^* (m_0)	μ ($cm^2V^{-1}s^{-1}$)
$MoSi_2As_4$	electron	0.70	243
	hole	0.57	1050

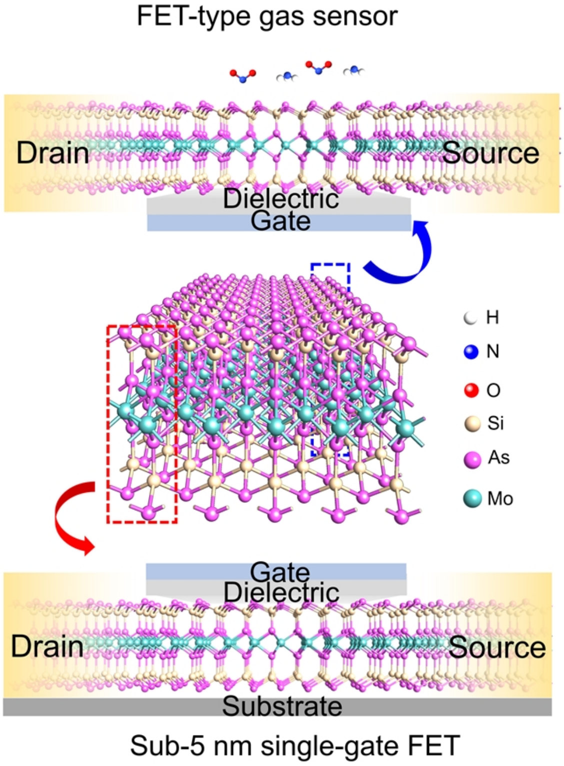

Figure S3. The schematic diagram of the $MoSi_2As_4$-based FET and FET-type gas sensor.

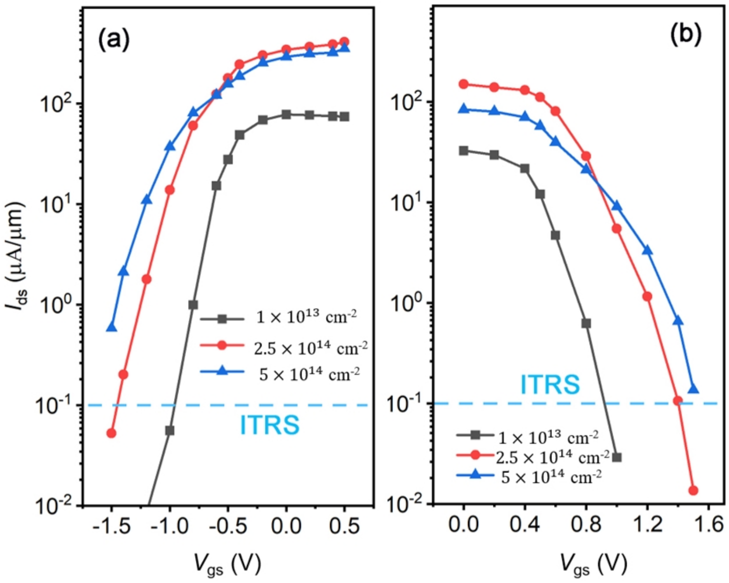

Figure S4. The transfer characteristics of SG (a) *n*-type and (b) *p*-type 5 nm gate-length MoSi$_2$As4 FET without underlap structure at different doping concentration.

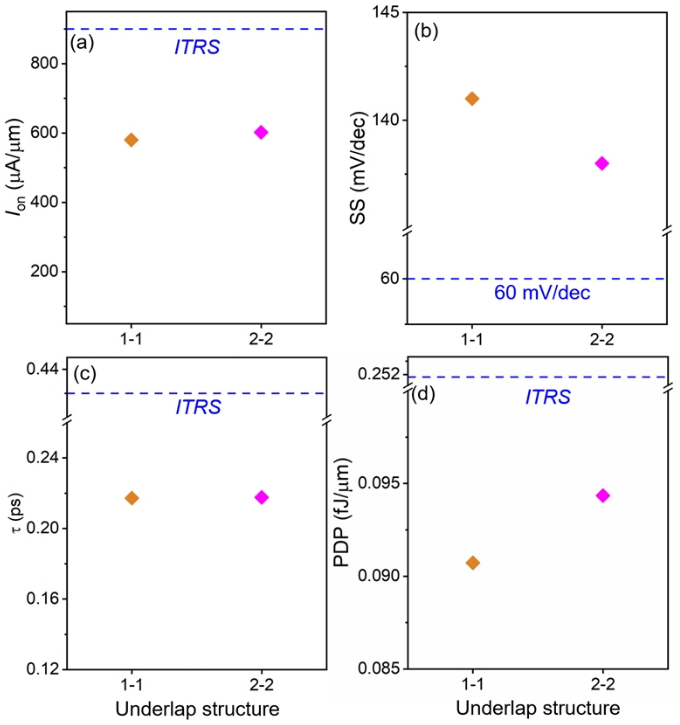

Figure S5. (a) On-state current (I_{on}), (b) subthreshold swing (SS), (c) delay time (τ), and (d) power dissipation (PDP) of SG *n*-type 5 nm gate-length MoSi$_2$As$_4$ FET with different underlap structures. The blue dashed lines represent the ITRS for HP requirements. The underlap structures "N-N" represent the parts of UL$_1$= UL$_2$=N nm.

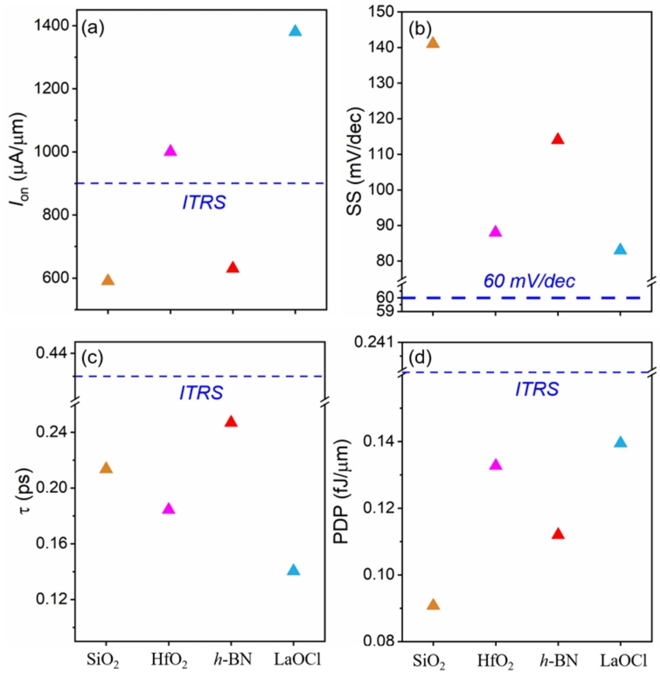

Figure S6. (a) On-state current (I_{on}), (b) subthreshold swing (SS), (c) delay time (τ), and (d) power dissipation (PDP) of SG *n*-type 5 nm gate-length $MoSi_2As_4$ FET with SiO_2/ HfO_2/*h*-BN/LaOCl dielectric material. The blue dashed lines represent the ITRS for HP requirements.

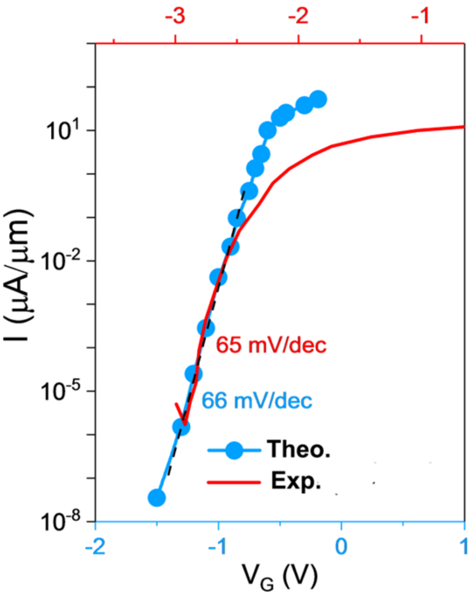

Figure S7. Benchmark of the simulated transfer characteristic against the experimental one for the 1 nm gate-length 2D MoS_2 transistors.[1]

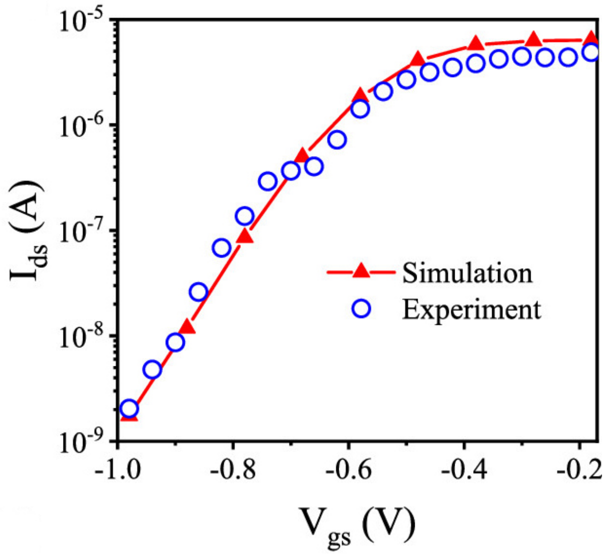

Figure S8. Experimental transfer characteristic of the 1.3 nm-diameter CNT FET with 5 nm gate length against the simulated data based on first-principles quantum transport calculations of the single-gate (8, 0) CNT-based FET.[2]

Table S2. The comparison of the performance of the FETs between the experiments and theories using the DFT+NEGF method. The theoretical results represent the performance limit of the FETs. SS: subthreshold swing; I_{off} and I_{on} are the off-state and on-state current; τ: delay time; PDP: power dissipation; EDP: energy-delay product.

Channel material	Gate length	Performance	Method	Value	Reference
MoS_2	1 nm	SS (mV/dec)	Experiment	65	1, 3, 4
			DFT+NEGF	66	
		I_{on} (μA/μm)	Experiment	250	
			DFT+NEGF	519	
Carbon nanotube	5 nm	I_{off} (μA/μm)	Experiment	50	2, 5
			DFT+NEGF	50	
		I_{on} (μA/μm)	Experiment	1412	
			DFT+NEGF	1775	
		τ (fs)	Experiment	46	
			DFT+NEGF	26	
		PDP (fJ/μm)	Experiment	0.026	
			DFT+NEGF	0.018	
		EDP (Js/μm)	Experiment	1.2×10^{-30}	
			DFT+NEGF	0.5×10^{-30}	

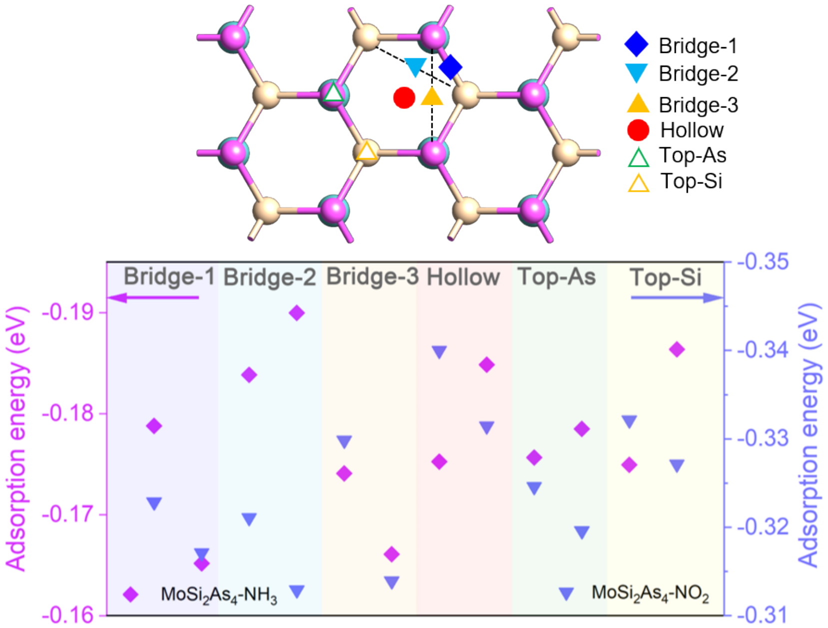

Figure S9. The adsorption sites and adsorption energy of the NH_3 and NO_2 adsorbed $MoSi_2As_4$.

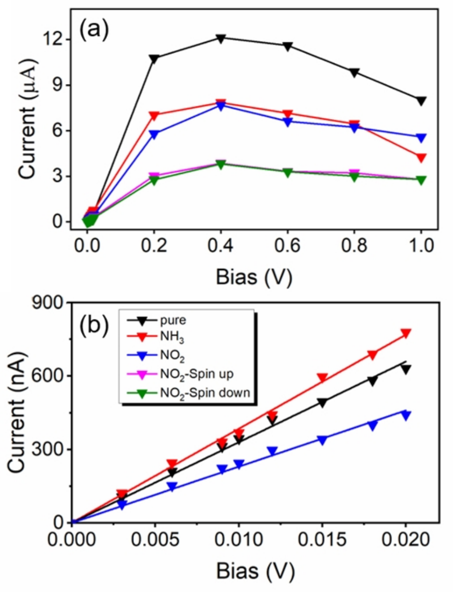

Figure S10. (a) The current as a function of bias voltage and (b) the current as a function of bias voltage within a low bias range of the $MoSi_2As_4$ sensor before and after adsorbing of NH_3 or NO_2.

References

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