Supporting Information

Integrated 4-terminal Single-Contact Nanoelectromechanical Relays Implemented in a Silicon-On-Insulator Foundry Process

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Table S1. Comparison of the state-of-the-art 4-T relays

REFERENCE	**[1]**	**[2]**	**[3]**	**[4]**	**[5]**	**[6]**	**THIS WORK**
Architecture	out-of-plane four contacts	out-of-plane two contacts	in-plane two contacts	out-of-plane one contact	in-plane one contact	in-plane one contact	**in-plane one contact**
Structural material	poly-$Si_{0.4}Ge_{0.6}$	poly-$Si_{0.4}Ge_{0.6}$	poly-Si	Ni	Si	Si	**Si**
Dielectric plug material	Al_2O_3	Al_2O_3	HfO_2	SU8	nLof	AlOx	**AlOx**
Footprint	111 × 82 μm^2	76 × 53 μm^2	25 × 10 μm^2	620 × 620 μm^2	237 × 70 μm^2	25 × 10 μm^2	**25 × 10 μm^2**
Actuation gap	200 nm	200 nm	440 nm	1.4 μm	1.5 μm	300 nm	**300 nm**
Contact gap	100 nm	100 nm	340 nm	1 μm	1 μm	200 nm	**200 nm**
Contact material	W + TiO2 (3Å)	W	TiN	Au	NCG	Au	**Au**
Pull-in voltage	~ 6 V	~ 7 V	31 V	23-30 V	25 V ($V_B = -10$ V)	11.6 V	**7.8 V (V_B =-8 V)**
Fabrication Complexity	Four-mask	Four-mask	Three-mask	Seven-mask	Three-mask	Three-mask	**Three-mask**
Integrated Metal interconnects	No	No	No	No	No	No	**Yes**

1. Characterization of the 4-T NEM relays with different contact sizes

We actuated six 4-T NEM relays (marked as devices sw0 to sw5) by ramping the gate voltage up and down, taking care to avoid over-drive. The measurement result for device sw0, the contact of which is fully covered with Au, has been shown in Figure S1a. Devices sw1 to sw5 are relays with contacts that were to 50% (half-tip) covered with Au. We measured devices sw1, sw2 and sw3 under a 10 nA current limit, as shown in Figure S1b. A clear pull-in was detected on all three relays, but we did not detect a pull-out. Then, we lowered the current limit during the actuation of devices sw4 and sw5 to 1 nA, as shown in Figure S1c, clear pull-in and pull-out were repeatably demonstrated. The pull-in voltages of all six relays were in a range of 16 V $\pm$ 2 V, as shown in Figure S1d.

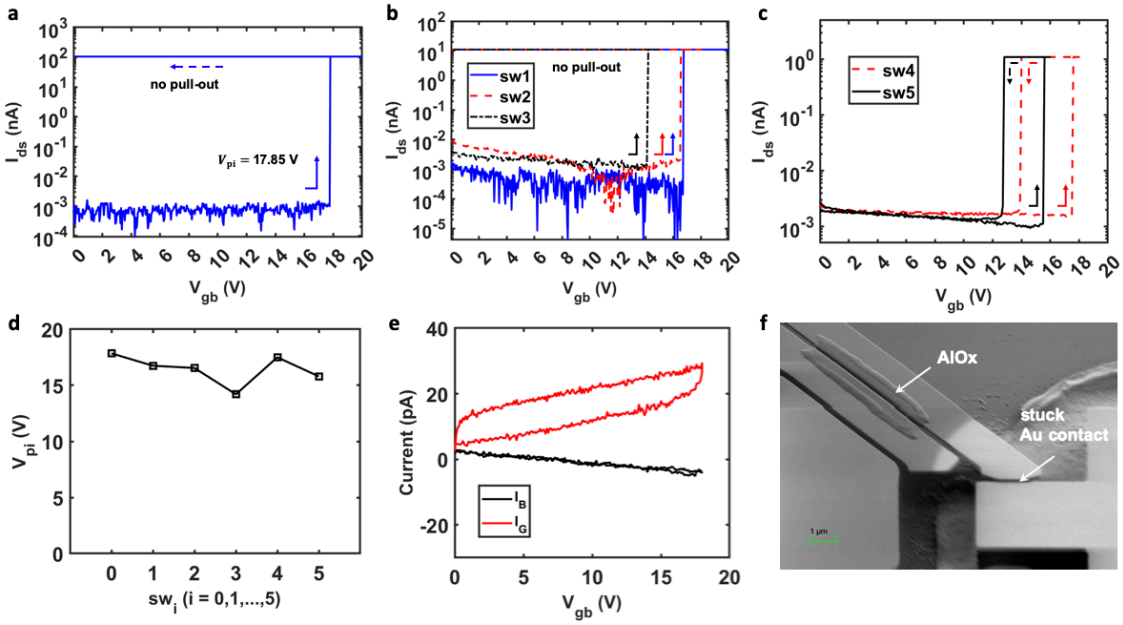

Figure S1. (a) Measured actuation of an integrated 4-T NEM relay with a full contact tip Au metallization. The relay shows pull-in at 17.85 V, but no pull-out. (b) Actuation of devices sw1, sw2 and sw3 with half-tip metallization under 10 nA current limit. (c) Actuation of devices sw4 and sw5 with half-tip metallization under 1 nA current limit. (d) Summary of the pull-in voltages of the measured six 4-T NEM relays. (e) Measured current through Body and Gate versus gate voltage of device sw4. (f) SEM image of the full-tip 4-T NEM relay imaged after failure (contact is stuck).

Notably, there is no current flowing through the *Body* electrode during actuation (see Figure S1e), indicating effective electrical isolation between the *Source* and *Body* electrodes. Moreover, we inspected device sw0 by SEM imaging after the Au contact became stuck (Figure S1f), showing that the two suspended beams of the relay remain firmly connected by the AlOx plug without observable stress-induced bending, despite the relatively thin AlOx layer forming the plug.

In our demonstration we selected Au as NEM relay contact material as it is a working solution that was readily available in our lab. Based on our prior experience with NEM relays with Au contacts fabricated on the same platform, the contact resistance typically falls within a range of 250-550 MΩ. Unlike RF MEM relays, where achieving a contact resistance lower than 1 Ω is important for minimizing insertion loss, NEM relays for logic applications can tolerate much higher contact resistances due to the fact that the operating speed of digital circuits is primarily limited by the mechanical switching delay of the relay rather than the electrical charging delay "RC"[7]. In practical digital circuit applications, the required load current capacity for a NEM relay can be estimated by considering a representative load and the minimum time needed to charge the gate capacitance to the rail voltage. In a NEM relay-based circuit with two to four relays and a fanout of four gates, a representative capacitive load is approximately 1 to 2 fF. To ensure compliance with mechanical switching time constraints (assuming an RC time constant < 100 ns) at a rail voltage of 5 V, driving currents of the order of 100 nA are needed. This requirement translates to acceptable NEM relay contact resistances of the order of 50 MΩ.

2. Post-processing of iSiPP50G foundry wafers for completion of relay fabrication

After the NEM relays have been structured, the wafers were diced into 23 mm × 23 mm chips. Following post-processing steps described below were conducted at chip-level in the university lab.

AlOx patterning

After the SiPP50G wafer was completed and delivered by the foundry, a 70 nm thick layer of AlOx was deposited on the wafer surface (Figure 2b, step II). Next, the AlOx layer inside the NEM cavities was locally etched in the areas of the relay structures to allow the sacrificial release etching of the relays in a later step. The AlOx inside the NEM cavities was etched using wet buffered hydrofluoric acid (BHF) (see Figure S2a, step i). Thereafter, the AlOx layer in the areas above the metal pads was locally removed using a dry etching process (see Figure S2a, step ii). Dry etching was used in the step because we observed that the BHF etching solution could roughen or alter the metal surfaces of the metal pads.

Partial tip metallization

To reliably metallize the relay tips and avoid any short-circuit connection during the metal deposition process, we first performed a partial release with a vapor HF (vHF) etching step to create a partial (~150 nm) undercut below the relay structures (see Figure S2a, step iii, the full release of the 4-T NEM relays requires at least 1.6 μm of undercut). Then, we placed a resist lift-off mask with a window opening above the pre-defined (full/half) tip contact area of the NEM relays. Subsequently we deposited a thin layer of Au on the chip using a physical vapor deposition (PVD) process on the chip (using an 844GT system supplied by KDF Orangeburg, New York system). In a final lift-off step the Au was patterned so that it only covered the tip contacts of the relay structures. For the lift-off process we used SPR 700 and LOR 5A (both purchased from MICROPOSIT™, Germany) as photoresist (PR) and the lift-off resist (LOR), respectively. Before the resist coating the chip was baked at 200 °C for 10 min with a hotplate for dehydration. Then, the LOR 5A was coated at 4000 rpm with a spin-coater, and then baked at 170 °C for 3 min. After that, a layer of SPR 700 was spin-coated at 4500 rpm on top of the LOR 5A, and then pre-baked at 100 °C for 1 min before the exposure. Subsequently, after alignment, two lithography exposure steps were performed at doses of 170 $\mathrm{mJ/cm^2}$, but with

defocus value set at 9 and 0, respectively, to obtain straight side-walls on the resist double-layer at the bottom of the NEM cavities.

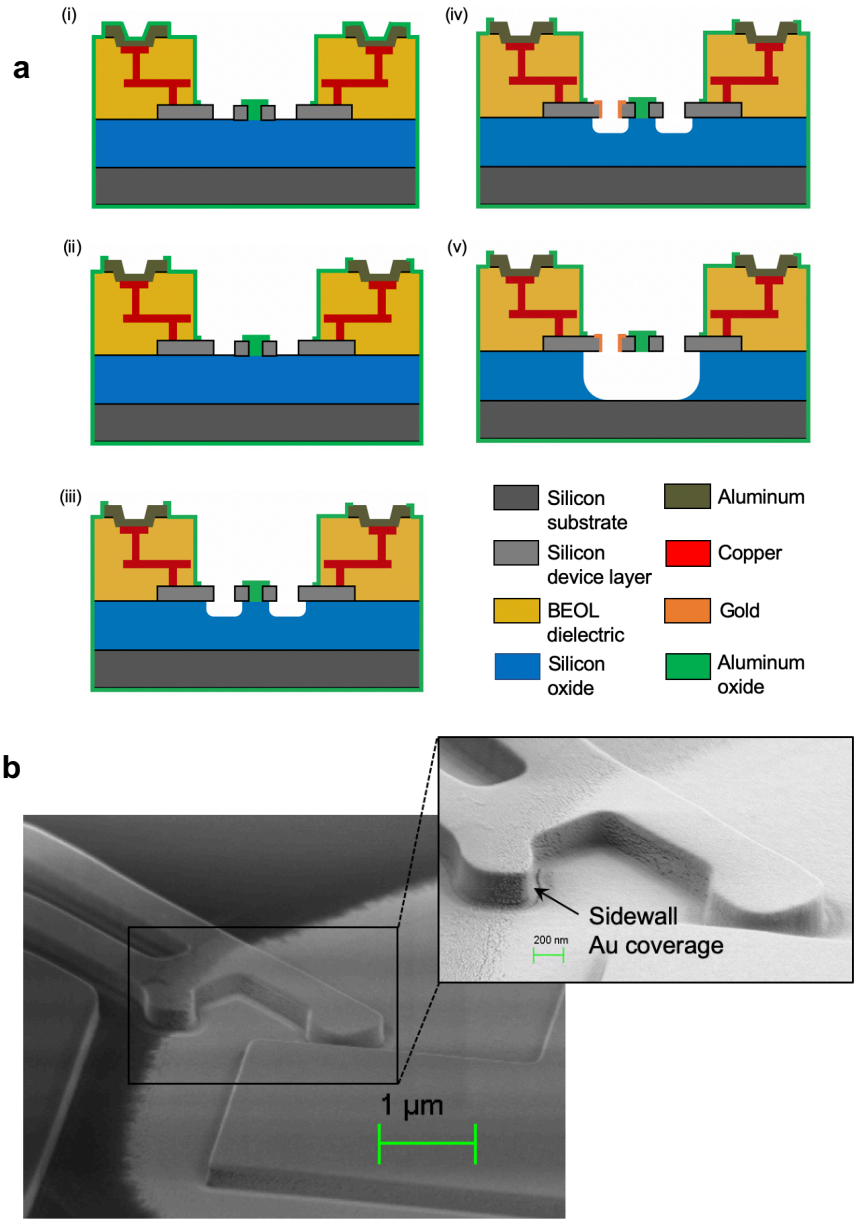

Figure S2. (a) Schematic cross-section of the wafer post-processing flow. (i) Etching the $AlOx$ inside the MEMS cavity by BHF; (ii) Etching the AlOx on top of the pads by vHF; (iii) Partial release of the NEM relay structures; (iv) NEM relay contact metallization with Au using a lift-off process; (v) Release etch to produce fully suspended 4-T NEM relays. (b) SEM image of the Au contact coating on a NEM process characterization structure. The distinctly visible color transition between the Si and Au surfaces within the enlarged SEM image shows the Au coverage of the sidewalls.

After exposure, the chip was post-baked at 110 °C for 1 min, and then developed using CD26 (purchased from MICROPOSIT™, Germany) for 100 s to create an ~ 1.5 μm undercut in the LOR layer. In the lift-off process, Acetone was used first to remove the extra Au and the PR layer, at room temperature. Then, the chip was immersed into the heated (60 °C) remover

REM 700 (purchased from MICROPOSIT™, Germany) for 30 min, to dissolve the LOR layer and perform the lift-off (see Figure S2a, step (iv)). Figure S2b shows the Au coverage of the sidewalls of a NEM process evaluation structure that was fabricated at the same time and on the same wafer as the 4-T NEM relays. In our PVD Au deposition process, the estimated ratio between sidewall coverage and top surface coverage is about 0.4, resulting in an expected sidewall layer thickness of approximately 30 - 35 nm when depositing an 80 nm thick layer of Au on the top surface.

3. 2D Schematic and geometric parameters of the 4-T NEM relay design

Our in-plane Si 4-T NEM relay design is illustrated in Figure S3, and the detailed relay design parameters are listed in Table S2. Generally, 4-T NEM relay designs with low pull-in voltages are desired because the dynamic energy consumed per binary switching transfer is directly proportional to CV^2, where C represents the gate capacitance, and V the voltage swing across the gate. Our 4-T NEM relay design shares a common architecture with the micro-scale 3-T and 4-T relays presented previously[5], but distinguishes itself by substantially scaled-down dimensions and an AlOx dielectric plug. Notably, the dielectric AlOx plug does not significantly affect the mechanical characteristics and the pull-in behavior of the NEM relay. Therefore, the resulting pull-in voltages of 3-T and 4-T relays based on this architecture adhere to the same set of design principles, which have been comprehensively analyzed using finite element analysis[5].

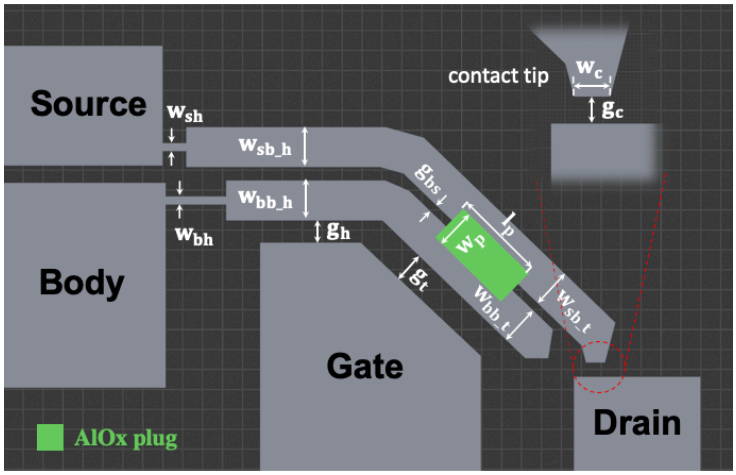

Figure S3. 2D illustration of the in-plane 4-T NEM relay realized in an SOI foundry process (the AlOx plug is shown in green).

Table S2. Design parameters of the 4-T NEM relay

Parameters	**Size**
Silicon device layer thickness	220 nm
Source hinge width w_{sh}	200 nm
Body hinge width w_{bh}	200 nm
Body-gate airgap horizontal g_{h}	300 nm
Body-gate airgap tilted g_{t}	350 nm
Source beam width horizontal $w_{\mathrm{sb\_h}}$	1.5 μm
Body beam width horizontal $w_{\mathrm{bb\_h}}$	1.5 μm
Source beam width tilted $w_{\mathrm{sb\_t}}$	1.5 μm
Body beam width tilted $w_{\mathrm{bb\_t}}$	1.5 μm
Body-source airgap g_{bs}	200 nm
Plug-length l_{p}	7.0 μm
Plug-width w_{p}	2.4 μm
Contact width w_{c}	1.0 μm
Contact airgap g_{c}	200 nm

Reference

(1) Nathanael, R.; Pott, V.; Kam, H.; Jeon, J.; Liu, T. K. 4-Terminal Relay Technology for Complementary Logic. *IEEE IEDM Tech. Dig.* **2009**, 223-226

(2) Jeon, J.; Pott, V.; Kam, H.; Nathanael, R.; Alon, E.; Liu, T. -J. K. Perfectly Complimentary Relay Design for Digital Logic Applications. *IEEE Electron Device Lett.* **2010**, Vol.31, No.4, pp. 371-373

(3) Lee, D.; Lee, W. S.; Chen, C.; Fallah, F.; Provine, J.; Chong, S.; Watkins, J.; Howe, R. T.; Wong, H. -S. P.; Mitra, S. Combinational Logic Design Using Six-Terminal NEM Relays. *IEEE Trans. Comput. -Aided Des. Integr. Circuits Sys.* **2013**, 32, 653

(4) Yoon, Y. -H.; Jin, Y.; Kim, C. -K.; Hong, S.; Yoon, J. -B. A Low Contact Resistance 4-Terminal Mems Relay: Theoretical Analysis, Design and Demonstration. *J. Microelectromech.Syst.* **2018**, 27, 497

(5) Reynolds, J. D.; Rana, S.; Worsey, E.; Tang, Q.; Kulsreshath, M. K.; Chong, H. M. H.; Pamunuwa, D. Single-Contact, Four-Terminal Microelectromechanical Relay for Efficient Digital Logic. *Adv. Electron. Mater.* **2022**, 2200584

(6) Li, Y.; Bleiker, S. J.; Edinger, P. et al. Design and fabrication of a 4-terminal in-plane nanoelectromechanical relay. *Transducers* **2023**, Kyoto, Japan.

(7) A. Peschot; C. Qian; T. J. K. Liu. Nanoelectromechanical Switches for Low-Power Digital Computing. *Micromachines*. 2015, 6, 1046-1065.