Supplemental Material for "Device Performance Limit of In-Plane Monolayer VTe$_2$/WTe$_2$ Heterojunction-Based Field-Effect Transistors"

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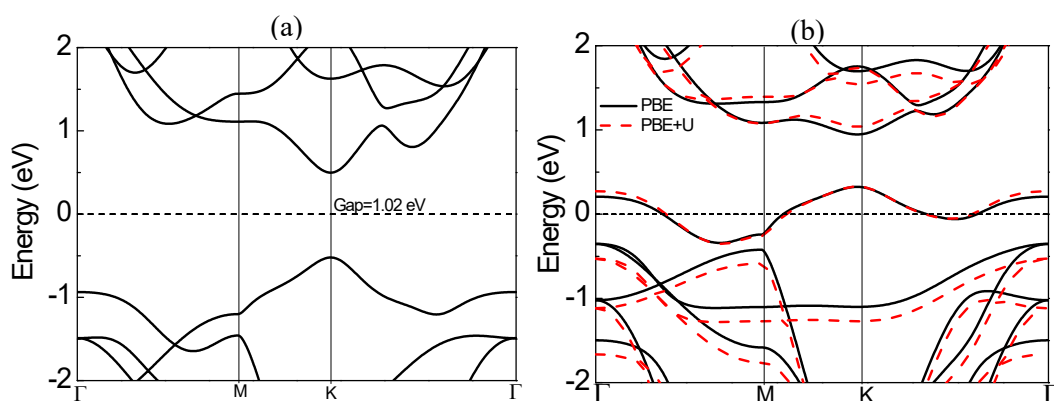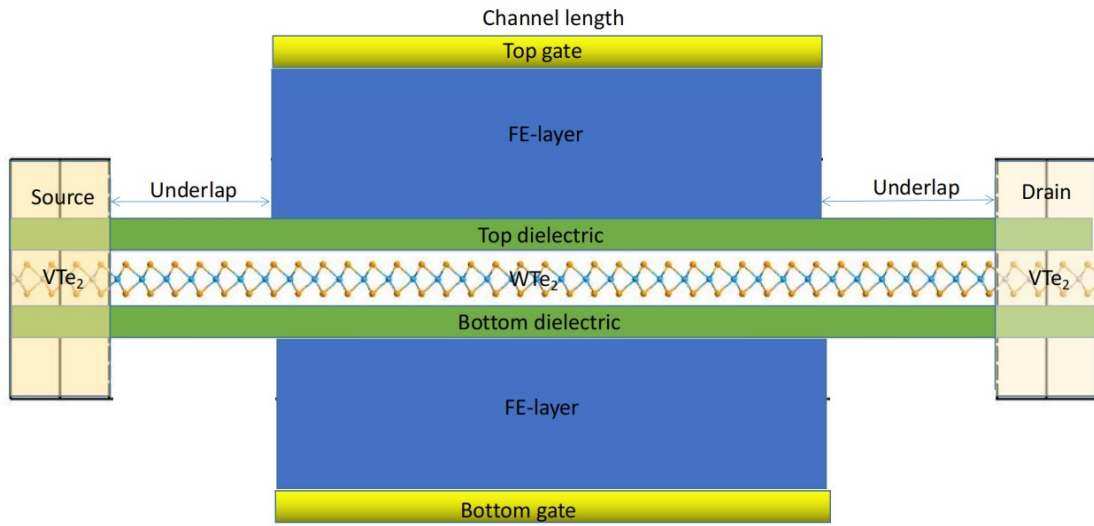
Fig. S1. (a) Band structure of monolayer WTe$_2$. (b) Band structure of monolayer VTe$_2$ by using usual PBE and PBE+U. The band structures of VTe$_2$ are only a little different using PBE and PBE+U. The value of U are fixed as 2 eV for V [Sci. Rep. 6, 32625 (2016); Phys. Rev. B 50, 16861 (1994)]. Therefore, we use PBE in this work.

Fig. S2. Schematic view of the DG-cold-source VTe_2/WTe_2-based FET devices covered by ferroelectric layers on the top and bottom gate regions.
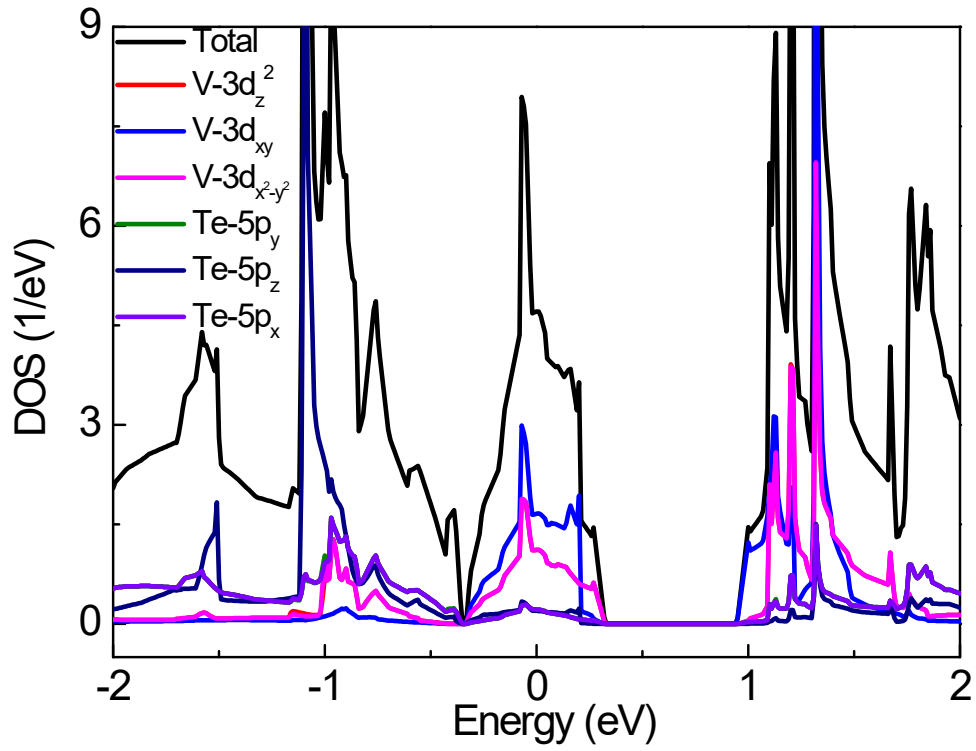
Fig. S3. The total DOS and the projected DOS of monolayer VTe_2. The numerical results show that the total DOSs are formed by $V\text{-}3d_z^2$, $V\text{-}3d_{xy}$, $V\text{-}3d_{x^2\text{-}y^2}$, $Te\text{-}5p_x$, $Te\text{-}5p_y$, $Te\text{-}5p_z$ orbits.

Table S1. The basic key parameters of the DG-cold-source VTe$_2$/WTe$_2$-based FET devices with a 5-nm L_g versus the criteria required by the 2028 needs of the ITRS 2013 for the high-performance and low-power-dissipation applications.

	L_g (nm)	U_L (nm)	SS (mV/dec)	I_{off} (μA/μm)	I_{on} (μA/μm)	I_{on}/I_{off}	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
	5	0	141	0.1	1038.63	1.04×10^4	0.22	0.41	0.27
		1	81	0.1	2573.05	2.57×10^4	0.19	0.14	0.24
		2	63	0.1	1725.78	1.73×10^4	0.13	0.14	0.16
		3	55	0.1	1149.72	1.15×10^4	0.10	0.17	0.12
	3	0	323	0.1	-	-	-	-	-
		1	168	0.1	100.13	1.00×10^3	-	-	-
HP		2	99	0.1	1329.90	1.33×10^4	0.08	0.12	0.10
		3	76	0.1	986.60	9.87×10^3	0.07	0.13	0.08
	1	1	617	0.1	-	-	-	-	-
		2	239	0.1	-	-	-	-	-
		3(o-NC)	147	0.1	456.65	4.57×10^3	0.03	0.12	0.03
		3(w-NC)	118	0.1	1035.98	1.04×10^4	0.04	0.07	0.04
	5	0	141	5×10^{-5}	-	-	-	-	-
		1	81	5×10^{-5}	-	-	-	-	-
		2	63	5×10^{-5}	434.17	8.68×10^6	0.10	0.45	0.13
		3	55	5×10^{-5}	578.42	1.16×10^7	0.07	0.25	0.09
		0	323	5×10^{-5}	-	-	-	-	-
	3	1	168	5×10^{-5}	-	-	-	-	-
LP		2	99	5×10^{-5}	-	-	-	-	-
		3	76	5×10^{-5}	0.14	1.40×10^4	-	-	-
		1	617	5×10^{-5}	-	-	-	-	-
	1	2	239	5×10^{-5}	-	-	-	-	-
		3	147	5×10^{-5}	-	-	-	-	-
ITRS HP 2028	5.1	-	-	0.1	900	9.00×10^3	0.6	0.423	0.24
ITRS LP 2028	5.9	-	-	5×10^{-5}	295	5.90×10^6	0.69	1.493	0.28

L_g: the gate length. U_L: the underlap length. SS: the subthreshold swing. I_{off}: the off-state current. I_{on}: the on-state current. C_g: the gate capacitance. τ: the delay time. PDP: the power dissipation.