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Supporting Information

Effects of Thermal Annealing on Analog Resistive Switching Behavior in Bilayer HfO_2/ZnO Synaptic Devices: The Role of ZnO Grain Boundaries

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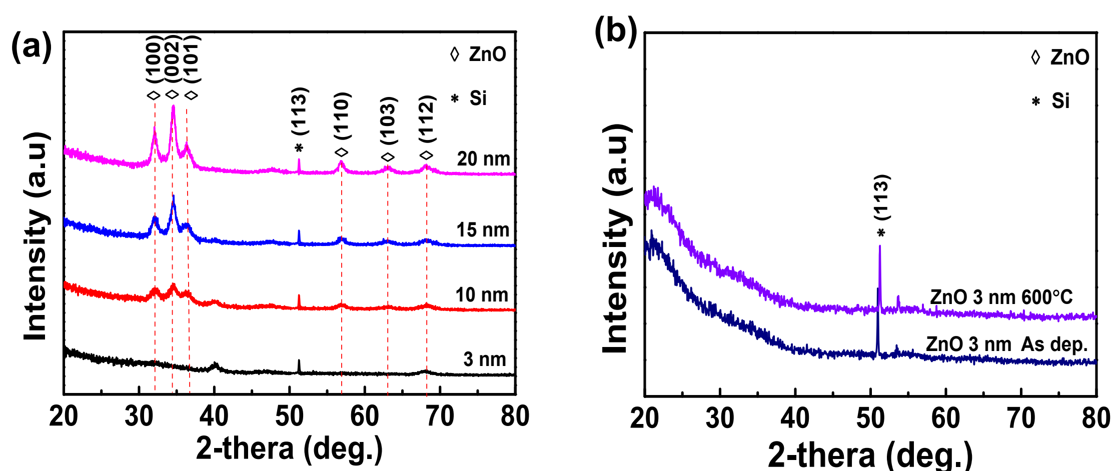

Figure S1. X-Ray diffraction spectra of (a) the active ZnO layer thickness from 3 nm to 20 nm without thermal annealing. (b) HfO_2/3 nm ZnO films on annealing temperature. All samples exhibit a common XRD peak at around 51°, which originates from the Si substrate.

Figure S1 showed the XRD diffraction spectra of the active ZnO layer thickness from 3 nm to 20 nm without thermal annealing on Si/SiO_2 substrate. The crystal orientation of the ZnO film was favored in the Z-axis direction and appeared in the (002) crystal plane. The diffraction peaks below the 10 nm ZnO films were not observed in the XRD results as shown in Figure S1(a), which means broad diffraction peaks and low signal-to-noise ratios due to the formation of amorphous and/or nanocrystalline structures in ZnO deposited samples. Also, the diffraction peaks of the HfO_2/3 nm ZnO films on annealing temperature were not observed in the XRD results as shown in Figure S1(b). Therefore, we propose XRD diffraction spectra analysis on annealing temperature at the active 10 nm ZnO film to examine the tendency of crystallization.

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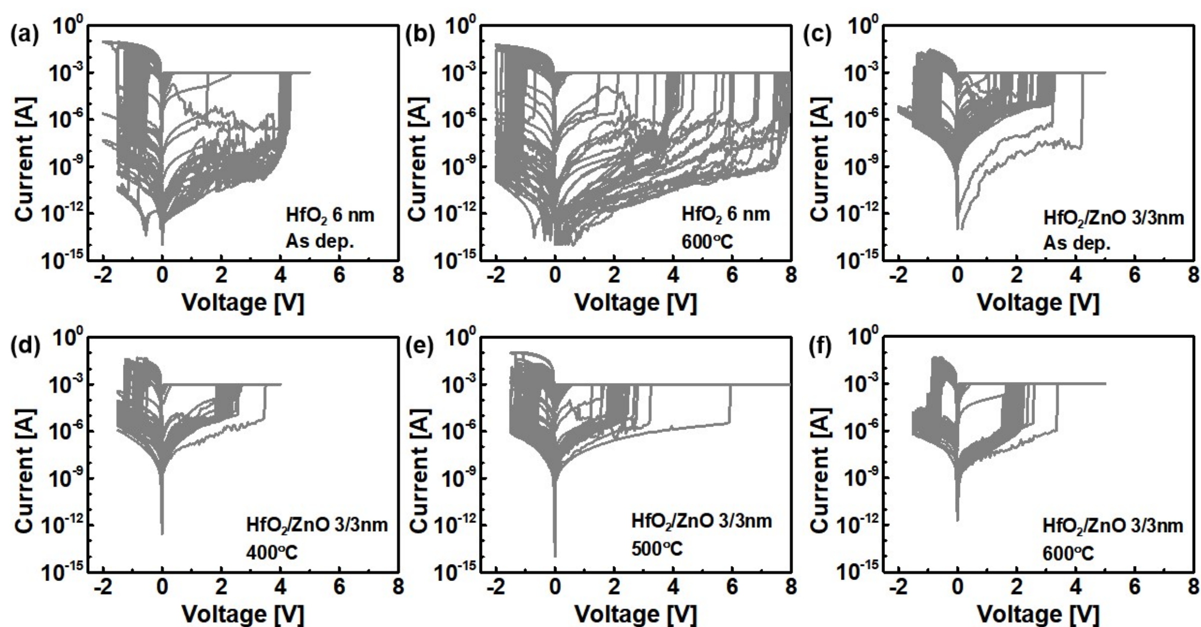

Figure S2. I-V resistive switching cycle behaviors of 40 synaptic devices for single layer (a) HfO2 and (b) within thermal annealing, bilayer HfO_2/ZnO synaptic devices (c) without and with thermal annealing at (d) 400℃, (e) 500℃, and (f) 600℃ for 1 h in an N_2 ambient.

Figure S2 shows the measured forming cycles of 40 synaptic devices for each structure. It illustrates variations between devices and extracts the initial state and low-resistance state (LRS). In Figure 4, the uniformity of HfO_2/ZnO bi-layer synaptic devices is shown to be superior to that of HfO_2 single-layer synaptic devices. Additionally, an increase in annealing temperature correlates with improved performance.

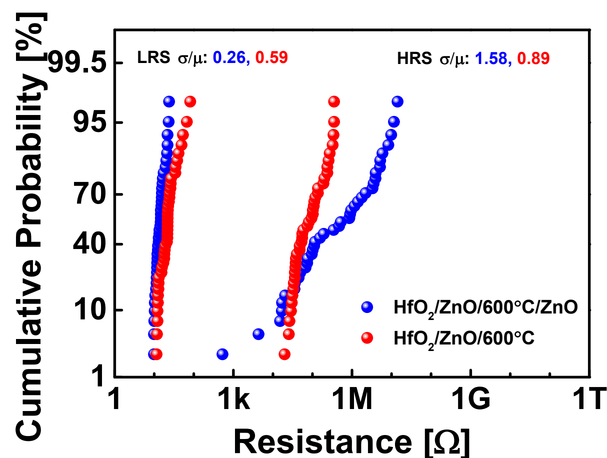

Figure S3. Distribution and cumulative probability of the high-resistance state (HRS) and low-resistance state (LRS) for bilayer 3 nm HfO_2/3 nm ZnO synaptic devices with thermal annealing at 600℃ and bilayer 3 nm HfO_2/3nm ZnO-thermal annealing at 600℃/3 nm ZnO synaptic devices, where the HRS and LRS were extracted at a read voltage of ±0.3 V.

Figure S3 showed the distribution and cumulative probability of HRS and LRS for the added 3 nm ZnO films after a bilayer 3 nm HfO_2/3 nm ZnO structure with thermal annealing at 600℃. The added ZnO films caused the cumulative probability and distribution degradation of HRS and LRS. As result, the resistive switching behavior based on ZnO film synaptic devices was not improved by simply increasing the thickness without thermal annealing.

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