Supporting Information

Floating-Gate Field-Effect Transistor Memory Based on Organic Crystals with Built-In Tunneling Dielectric by One-Step Growth Strategy

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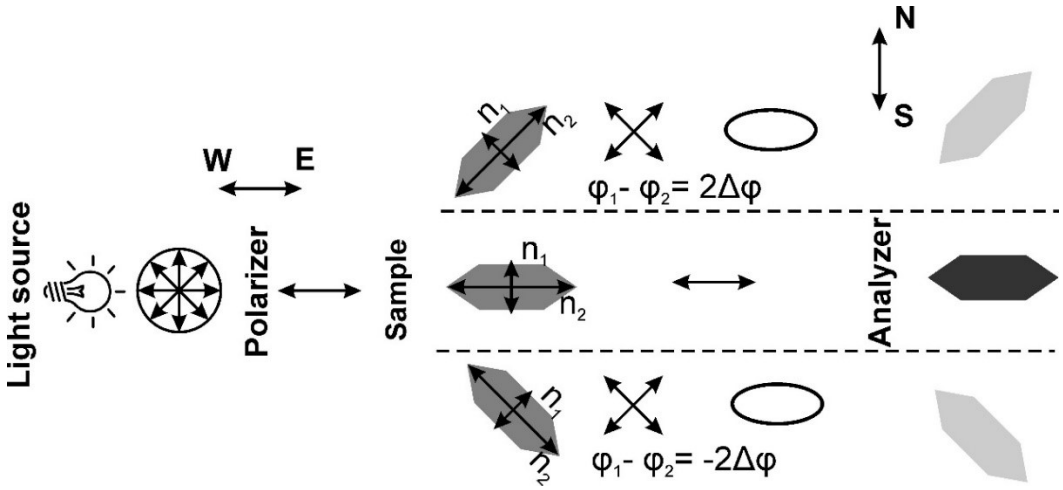

Figure S1. Schematics of light propagation in an anisotropic crystal during CPOM in reflected configuration.

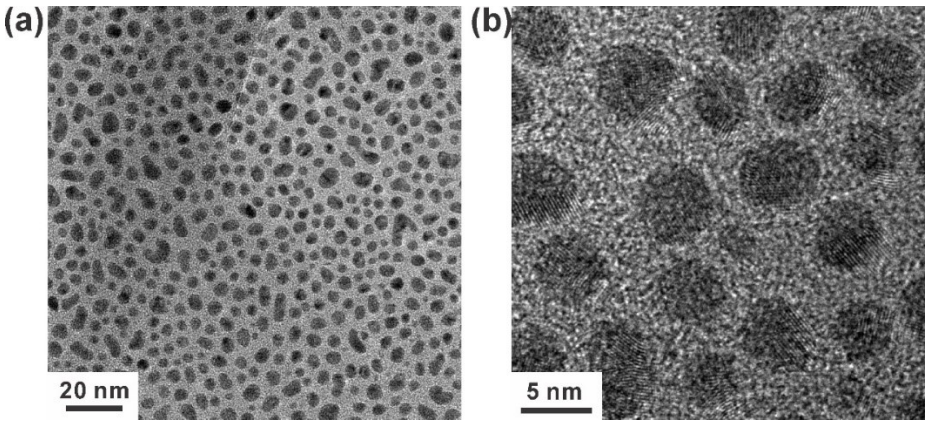

Figure S2. (a) Low-magnification TEM image and (b) HRTEM image of the Au NPs deposited by sputtering method. The lattice fringes in Au NPs can be clearly observed from HRTEM image.

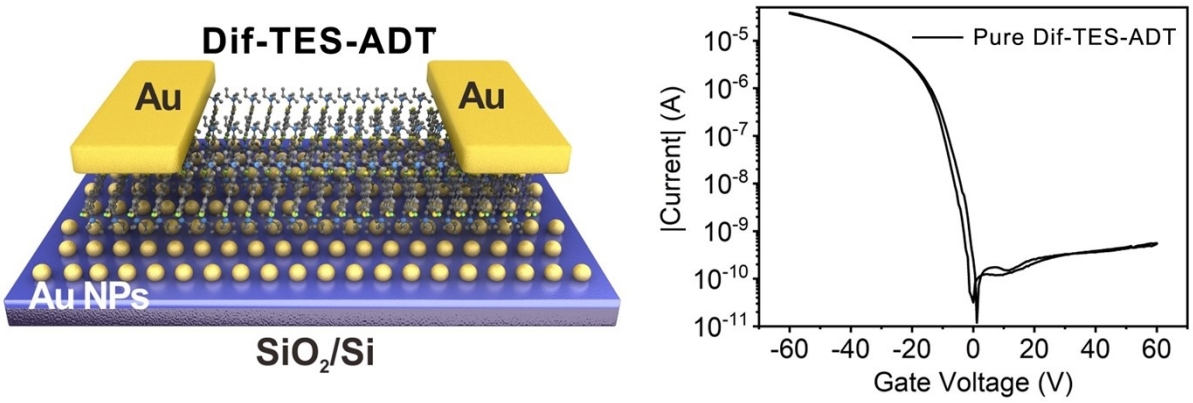

Figure S3. (a) Schematic illustration and (b) electrical transfer characteristic of a pure Dif-TES-ADT based transistor without a PS layer. A fixed V_{DS} of 1 V was applied.

The pure Dif-TES-ADT device was fabricated on the top of the flexible substrate from 3 mg mL^{-1} Dif-TES-ADT solution in toluene *via* an established blade-coating method. A piece of silicon wafer was used as the blade to drag the Dif-TES-ADT solution across the substrate at a speed of ~115 μm s^{-1}. With the solvent evaporation, molecules would nucleate and crystallize, generating highly ordered Dif-TES-ADT crystals on the flexible substrate. The detailed fabrication of substrate and electrodes are the same as in the manuscript.

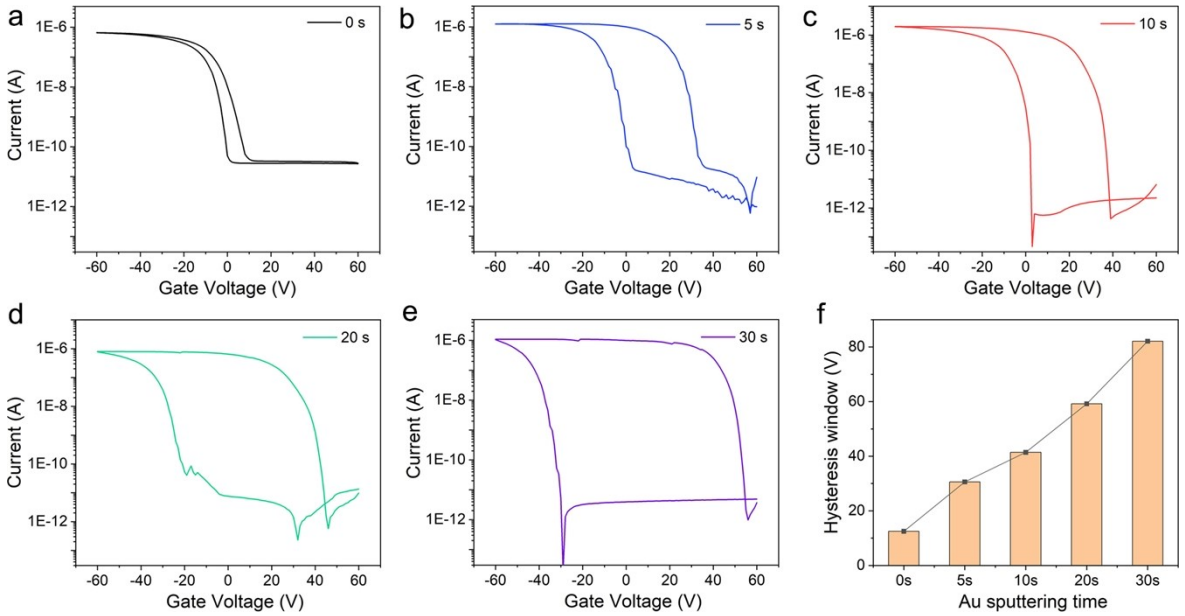

Figure S4. Electrical transfer characteristics of the FG-OFET devices with different Au NPs sputtering time of (a) 0 s, (b) 5 s, (c) 10 s, (d) 20 s, (e) 30 s and (f) the comparison of hysteresis windows in FG-OFET memory devices with different Au NPs sputtering times.

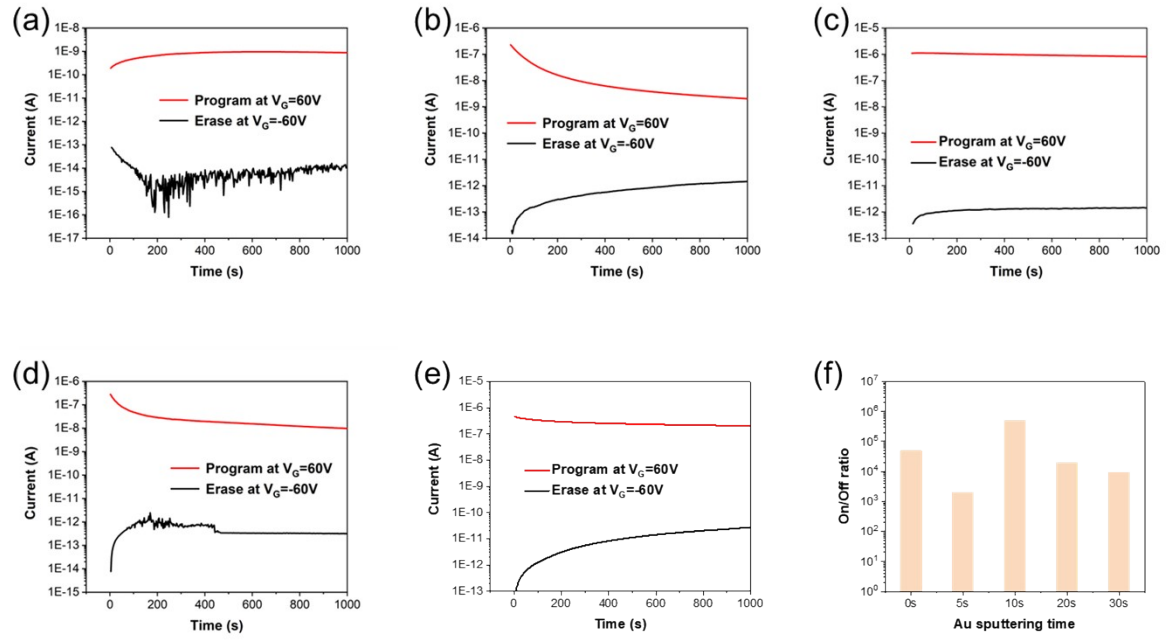

Figure S5. Retention behaviors of the FG-OFET devices with different Au NPs sputtering time of (a) 0 s, (b) 5 s, (c) 10 s, (d) 20 s, (e) 30 s and (f) the comparison of on/off ratios after 100 s.

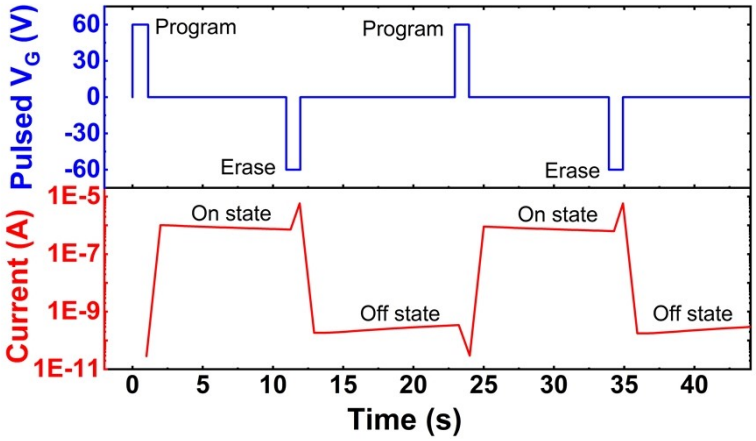

Figure S6. The detailed pattern of the pulsed gate voltage for the dynamic switching between the erased state (Off) and the programmed state (On). The duration time of the programing and erasing bias is 1 s.

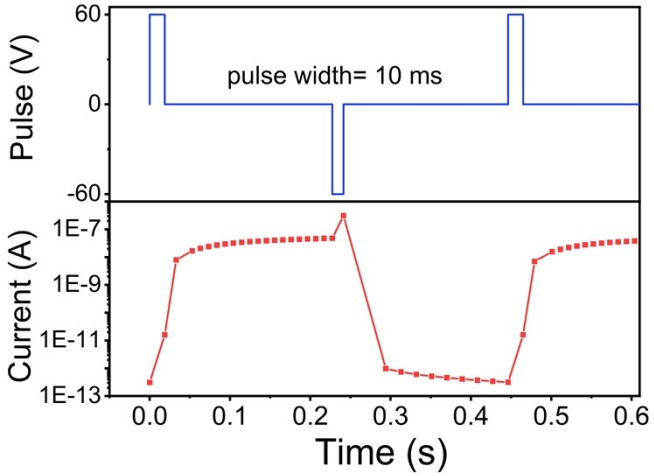

Figure S7. Transient curve of the FG-OFET memory device under the ±60 V programing and erasing voltages with a programing/erasing pulse width of 10 ms.

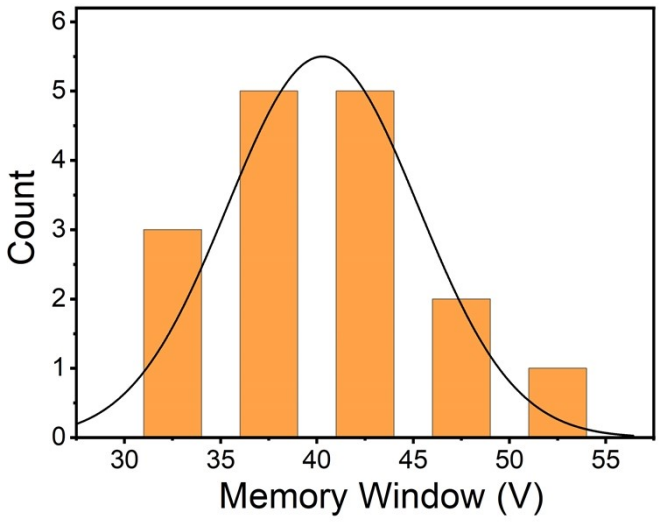

Figure S8. Memory window distribution in the 4×4 FG-OFET memory devices array on same substrate.

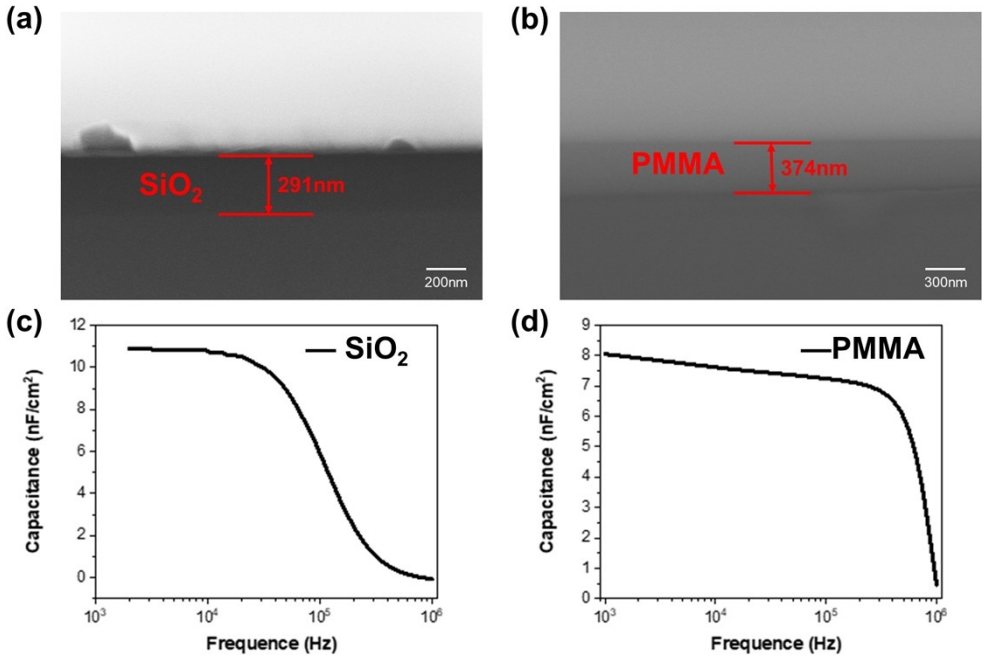

Figure S9. The cross-sectional SEM images of (a) SiO_2 and (b) PMMA dielectric layers. The capacitance per unit area-frequency characteristics of (c) SiO_2 and (d) PMMA dielectric layers.

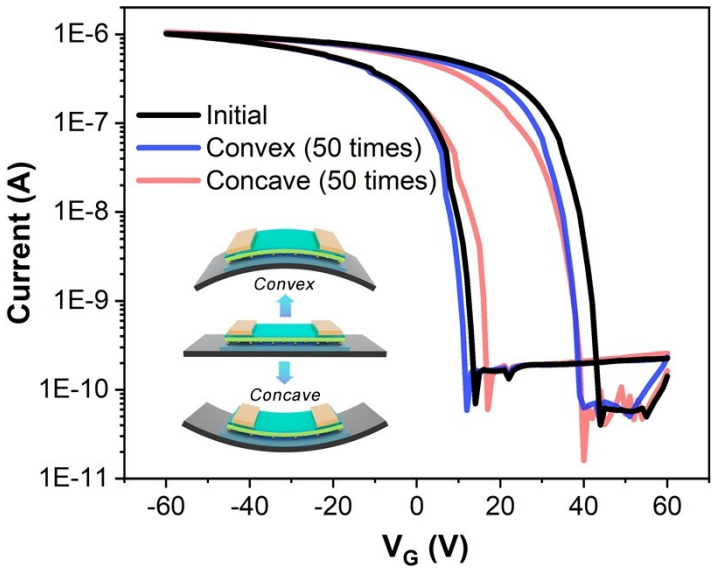

Figure S10. The endurance characteristics of the flexible FG-OFET memory device under convex and concave bending states in 50 cyclic tests. A fixed V_{DS} of 1 V was applied and the bending radius (R) was 1 cm.

Table S1. Comparison of device performances of low-dimensional semiconductor-based OFGMs.

Device structure	Hysteresis window/Operation voltage (V)	Retention (s)	ON/OFF ratio	Ref
Pentacene/SiO_2/Au NPs	23.6/80	N/A	~10	Ref[1]
Pentacene/AlO_x/PVDF-TrFE	20/80	2×10^4	10^3	Ref[2]
Pentacene/HfO_2	22.6/120	\	10^3	Ref[3]
Pentacene/APTES/Au NPs	10/180	10^5	10^3	Ref[4]
P3HT/MoS_2	23/160	\	10^5	Ref[5]
CDT-DPP-TVT/Cytop/Au NPs	25/120	10^4	10^4	Ref[6]
Pentacene/Maltoheptaose	3.2/100	3.6×10^4	10^6	Ref[7]
Pentacene/Polarizable polymers	33.7/140	<1000	10^4	Ref[8]
Pen/Pentafluorosulfanylated polymers	34/240	10^4	10^6	Ref[9]
QQT$(CN)_4$/PVDF-TrFE	25/100	6000	$<10^3$	Ref[10]
DH-6T/SAM	0.1/4	~3600	2.4	Ref[11]
PTDPPTFT4/o-MeO-DMBI	47/200	10^4	10	Ref[12]
Dif-TES-ADT:PS/Au NPs	41.4/120	5×10^3	10^5	Our work

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