Electronic Supplementary Material (ESI) for RSC Advances.

Supplementary Information

Low voltage-driven, high-performance TiO_2 thin film transistors with MHz switching speed

Xiaoping Chen,[a,b,c] Jiancong Ni,[a,b,c] Weiqiang Yang,[a,b,c] Shaoying Ke,[d]* and Maosheng Zhang[a,b,c]*

[a]Department of Chemistry, School of Chemistry and Chemical Engineering and Environment, Minnan Normal University, Zhangzhou 36300, China

[b]Fujian Provincial Key Laboratory of Modern Analytical Science and Separation Technology, Minnan Normal University, Zhangzhou, 363000, China

[c]Fujian Provincial University Key Laboratory of Pollution Monitoring and Control, Minnan Normal University, Zhangzhou 36300, China

[d]College of Physics and Information Engineering, Minnan Normal University, Zhangzhou 363000, China

*Corresponding authors: syke@mnnu.edu.cn and zms0557@mnnu.edu.cn

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Supplementary section S1. Fabrication flow schematics

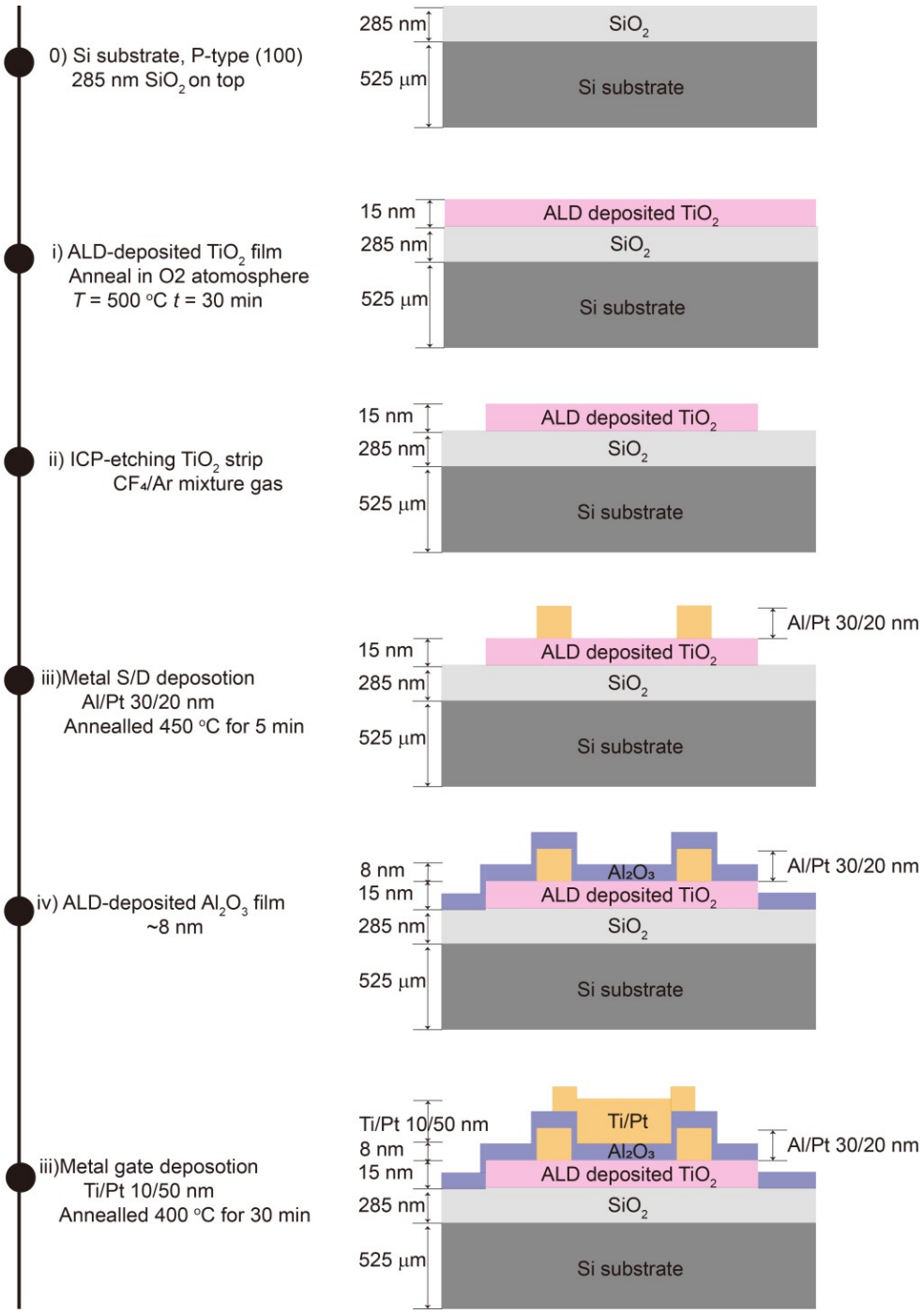

Figure S1. Stepwise fabrication flow of TiO_2 thin film transistors and the corresponding cross-section illustration for each step.

Supplementary section S2. Top-view SEM image and device dimension

Figure S2 shows the SEM planar image of our fabricated TiO_2 thin film transistors. The active channel of TiO_2 TFTs is 18 (length)× 10 (width) μm^2, while the contact pad area is designed 120 × 120 μm^2 for probe electrical measurement. The gap lengths between the top gate and the active channel were fabricated as 2.2 and 4.4 μm, respectively. We notice that the edge of metallic pads is rounded and not perfectly complete probably due to contamination during the photolithography process.

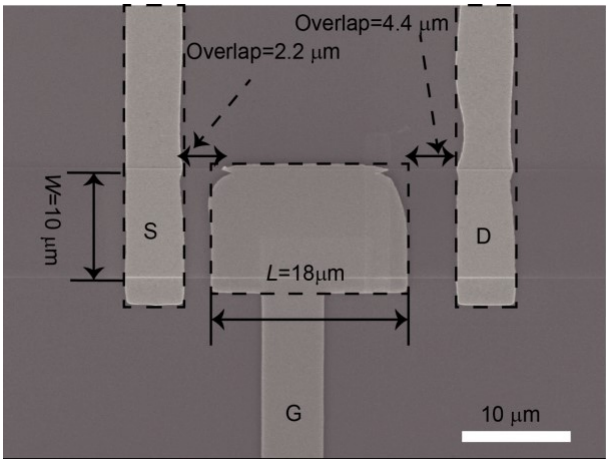

Figure S2. SEM image of the fabricated TiO_2 thin film transistors.

Supplementary section S3. XRD and Raman measurement of TiO_2 thin film

To investigate the TiO_2 film quality as the channel material, the X-ray diffraction technique and Raman spectroscopy were typically utilized to characterize the crystalline phase and thin film quality. Figure S3a exhibits the XRD spectrum of TiO_2 thin film deposited on silicon substrates, where three distinct diffraction peaks were collected at 25°, 35°, and 46°. These three peaks correspond to the crystalline facets of (101), (004), and (200) for the anatase phase of TiO_2 (JCPDS, No.21-1272), showing a good crystallinity of deposited TiO_2 thin film after annealed at 500 °C for 30 min.[1-2] We also observe that our collected signal intensity of XRD spectra is much lower than the counterparts reported in other literature due to the ultrathin thickness of our deposited TiO_2 thin films (~ 15.8 ± 0.4 nm). This is also the reason why we have chosen silicon as the substrate for material characterization for high collection signals (TiO_2 thin film was deposited on Si substrate for XRD analysis. To confirm the improvement of crystallinity and quality of TiO_2 thin film before and after annealing, we also collected the corresponding Raman spectra using a 325 nm laser at the Raman shift ranging from 100 cm^{-1} to 800 cm^{-1} (Figure S3b). For as-deposited TiO_2 thin film, we can only observe one Raman peak of Si substrate located at 520 cm^{-1} without significant Raman features of TiO_2 thin film, which suggests the amorphous phase before annealing. In terms of the O_2-annealed TiO_2 thin film, there exist three obvious Raman features located at 142, 396, and 635 cm^{-1}, which corresponds to the E_g, B_{1g}, and E_g modes of the anatase phase of TiO_2 accordingly.[3] We also noticed that the Raman peaks of silicon are present since an ultrathin layer of TiO_2 thin film (15.8 ± 0.4 nm) was deposited directly on bare silicon substrates due to their low Raman scattering cross-section and high optical

transparency.[4-5] Based on the XRD and Raman spectrum, we can confirm the formation of the anatase polycrystalline phase of TiO_2 thin film after O_2 annealing, which could contribute to a higher electron mobility as a channel material.

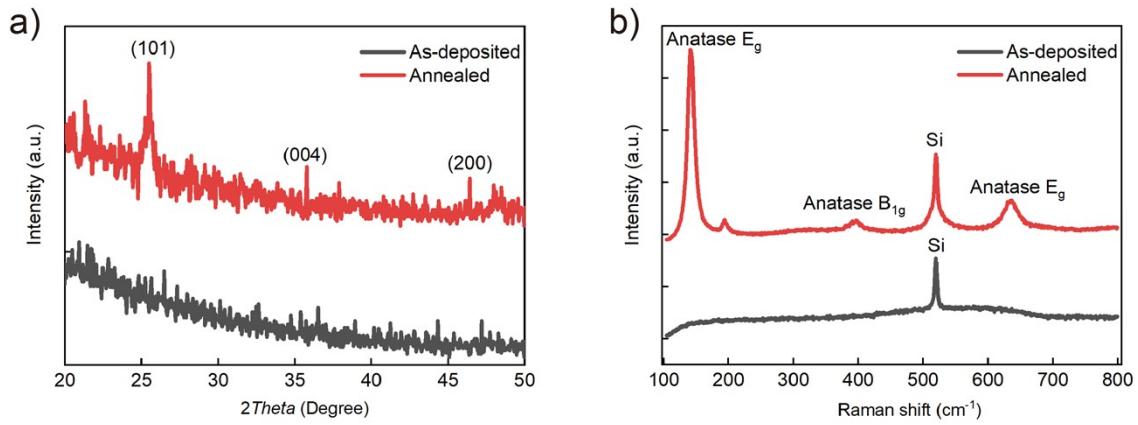

Figure S3 Material characterization of as-deposited and annealed TiO_2 thin film. (a) XRD spectrum showing the (101) orientation and the anatase phase after TiO_2 thin film annealing at 500 ^oC for 30 min at an oxygen atmosphere. (b) Raman Spectra showing the improvement of crystallinity after O_2 annealing treatment.

Supplementary section S4. XPS measurement of TiO_2 thin film

Figure S4 shows the X-ray photoelectron spectroscopy (XPS) and ultraviolet photoelectron spectroscopy (UPS) characterizations for the as-deposited and annealed TiO_2 films. Figure S4a gives the survey results of the material, O 1s, Ti 2p, and the VB binding energy can be found in the spectra, and the existence of C 1s could be due to the inevitable contamination. Figure S4b exhibits the Ti 2p orbital binding energies with typical Ti^{4+} splits at 464.8 eV ($2p_{1/2}$) and 458.9 eV ($2p_{3/2}$); while for the as-deposited one, a pair of extra peaks present at 463.3 eV ($2p_{1/2}$) and 457.2 eV ($2p_{3/2}$) could be due to the byproducts of Ti^{3+} species[6-7]. The O 1s spectra (Figure S4c) confirm the existence of Ti^{3+} species before annealing, where the O 1s at 530.4 eV and 530.8 eV are assigned to O bonded to Ti^{4+} and Ti^{3+}, respectively[7]. The valence band results from UPS characterization are shown in Figure S4d, we can see a shift of the valence band from 2.61 eV to 3.00 eV after annealing the TiO_2 which removes the defects raised from Ti^{3+}-associated species, the phenomenon is in good agreement with the previous report[6]. The characterization results indicate that the annealing process removes the defects of non-totally oxidized Ti, therefore improving the crystalline lattice and electron mobility.

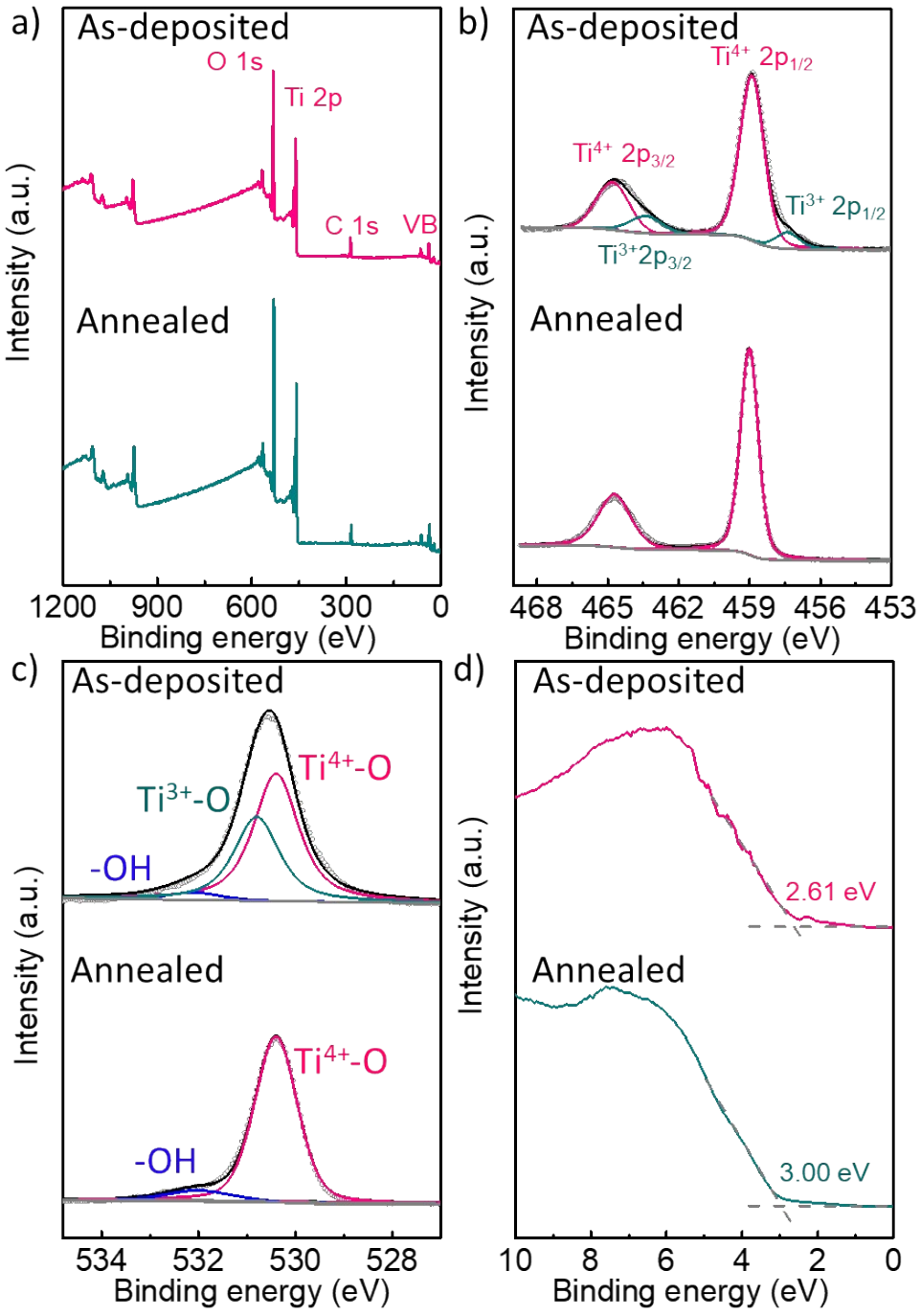

Figure S4 XPS characterization of as-deposited and annealed TiO_2 thin film. (a) XPS survey for the as-deposited (pink line) and annealed (dark cyan) TiO_2 layers. Ti 2p spectra (b), O 1s spectra (c), and UPS valence bands (d) for as-deposited (top section) and annealed (bottom section) TiO_2 layers.

Supplementary section S5. AFM measurement of TiO_2 thin film

AFM technique is one of the common techniques to characterize the surface roughness of thin films. Figure S5a shows the 3D schematic illustration of surface roughness over an area of 1×1 μm^2. The root mean square (RMS) of thin film is to characterize the surface microscopic peaks and valleys. The root mean square of the surface roughness is around 0.3 nm, which suggests the surface of the as-deposited TiO_2 thin film is quite uniform at atomic levels. Figure S5b presents the vertical profile as a function of horizontal distance.

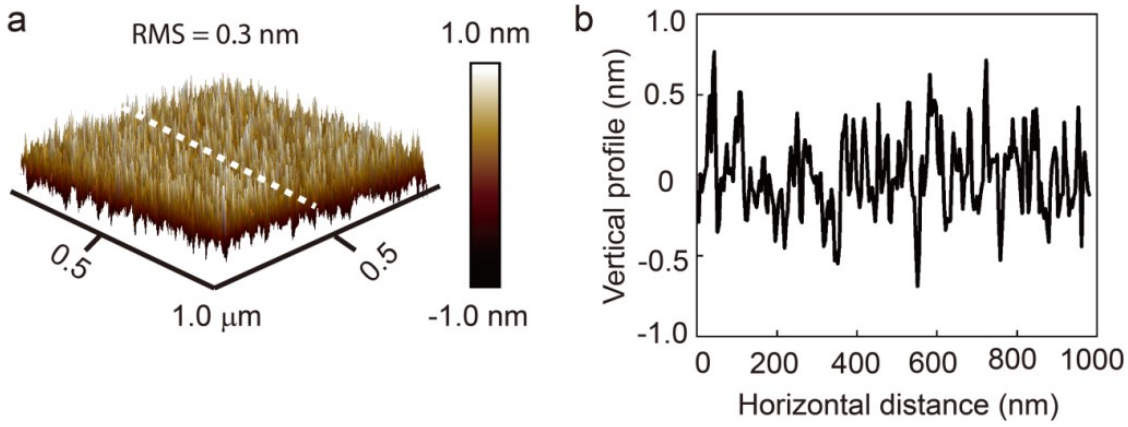

Figure S5. AFM measurement of the as-deposited TiO_2 thin film. (**a)** 3D schematic illustration of surface roughness over an area of 1×1 μm^2. The surface roughness (RMS) of the thin film is around 0.3 nm, which is limited by the detection limit. (**b)** Vertical profile as a function of horizontal distance.

Supplementary section S6. Ellipsometry measurement of TiO_2 thin film

To measure the thickness and uniformity of TiO_2 thin film, ellipsometry is an indispensable technique to investigate the dielectric properties by collecting the change of polarization of incident light and fitting the result to an appropriate model. The change of polarization can be characterized by the amplitude ratio (ψ) and phase difference (Δ), which are dependent on the optical properties and thickness of thin films. Figure S6 shows the spectral ellipsometry result of TiO_2 thin film on silicon substrates. As is shown in Figures S6a, 6b, and 6c, we have collected the ellipsometry signals over five different locations and the averaged thickness is 15.76 ± 0.43 nm, suggesting excellent TiO_2 thin film uniformity. Figure S6d illustrates the spectral dependent amplitude component (ψ) and phase difference (Δ), which are fitted by the Cauchy model with good agreement.[8-9] Even though the electron mobility of TiO_2 thin film is dominated by thin film quality and crystalline phases, the electron mobility can deteriorate significantly when the thickness of TiO_2 thin film decreases to a threshold value due to significant surface scattering. It would be interesting to take a closer look at the role of decreased thin film thickness on the transistor electrical performances, which will be our future work.

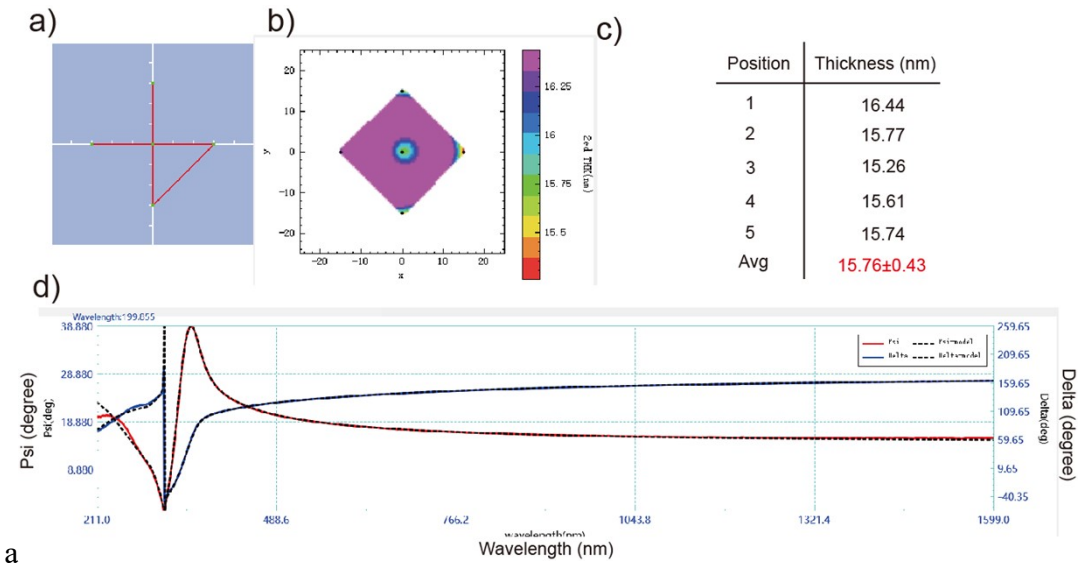

Figure S6. Ellipsometry measurement of TiO_2 thin film on silicon substrates. (a) Schematic illustration of measured various positions across the whole sample (2 cm × 2 cm). (b) Color map of thermally-grown TiO_2 thickness collected at five positions. (c) Table of measured results of TiO_2 thickness collected at various positions. The average thickness of thermally-grown TiO_2 is 15.76±0.43 nm. (d) Fitted curves of Psi and delta signals as a function of wavelength in a unit of nm.

Supplementary section S7. Source and drain contact resistivity between Al(Pt)/TiO_2 interfaces

Before we investigate the electrical properties of TiO_2 thin film transistors, we have to make sure of the formation of Ohmic contact between Al and TiO_2 layers. The transfer length method, also known as TLM, is a common technique to determine the specific contact resistivity of metal-semiconductor interfaces, which show Ohmic contact behaviour[10-11]. The specific contact resistivity (ρ_C) can be fitted via the function between total resistance (R_{total}) and transfer length (L_T) as illustrated in the following Equation (1):

$$R_{total} = \frac{R_s}{W}(L + 2L_T)$$

wherein R_S stands for the sheet resistance of the semiconducting layer. Figures S7a and S7b illustrate the top-view design layout and the corresponding cross-section schematic for TLM measurement. The blue rectangular represents the metal pad directly deposited onto as-fabricated TiO_2 thin film. The deposited metal pads are spaced at various distances from 5 μm to 150 μm for the electrical measurement of *I*(V) curves. Figure S7c represents the current-voltage characteristics performed across each gap spacing and *I*(V) curves show good Ohmic properties since each curve crosses the origin (0,0) and the calculated resistance increases as the gap widens. Figure S7d shows the plot of calculated total resistance (R_{total}) as a function of gap length and the red dotted line represents the fitting result, where we can determine the transfer length (L_T) of 6.58 μm and the specific contact resistivity (ρ_C) of 0.13 Ω·cm^2. We also notice the fitted specific contact resistivity is 3-4 orders of magnitude higher compared with well-established silicide technology,

which suggests there is plenty of room for improvement in terms of drain/source contacts[12-13].

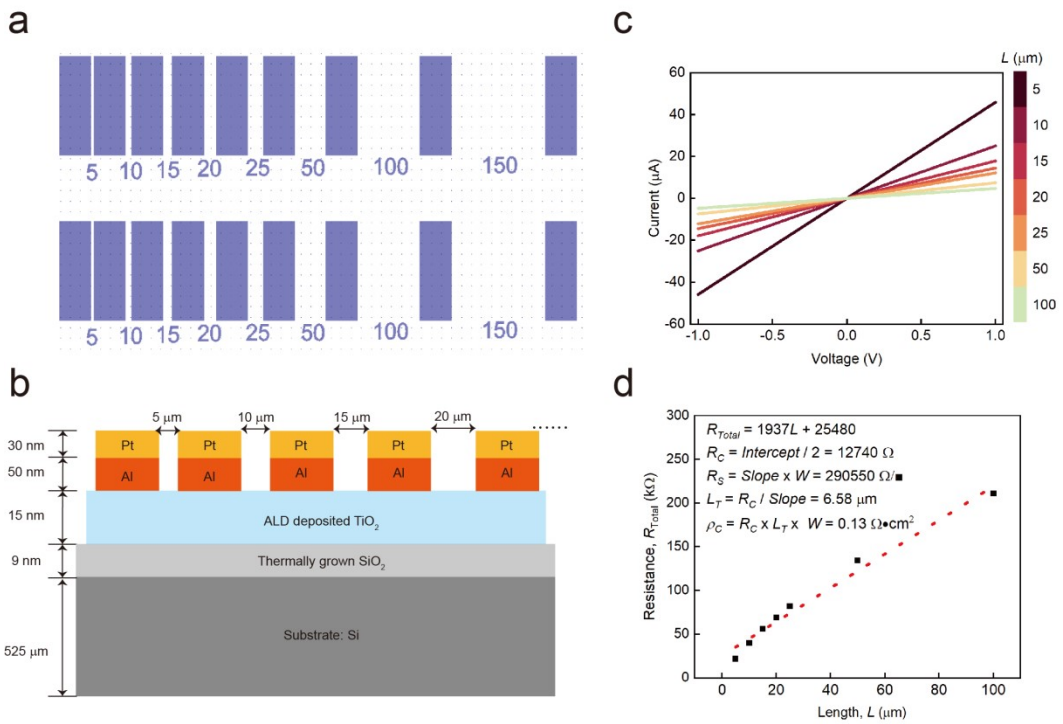

Figure S7 (a) Top view of design layout for TLM measurement. The blue rectangular represents the metal pad directly deposited onto as-fabricated TiO_2 thin film. (b) The cross-section schematic illustration shows spaced metal pads with designated distances. (c) Current-voltage relation of TiO_2/Al/Pt contacts. Each curve represents the contact measured with various spacing distances. (d) Total resistance (R_{Total}) plotted against the transfer length (L) with calculated electrical parameters of TiO_2/Al/Pt contacts.

Supplementary section S8. MOS electrostatics: leakage current, breakdown voltage, and effective mobility extraction

For the electrical performance of thin film transistors, three major parameters need to be investigated including the leakage current, breakdown voltage, and effective mobility extraction. To study the electrical property of the MOS (metal-oxide-semiconductor) configuration, as is shown in Figure S8a, we have fabricated a new device consisting of a Ti/Pt top metal, an Al_2O_3 oxide layer, and an ALD-deposited TiO_2 layer (Ohmic contacted with another layer of Al/Pt). Figure S8b shows the leakage current as a function of applied voltages collected from three different devices. It is noticeable that the breakdown voltages of the three devices are around 4.8 V and the corresponding breakdown electrical field is 6.0 MV/cm, which is close to the reported values and lower than the counterpart of SiO_2 dielectrics due to the lower band gap[14-15]. We also observe that the leakage current density is below 10^{-6} A/cm^2 at the voltage range -2.0 V to +2.0 V of our interest, suggesting our deposited Al_2O_3 layer is of good insulating quality. The capacitance of the Al_2O_3 layer can be extracted via capacitance-voltage measurement at a frequency of 1.0 KHz (Figure S8c) and the corresponding value is 1.05×10^{-6} F/cm^2. Figure S8d shows the transfer curve of TiO_2 thin film transistors collected at V_{DS} = 100 mV. It can be found that the threshold voltage is 0.20 V via the extrapolation in the linear region (gate voltage axis intercept, i.e., I_{DS} = 0). We can also calculate the effective electron mobility of TiO_2 thin film using the equation (E1):

$$\mu = L/(C_{ox} \cdot W \cdot V_{DS}) \cdot \frac{\partial I_{DS}}{\partial V_{GS}}$$

Where C_{ox} is the geometrical capacitance of the Al_2O_3 dielectric layer; L and W represent the channel length and width, respectively. Our calculated electron mobility of TiO_2 thin

film is 3.87 $cm^2 \cdot V^{-1} \cdot s^{-1}$, which is comparable with the as-far best-reported value (~10.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$).[16] We understand that there are many other methods to estimate an effective electron mobility, and each method has its pros and cons. Herein, for a fair comparison, we followed the same extraction procedure in the field of TiO_2 thin film transistors.

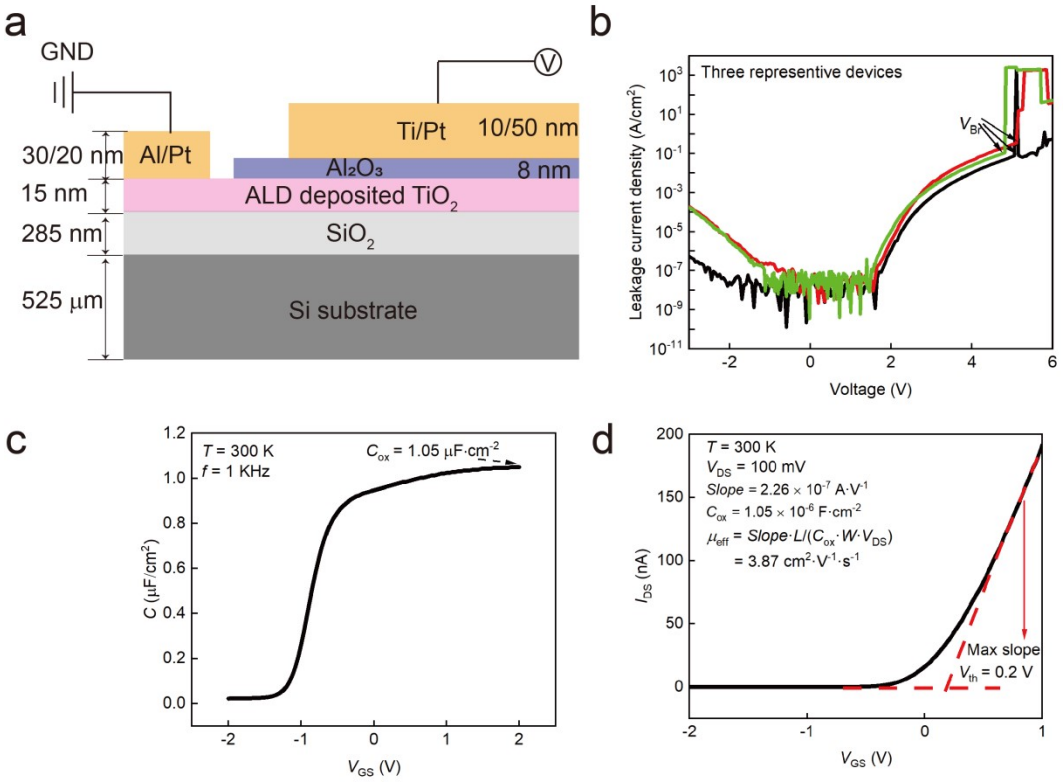

Figure S8 (a) Cross-section schematic of MOS structure and the electrical connection. The thickness of each layer corresponds to the TiO_2 thin film transistors. (b) Leakage current as a function of applied voltages ranging from -3.0 V to +6.0 V. (c) Capacitance-voltage measurement based on MOS structure to extract the C_{OX} at a frequency of 1.0 KHz. (d) Transfer curve of TiO_2 thin film transistors collected at V_{DS} = 100 mV to extract the effective mobility and the threshold voltage.

Supplementary section S9. Subthreshold swing calculated at various temperatures

To investigate the temperature-dependent transfer characteristics, we have calculated and plotted the subthreshold swing of TiO_2 TFTs at various temperatures. Figures S9a and S9b present the transfer and output curves at T= 77 K (V_{DS} ranging from 0.2 V to 2.0 V at an interval of 0.2 V. Our proposed TiO_2 TFTs can operate at low temperatures and show similar behaviour compared with the counterparts at T =300 K. Figures S9c and S9d plot the extracted subthreshold swing as a function of temperature collected at V_{DS} = 0.2 V and 2.0 V, respectively. The temperature ranges from 300 K to 77 K at an interval of 30 K. We notice that the extracted subthreshold swing decreased as a function of temperature at the same drain-to-source current. Figure 3e presents the minimum subthreshold swing as a function of temperature, which manifests that the minimum subthreshold swing value decreases linearly against temperature.

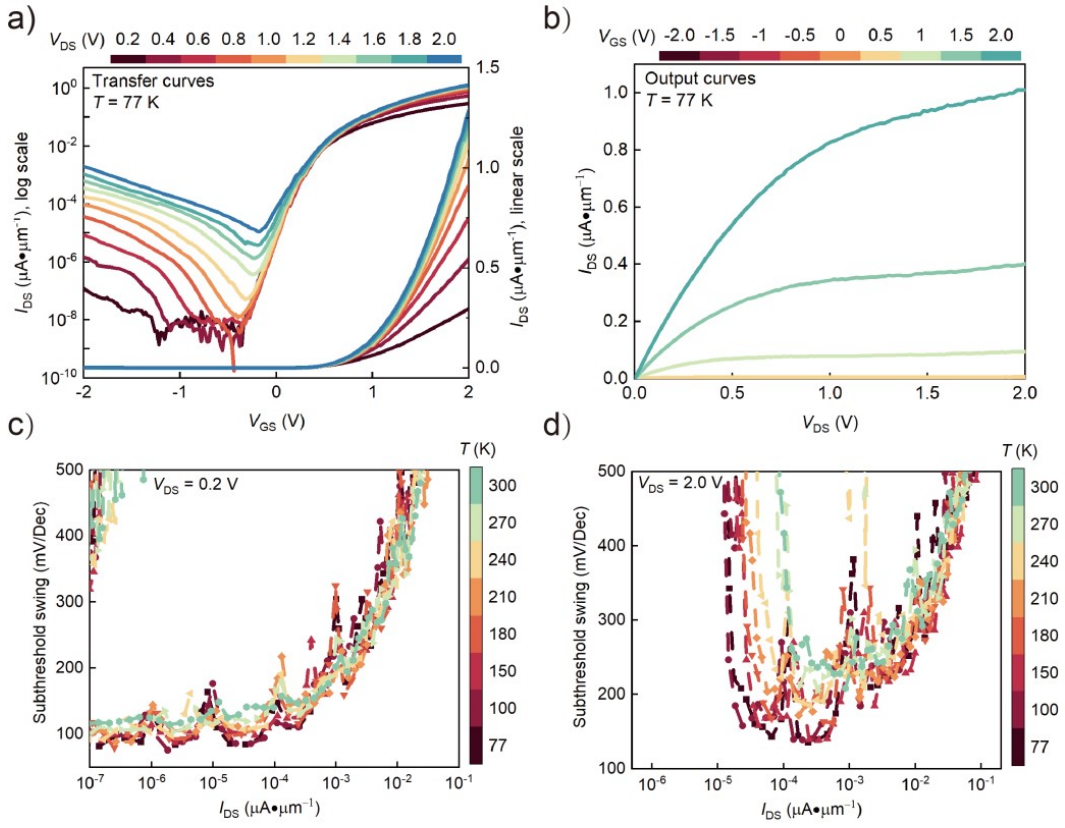

Figure S9 (a)-(b) Extracted subthreshold swing as a function of temperature collected at V_{DS} = 0.2 V (a) and 2.0 V (b), respectively. The temperature ranges from 300 K to 77 K at an interval of 30 K.

Supplementary section S10. Dynamic switching speed at $T = 77$ K

To further study the time-resolved transient switching characteristics of TiO_2 TFTs at $T = 77$ K, we have repeated the measurement demonstrated in Figure 3 from the main text. Figures S10 (a)-(f) represent the corresponding dynamic time traces collected at different frequencies from 100 Hz to 10 MHz at an interval of one order of magnitude. We notice that the switching behaviour of TiO_2 thin film transistors operated at $T = 77$ K shares a similar trend compared with the counterpart at 300 K. Our result shows that the proposed TiO_2 TFTs can be switched on and off at various temperature ranges.

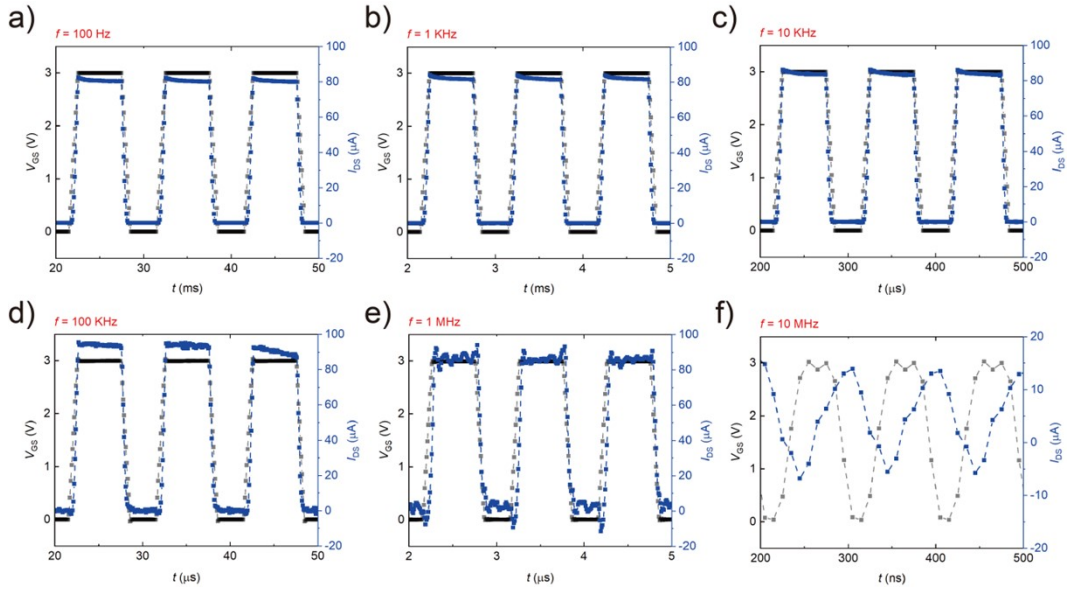

Figure S10 Transient threshold switching dynamics of TiO_2 thin film transistors at T = 77 K. (a)-(f) represent the corresponding dynamic time traces collected at different frequencies from 100 Hz to 10 MHz at an interval of one order of magnitude.

Supplementary section S11. Benchmark and highlights of electrical performance

Table S1 Benchmark of electrical performance for our proposed TiO_2 TFTs and the counterparts reported from other literature

Ref	Material	I_{on}/I_{off}	SS (mV/Dec)	Mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	Switch Speed	Inverter Gain
[17]	a-Si	$>10^6$	~ 500	< 1	100 K	-
[18]	Poly-Si	10^8-10^9	~110	60-80	100 MHz	-
[19]	a-IGZO	10^5 - 10^6	~ 300	10.51	0.1 MHz	15
[20]	ZnON	10^7-10^8	> 1000	50	0.1 MHz	-
[21]	Organic	$\sim 10^{10}$	59	4.3	21 MHz	3-4
[22]	TiO_2	10^4 - 10^5	> 1000	~ 0.1	-	-
[23]	TiO_2	10^4 - 10^5	> 1000	0.057	-	-
[24]	TiO_2	10^7-10^8	> 1000	~ 0.1	-	-
[25]	TiO_2	10^5 - 10^6	> 1000	~ 0.05	-	-
[16]	TiO_2	10^4	~ 1000	10.7	-	-
[26]	TiO_2	10^4	> 1000	0.08	-	-
[27]	TiO_2	10^7 - 10^8	72	5.74	-	-
This work	TiO_2	10^7-10^8	~ 300	5.4	> MHz	~5

References

1 G. Luka, B.S. Witkowski, L. Wachnicki, M. Andrzejczuk, M. Lewandowska and M. Godlewski, *CrystEngComm*, 2013, **15**, 9949-9954.
2 A.T. Hassan, E.S. Hassan and O.M. Abdulmunem, *J. Mech. Behav. Mater*. 2021, **30**, 304-308.
3 J. Zhang, M. Jia, M.G. Sales, Y. Zhao, G. Lin, P. Cui, C. Santiwipharat, C. Ni, S. McDonnell and Y. Zeng, *ACS Appl. Electron. Mater.* 2021, **3**, 5483-5495.
4 H. Li, B. Sun, T. Gao, H. Li, Y. Ren and G. Zhou, *Chin. J. Catal.* 2022, **43**, 461-471.
5 D. Liu, B. Sun, S. Bai, T. Gao and G. Zhou, *Chin. J. Catal.* 2023, **50**, 273-283.
6 Y. Xu, S. Wu, P. Wan, J. Sun and Z.D. Hood, *RSC Adv*., 2017, **7**, 32461-32467.
7 B. Bharti, S. Kumar, H.N. Lee and R. Kumar, *Sci. Rep*., 2016, **6**, 32355.
8 B. Hajduk, H. Bednarski and B. Trzebicka, *J. Phys. Chem. B*, 2020, **124**, 3229-3251.
9 H.-Q. Jiang, Q. Wei, Q.-X. Cao and X. Yao, *Ceram. Int.*, 2008, **34**, 1039-1042.

10 H. Park, J. Yun, S. Park, I.-s. Ahn, G. Shin, S. Seong, H.-J. Song and Y. Chung, *ACS Appl. Electron. Mater.*, 2022, **4**, 1769-1775.
11 S. Wittmann, F. Aumer, D. Wittmann, S. Pindl, S. Wagner, A. Gahoi, E. Reato, M. Belete, S. Kataria and M.C. Lemme, *ACS Appl. Electron. Mater.*, 2020, **2**, 1235-1242.
12 N. Stavitski, M.J.H.v. Dal, A. Lauwers, C. Vrancken, A.Y. Kovalgin and R.A.M. Wolters, *IEEE Electron Device Lett.*, 2008, **29**, 378-381.
13 K.K. Ng and R. Liu, IEEE Trans. *Electron Devices*, 1990, **37**, 1535-1537.
14 J. Kolodzey, E.A. Chowdhury, T.N. Adam, Q. Guohua, I. Rau, J.O. Olowolafe, J.S. Suehle and C. Yuan, IEEE Trans. *Electron Devices*, 2000, **47**, 121-128.
15 J. Suñé, I. Placencia, N. Barniol, E. Farrés, F. Martín and X. Aymerich, *Thin Solid Films*, 1990, **185**, 347-362.
16 W.S. Shih, S.J. Young, L.W. Ji, W. Water and H.W. Shiu, *J. Electrochem. Soc.*, 2011, **158**, H609.
17 A. Sharma, C. Madhu and J. Singh, *Int. J. Comput. Appl*., 2014, **89**, 36-40.
18 S.D. Brotherton, C. Glasse, C. Glaister, P. Green, F. Rohlfing and J.R. Ayres, *Appl. Phys. Lett.*, 2004, **84**, 293-295.
19 M. Naqi, Y. Cho and S. Kim, *ACS Appl. Electron. Mater.*, 2023, **5**, 3378-3383.
20 H.-D. Kim, M. Naqi, S.C. Jang, J.-M. Park, Y.C. Park, K. Park, H.-H. Nahm, S. Kim and H.-S. Kim, *ACS Appl. Mater. Interfaces*, 2022, **14**, 13490-13498.
21 J.W. Borchert, U. Zschieschang, F. Letzkus, M. Giorgio, R.T. Weitz, M. Caironi, J.N. Burghartz, S. Ludwigs and H. Klauk, *Sci. Adv.*, 2020, **6**, eaaz5156.
22 N. Zhong, J.J. Cao, H. Shima and H. Akinaga, *IEEE Electron Device Lett.*, 2012, **33**, 1009-1011.
23 J.W. Park, S.W. Han, N. Jeon, J. Jang and S. Yoo, *IEEE Electron Device Lett.*, 2008, **29**, 1319-1321.
24 J.W. Park, D. Lee, H. Kwon and S. Yoo, *IEEE Electron Device Lett.*, 2009, **30**, 362-364.
25 P.H. Wöbkenberg, T. Ishwara, J. Nelson, D.D.C. Bradley, S.A. Haque and T.D. Anthopoulos, *Appl. Phys. Lett.*, 2010, **96**, 082116.
26 M. Katayama, S. Ikesaka, J. Kuwano, Y. Yamamoto, H. Koinuma and Y. Matsumoto, *Appl. Phys. Lett.*, 2006, **89**, 242103.
27 J. Zhang, P. Cui, G. Lin and Y. Zeng, *2021 5th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*, *IEEE*, 2021, 1-3.