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Chemical-vapor-deposited 2D VSe_2 nanosheet with threshold switching behaviors for Boolean logic calculations and leaky integrate-and-fire functions

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Preparation of VSe_2 nanosheets:

VSe_2 nanosheets were prepared on SiO_2/Si substrates by chemical vapor deposition (CVD) method using precursors of selenium (Se, Shanghai Aladdin Biochemical Technology Co., Ltd.) and vanadium trichloride (VCl_3, Shanghai Aladdin Biochemical Technology Co., Ltd.) powders. The Se and VCl_3 powders were respectively put in two quartz boats. Then, put the two quartz boats into a quartz tube which was placed in the middle of a tube furnace. The SiO_2/Si substrate was placed in the downstream tube furnace with a distance of 12 cm from the VCl_3 quartz boat. The mixture gas of H_2 and Ar (1:9) was used as the carrier gas at a flow rate of 100 standard cubic centimeters per minute (sccm). The tube furnace was heated from room temperature to 500 ℃ and maintained the temperature for 10 min. Then, the tube furnace was naturally cooled to room temperature. Finally, we synthesized hexagonal VSe_2 nanosheets on SiO_2/Si substrates by the CVD method.[1]

Device fabrication:

Two-terminal planar memristors with Pt as the electrodes were fabricated through the photolithography technique. A thin layer of photoresist was spin-coated on the SiO_2/Si substrate where VSe_2 nanosheets are prepared by the CVD method. The sample were exposed to UV light using a UV lithography machine by patterned mask. Then, the sample was placed in a developer and the exposed photoresist was etched by developer. After that, Pt thin films with thickness about 100 nm were prepared on the top surface of the sample by sputtering method. Finally, the redundant Pt electrodes were washed away by ultrasonic treatment in acetone. Herein, the two-terminal Pt/VSe_2/Pt devices were fabricated.

Annealing process:

In our experiments, the threshold switching (TS) behavior of Pt/VSe_2/Pt devices can be achieved through rapid annealing method. The prepared Pt/VSe_2/Pt device was placed in a quartz tube. The quartz tube was cleaned with pure Ar for 30 min, so that the tube was in a high

Ar atmosphere. The tube furnace was heated quickly to 550 ℃ and maintained for 5 min, then the furnace was quickly returned to room temperature.[2]

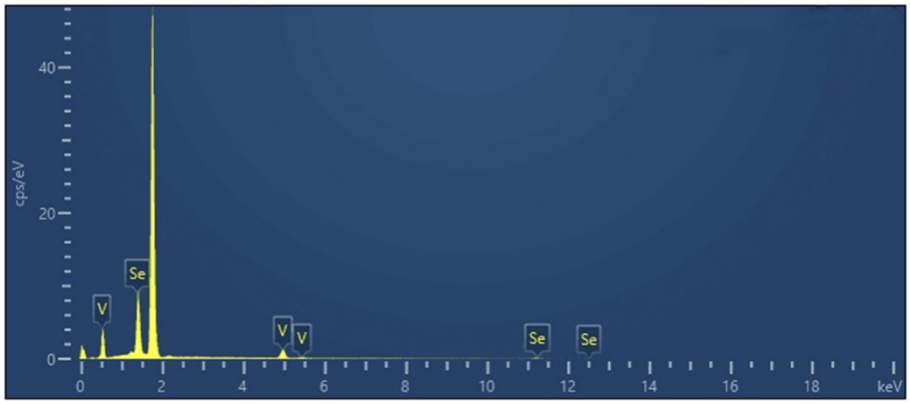

Fig. S1. Energy-dispersive X-ray spectroscopy (EDS) spectrum of the VSe_2 nanosheets.

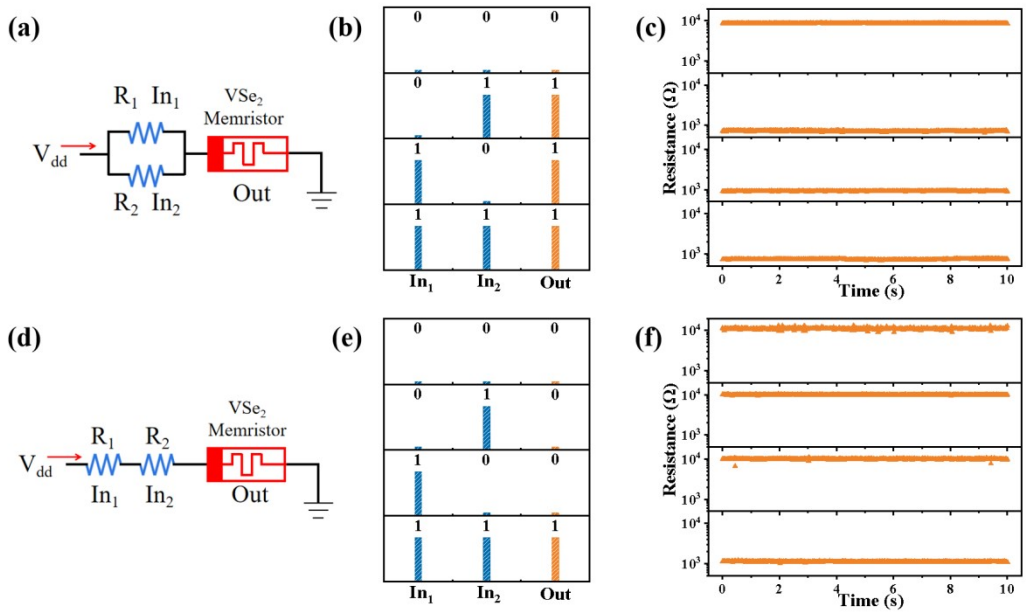

Fig. S2. Implementation of "OR" and "AND" logic gates with the Pt/VSe_2/Pt memristor. (a) Schematic of the "OR" logic gate circuit. (b) The truth table of the "OR" logic gate. (c) The experimental results of the continuous output resistance of the "OR" logic gate circuit within 10 s. (d) Schematic of the "AND" logic gate circuit. (e) The truth table of the "AND" logic gate. (f) The experimental results of the continuous output resistance of the "AND" logic gate circuit within 10 s.

The operation circuit of the "OR" and "AND" logic gates are shown in Figure S2(a) and (d). In our experiments, a VSe_2-based memristor (V_{TH} = 1.30 V, V_H = 0.40 V, the resistance at the HRS $R_{off} \approx 8000$ Ω and the resistance at the LRS $R_{on} \approx 700$ Ω) and two resistors R_1 and R_2 (both with high or low resistance states of 10000 or 700 Ω, respectively) are employed to realize the logic operation of "OR" and "AND" logic gates. The high (10000 Ω) and low (700 Ω) resistance states of the resistor are defined as the input high and low resistance states, i.e., "0" and "1", respectively. The high and low resistance states of the VSe_2 memristor are defined as the output "0" and "1", respectively. The "OR" logic gate circuit is realized by connecting the R_1 and R_2 in parallel and then in series with the VSe_2-based memristor. The "AND" logic gate circuit is implemented by the series connection of R_1, R_2 and VSe_2-based memristor. A constant voltage (V_{dd}) of 2V is applied. The VSe_2-based memristor gets different partial voltage owing to the

different resistance values of R_1 and R_2. Thus, the VSe_2-based memristor will obtain different resistance values according to the TS behaviors. Fig. S2(b) and (e) show the truth table for the "OR" and "AND" logic operations, respectively. The experimental resistance states of the memristor in the two logic gates are shown in Fig. S2(c) and (f), respectively. In each logic operation, the resistance output result of the VSe_2-based memristor is consistent with the result in the truth table, indicating that the designed logic circuit realizes the logic operation of "OR" and "AND". For example, in the logic “OR” circuit shown in Fig. S2(a), when the input resistor R_1 = 10000 Ω and R_2 = 10000 Ω, i.e., the input signals are “0” and “0”, the partial voltage on the memristor is approximately 1.23 V because of the initial HRS of the memristor based on the TS behaviors. The partial voltage (1.23 V, less than the V_{TH} of the memristor of 1.30 V) will keep the memristor at the HRS, i.e., the output is “0”. Furthermore, when the input resistor R_1 = 700 Ω and R_2 = 10000 Ω, i.e., the input signals are “1” and “0”, the partial voltage on the memristor is larger than the V_{TH} of the memristor 1.30 V, which will set the memristor from the HRS to the LRS, i.e., the output is “1”. Similarly, we can achieve the output “1” when the input signals are “0” and “1” as well as “1” and “1”. Therefore, the logic “OR” can be implemented based on our designed circuit by employing the fabricated memristor.[3]

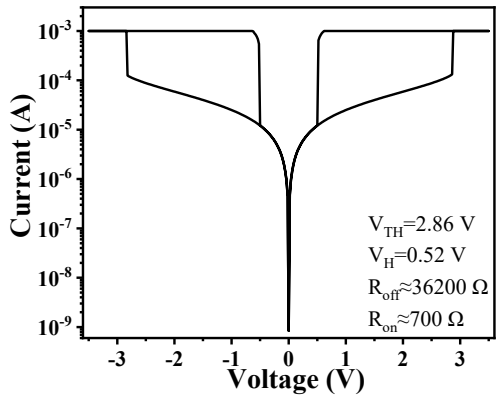

Fig. S3. The current−voltage *(I−V)* performance of VSe_2-based memristor for the leaky integrate-and-fire (LIF) activity.

Table S1. Element analysis of the synthesized VSe_2 nanosheets

Element	**Wt %**	**Atomic %**
Se	75.49	66.52
V	24.51	33.48

References

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