Electronic Supplementary Information

Multi-pulse atomic layer deposition of p-type SnO thin films: growth processes and the effect on TFT performance

Daisy Gomersall,*[a] Kham M. Niang,[a] James D. Parish,[b] Zhuotong Sun,[c] Andrew L. Johnson,[b] Judith L. MacManus-Driscoll,[c] and Andrew J. Flewitt[a]

[a] Electrical Engineering Division, Engineering Department, University of Cambridge, Cambridge CB3 0FA. E-mail: daisy.gomersall@cantab.net

[b] Department of Chemistry, University of Bath, Claverton Down, Bath, BA2 7AY

[c] Department of Materials Science & Metallurgy, University of Cambridge, Cambridge CB3 0FS

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Tab. S1 Summary of Hall measurements for the SnO films. The films deposited with 1 x Sn pulse and annealed at 250°C were beyond the limit of the Hall measurement system due to the high resistance of the films.

	Thickness (nm)	Annealing temperature (°C)	Resistivity (Ω cm)	Carrier Concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier type
1 x Sn pulse						
	55	250	-	-	-	-
		350	9.5	4.1×10^{17}	3.3	holes
3 x Sn pulse						
	65	250	87.2	6.4×10^{16}	1.4	holes
		350	31.1	5.3×10^{16}	3.8	holes
3 x Sn pulse + Exposure						
	70	250	28.9	3.7×10^{17}	1.3	holes
		350	27.3	2.4×10^{17}	1.2	holes

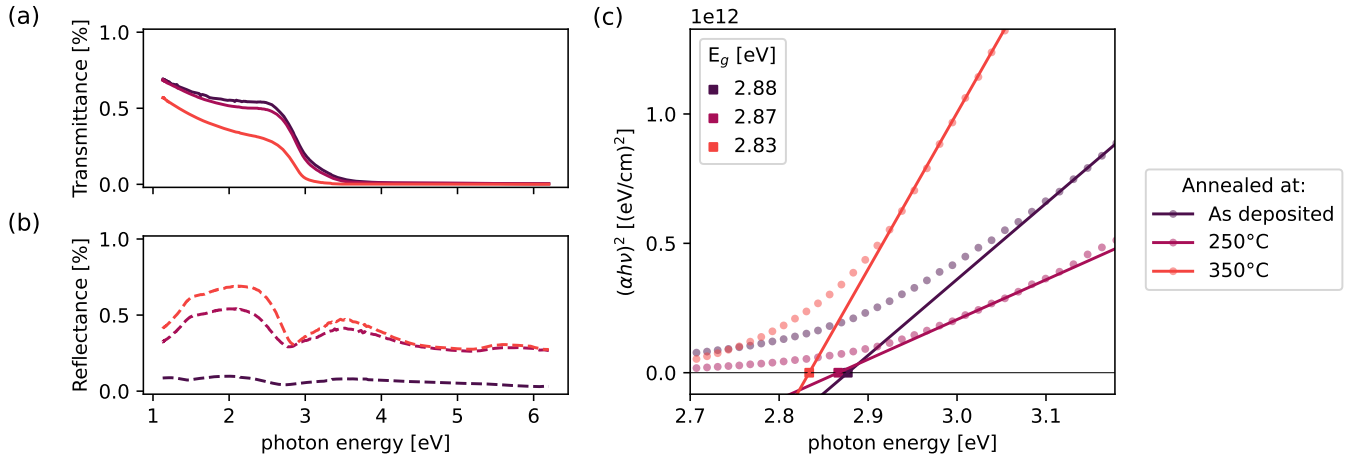

Fig. S2 Optical properties of SnO films with varying annealing temperatures, showing: **(a)** transmittance, **(b)** reflectance and **(c)** a Tauc plot with extracted band gap energies. The films were deposited using the 3 x Sn with exposure mode.

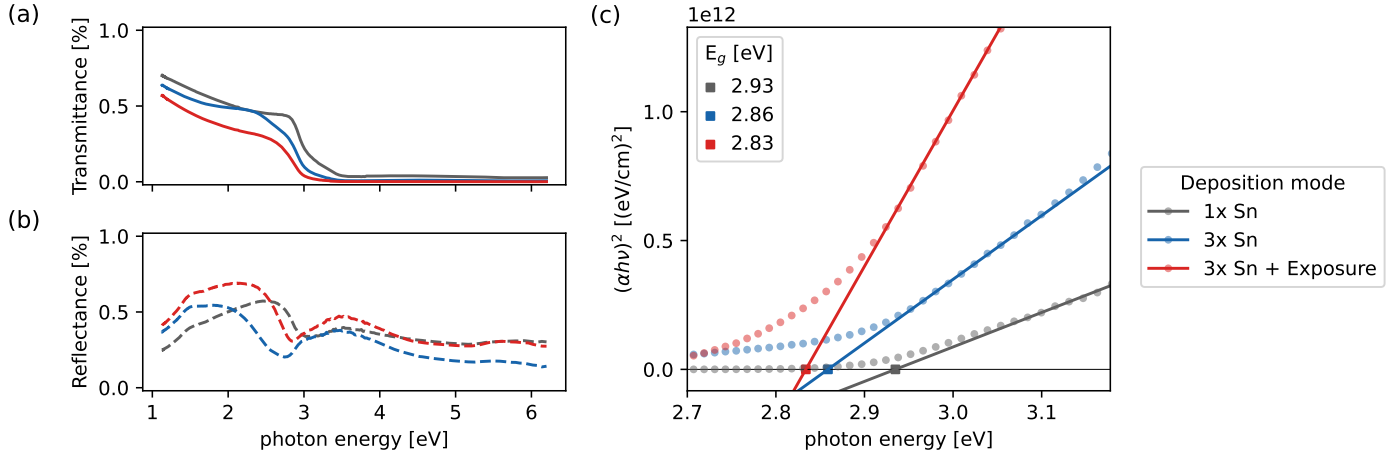

Fig. S3 Optical properties of the SnO films for each deposition mode, showing: **(a)** transmittance, **(b)** reflectance and **(c)** a Tauc plot with extracted band gap energies. The films have all undergone post deposition annealing at 350°C.

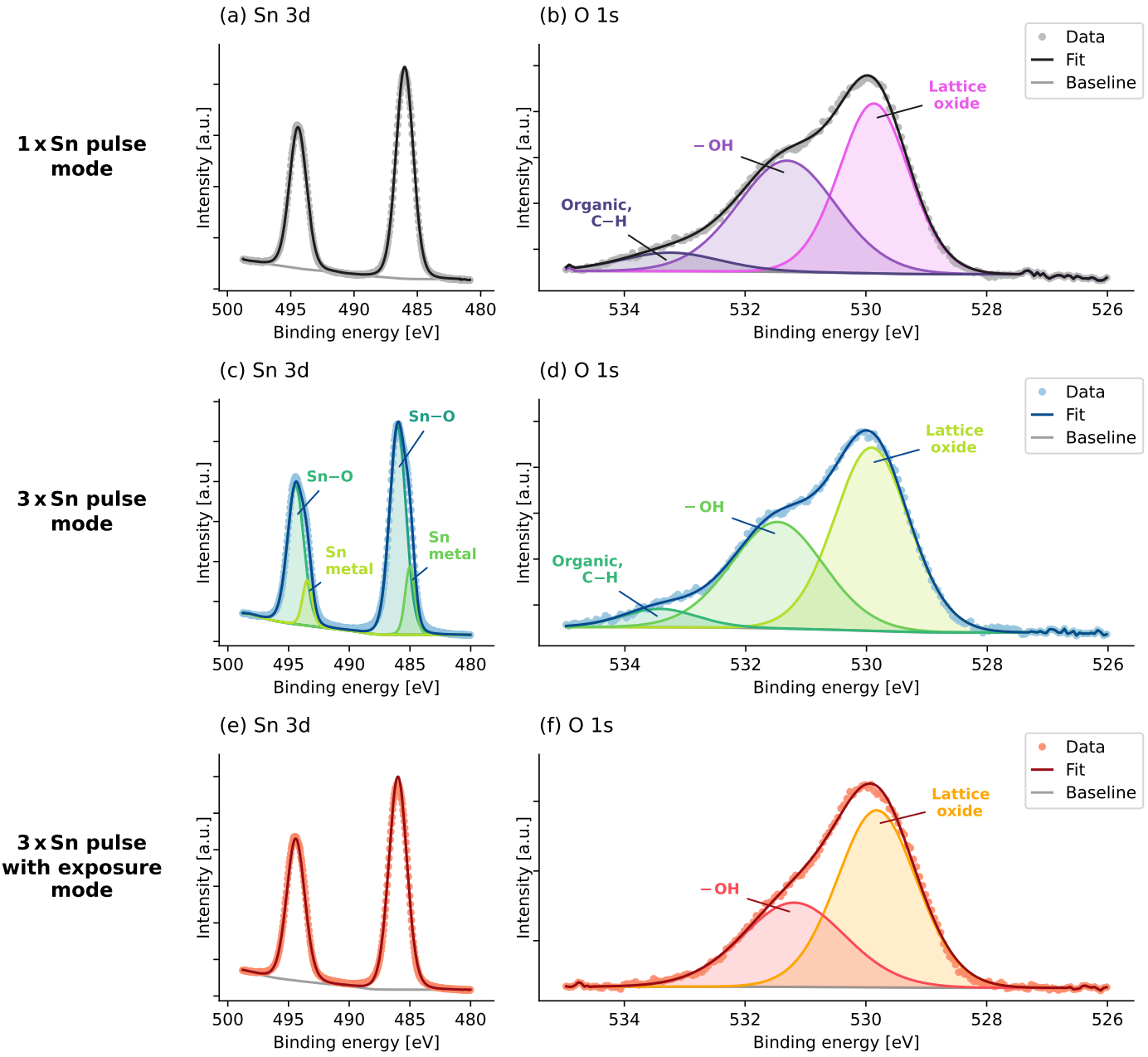

Fig. S4 Comparison of XPS spectra of Sn 3d and O 1s core levels for the three deposition modes. XPS was performed *ex-situ*, without any etching of the SnO surface.

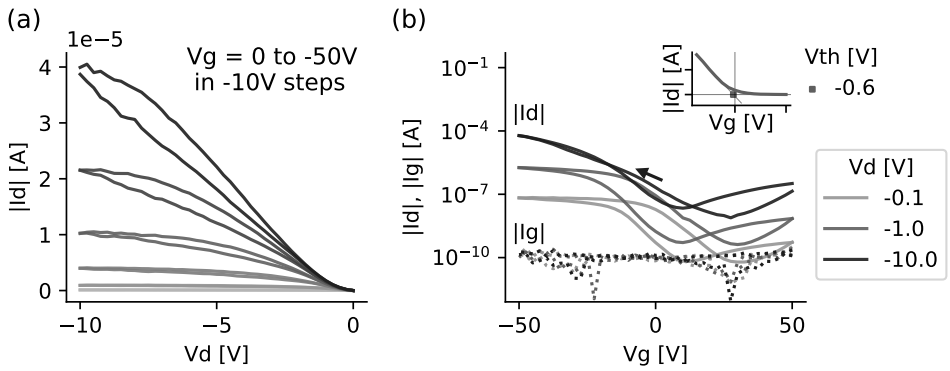

Fig. S5 Performance of SnO TFTs deposited in single pulse mode: **(a)** shows the output curves for V_g from 0 to -50 V; **(b)** shows the gate transfer curves (I_d) and gate leakage current (I_g, dotted lines) for 3 values of V_d, with the extracted threshold voltage at V_d = -1 V (inset).

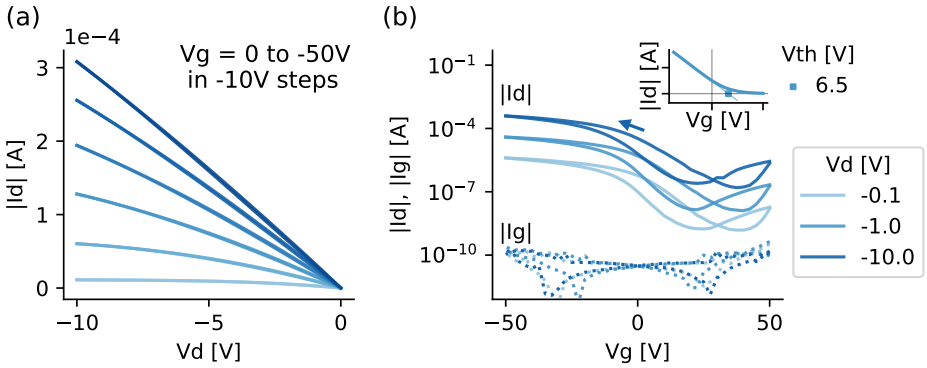

Fig. S6 Performance of SnO TFTs deposited in 3 Sn pulse mode: **(a)** shows the output curves for V_g from 0 to -50 V; **(b)** shows the gate transfer curves (I_d) and gate leakage current (I_g, dotted lines) for 3 values of V_d, with the extracted threshold voltage at V_d = -1 V (inset).

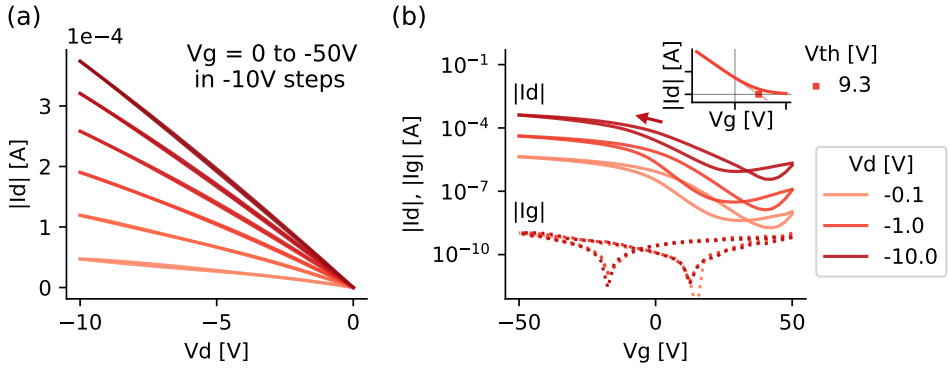

Fig. S7 Performance of SnO TFTs deposited in 3×Sn pulse with exposure mode: **(a)** shows the output curves for V_g from 0 to -50 V; **(b)** shows the gate transfer curves (I_d) and gate leakage current (I_g, dotted lines) for 3 values of V_d, with the extracted threshold voltage at V_d = -1 V (inset).