Electronic Supplementary Information

Optimization of solution-processed amorphous cadmium gallium oxide for high-performance thin-film transistors

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Table S1. Electrical performances of optimized *a*-$Cd_{5.5}Ga_{4.5}O_{12.25}$ TFT annealed at 500 °C :Comparison before and after 7 days exposure to ambient air.

	Mobility ($cm^2V^{-1}S^{-1}$)	V_{on} **(V)**	V_{th} **(V)**	**SS (V/dec)**
Initial	11.9	-5	4.49	1.71
One week exposure to ambient air	12.15	-8	3.41	1.31

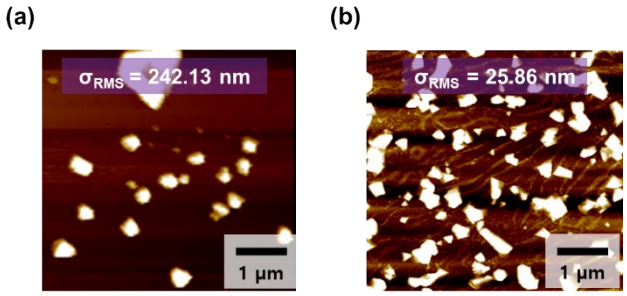

Figure S1. Atomic force microscopy (AFM) images of CdO thin-films annealed at (a) 500°C and (b) 350 °C.

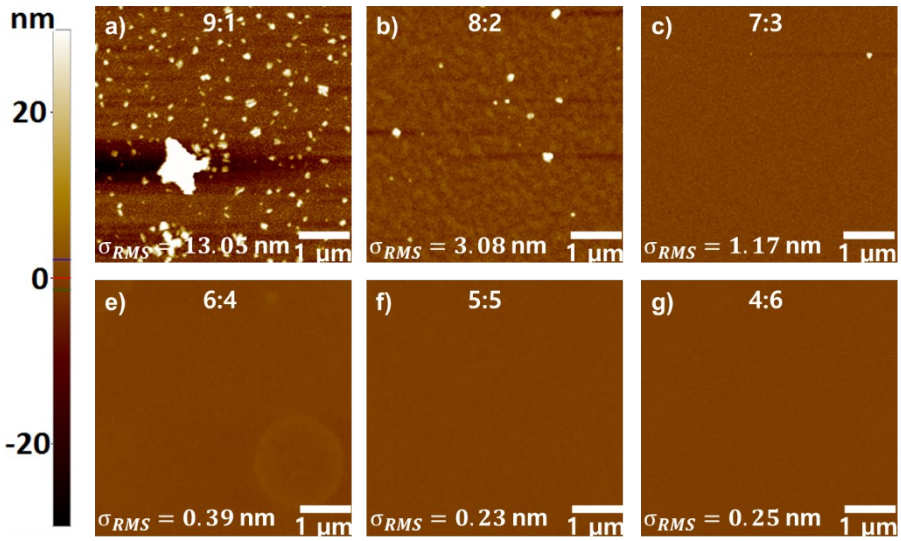

Figure S2. AFM images of CdGaO thin films annealed at 500 °C with Cd:Ga ratios of a) 9:1, b) 8:2, c) 7:3, d) 6:4, e) 5:5, and f) 4:6.

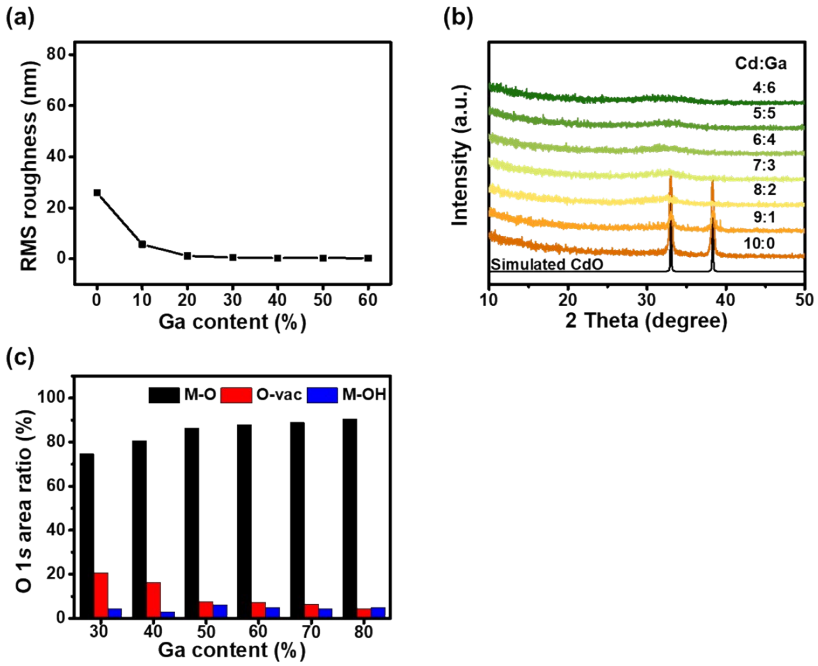

Figure S3. a) Root mean square surface roughness data for CdGaO films with Cd:Ga ratios ranging from 10:0 to 4:6, annealed at 350 °C. b) XRD patterns of CdGaO thin films with Cd:Ga ratios ranging from 10:0 to 4:6, annealed at 350 °C. c) Areal ratios of M–O–M, M–O_{vac}, and M–OH bonding states obtained from O 1s XPS profiles of *a*-CdGaO thin films with Cd:Ga ratios ranging from 7:3 to 2:8, annealed at 350 °C, after surface sputtering.

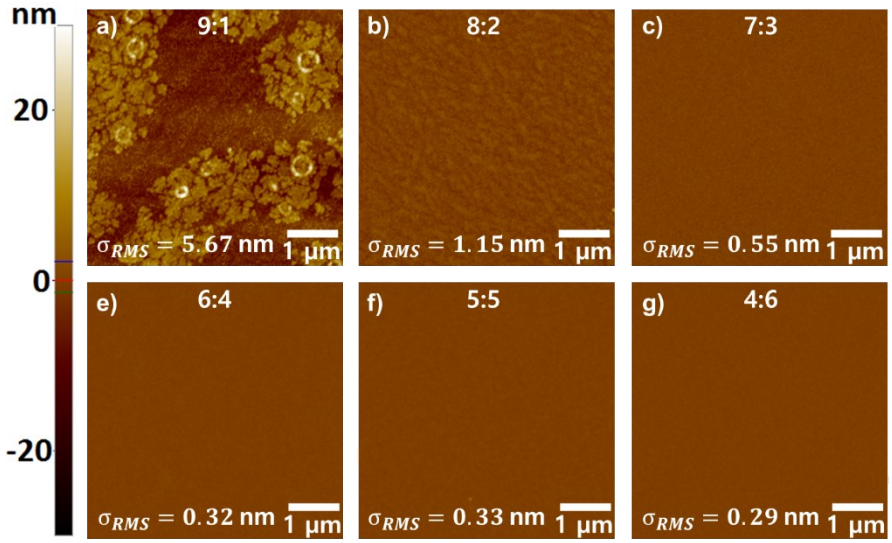

Figure S4. AFM images of CdGaO thin films annealed at 350 °C with Cd:Ga ratios of a) 9:1, b) 8:2, c) 7:3, d) 6:4, e) 5:5, and f) 4:6.

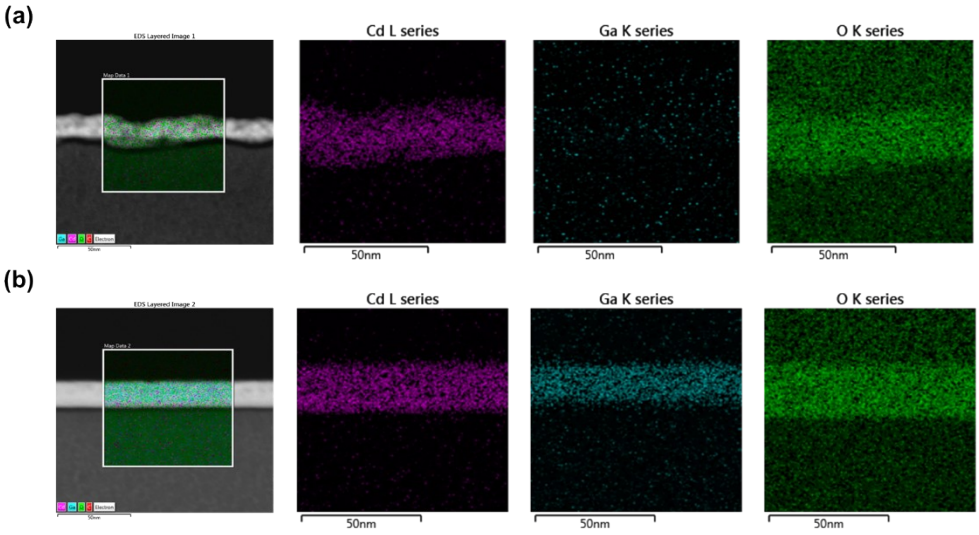

Figure S5. Energy-dispersive X-ray spectroscopy (EDS) mapping image of a) CdO thin-film and b) optimized *a*-$Cd_{5.5}Ga_{4.5}O_{12.25}$ thin-film annealed at 500°C.

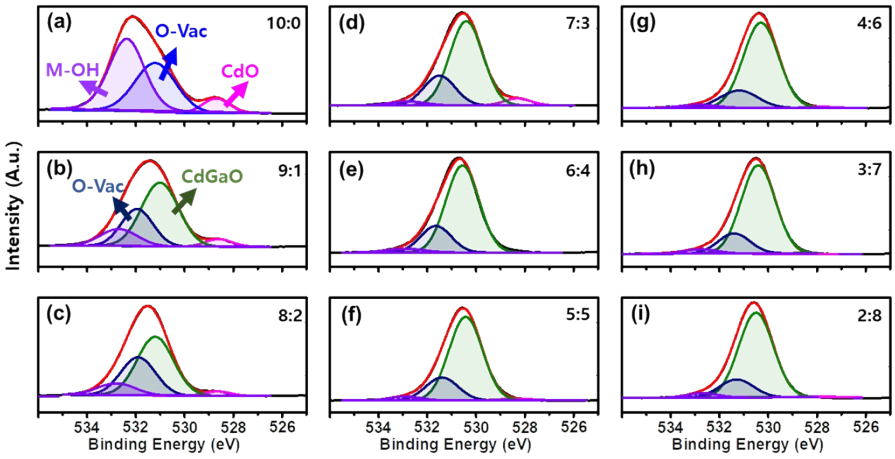

Figure S6. XPS O 1*s* analysis of CdGaO thin films annealed at 500 °C with Cd:Ga ratios of a) 10:0, b) 9:1, c) 8:2 d) 7:3, e) 6:4, f) 5:5, g) 4:6, h) 3:7, and i) 2:8 after surface sputtering.

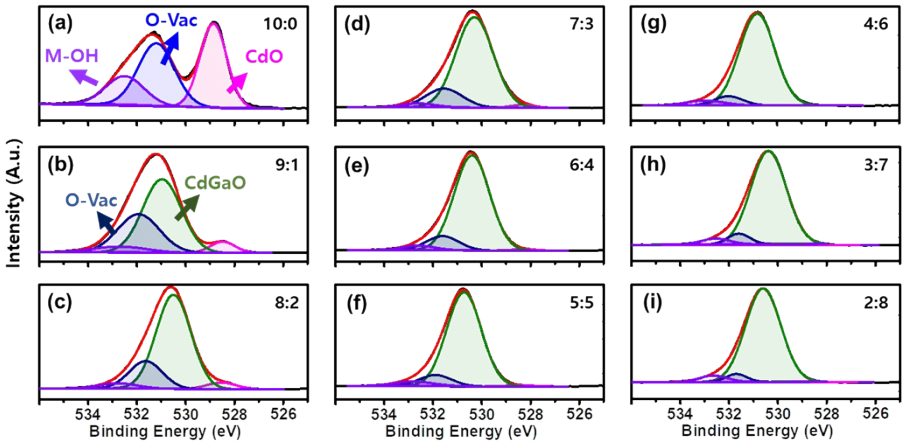

Figure S7. XPS O 1*s* analysis of CdGaO thin films annealed at 350 °C with Cd:Ga ratios of a) 10:0, b) 9:1, c) 8:2 d) 7:3, e) 6:4, f) 5:5, g) 4:6, h) 3:7, and i) 2:8 after surface sputtering.

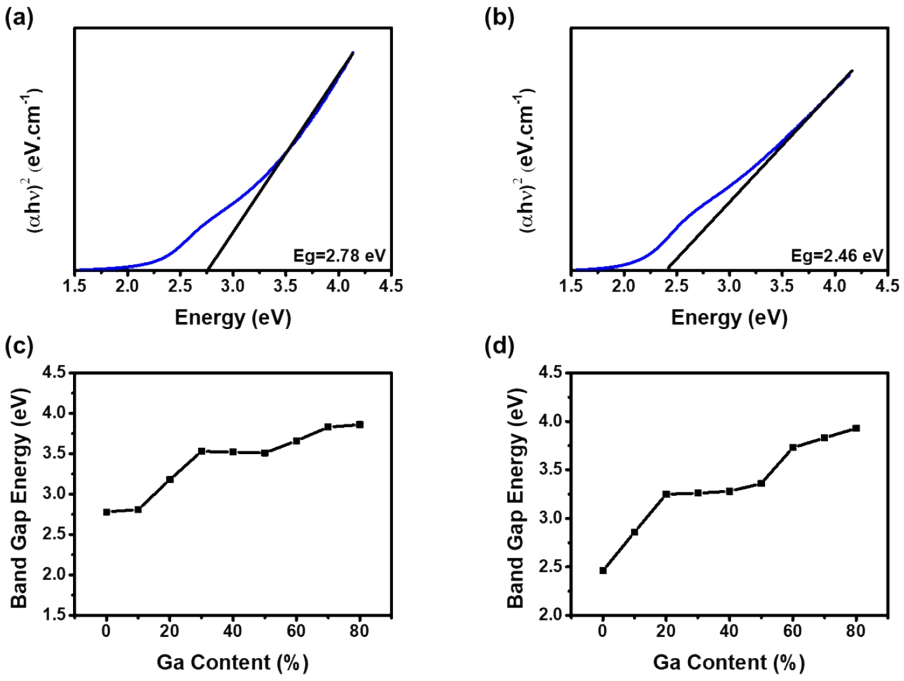

Figure S8. Tauc plots of CdO thin films annealed at a) 500 and b) 350 °C, and bandgap value of CdGaO thin films as a function of the amount of Ga incorporated, with ratios ranging from 10:0 to 2:8 for films annealed at c) 500 and d) 350 °C.

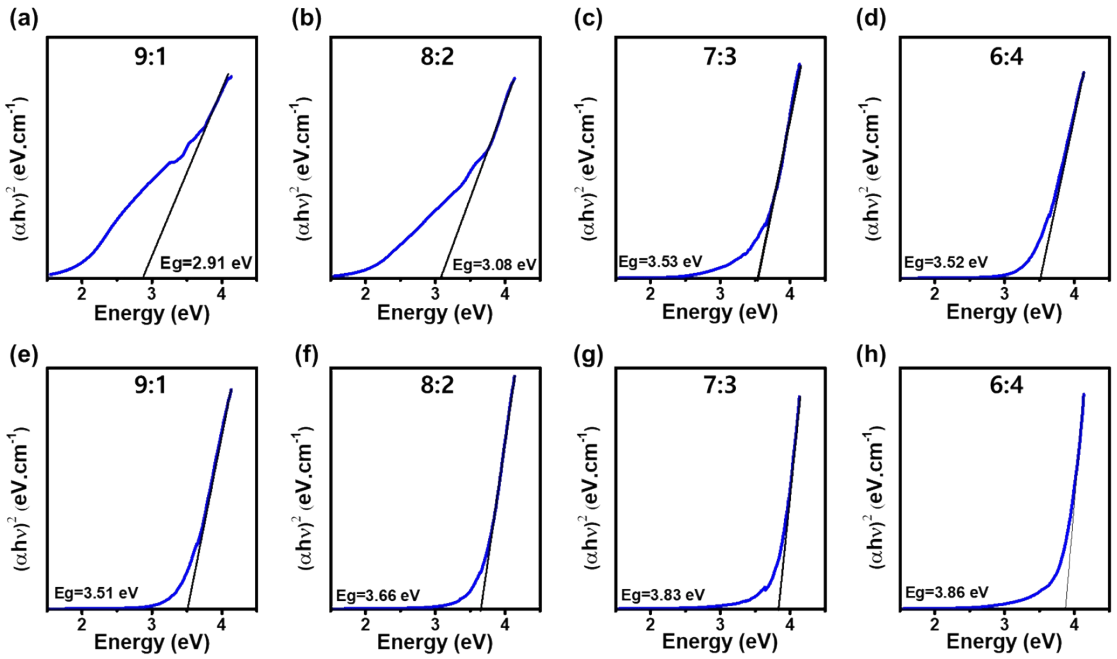

Figure S9. Tauc plots of CdGaO thin films with Cd/Ga ratios ranging from 9:1 to 2:8, annealed at 500 °C.

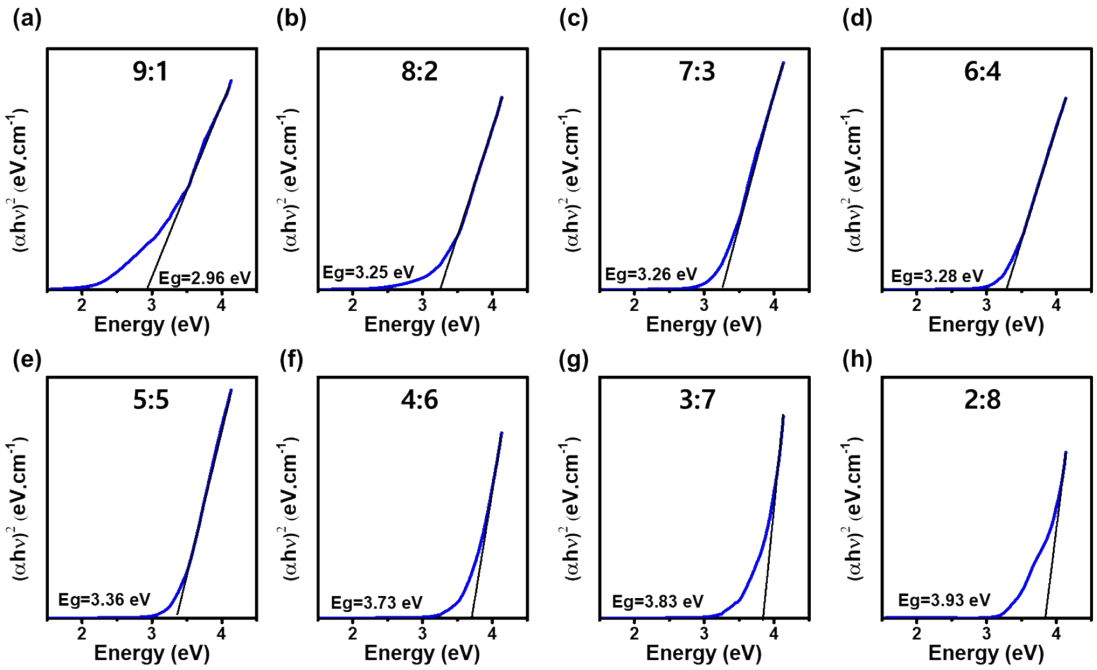

Figure S10. Tauc plots of CdGaO thin films with Cd/Ga ratios ranging from 9:1 to 2:8, annealed at 350 °C.

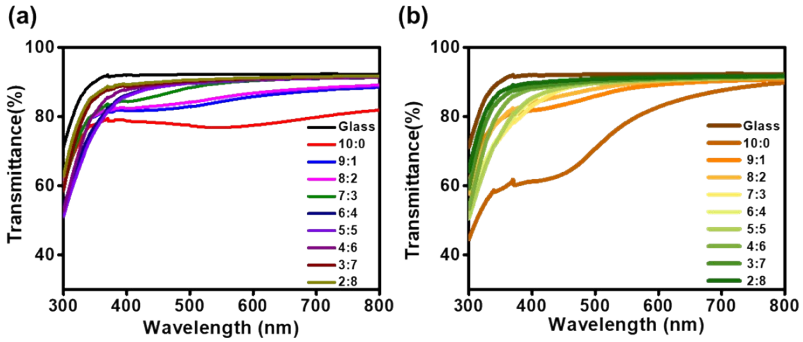

Figure S11. UV–vis spectra of CdGaO-based thin films with compositional ratios ranging from 10:0 to 2:8, annealed at a) 500 and b) 350 °C.

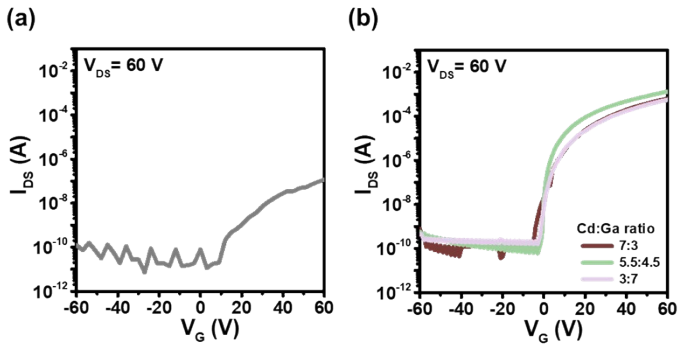

Figure S12. a) Transfer characteristics of the CdO-based TFT, annealed at 350 °C. b) Transfer characteristics of the CdGaO-based TFT with Cd/Ga ratios ranging from 7:3 to 3:7, annealed at 350 °C.

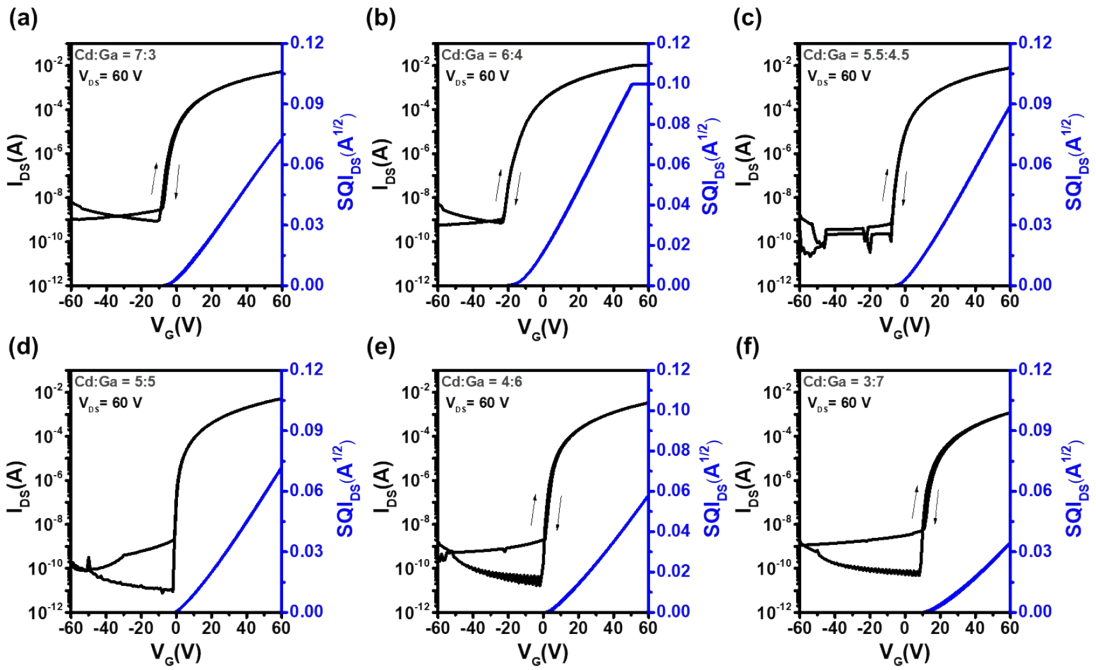

Figure S13. Transfer curves of the CdGaO TFT with Cd:Ga ratios ranging from 7:3 to 3:7, annealed at 500 °C.

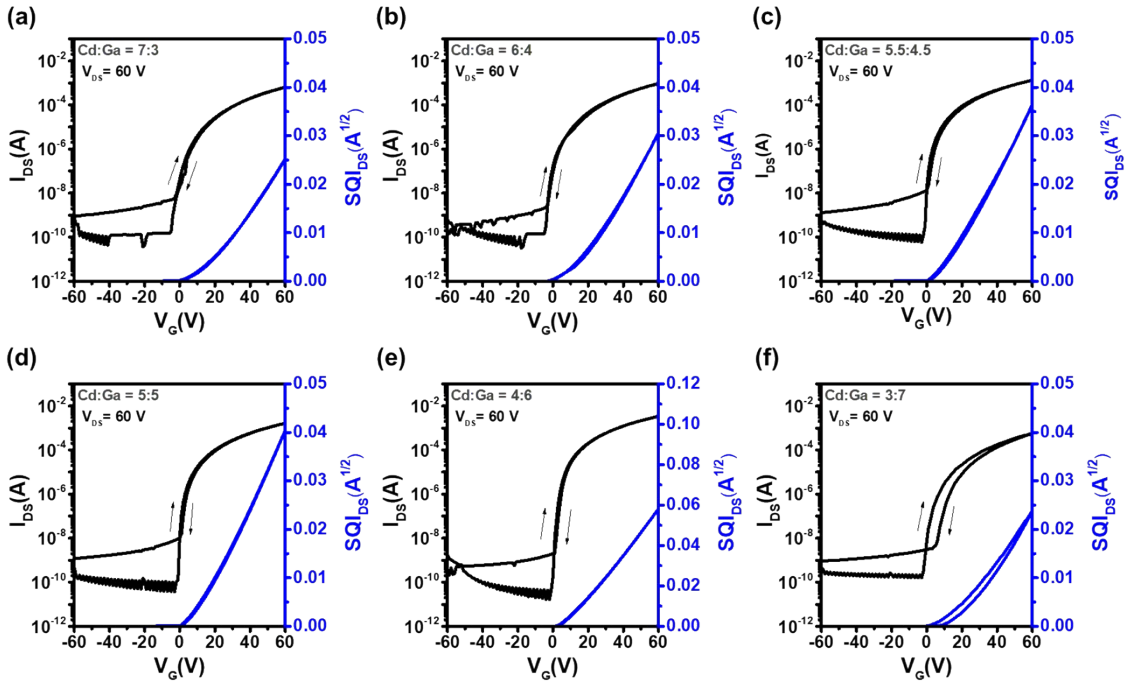

Figure S14. Transfer curves of the CdGaO TFT with Cd:Ga ratios ranging from 7:3 to 3:7, annealed at 350 °C.

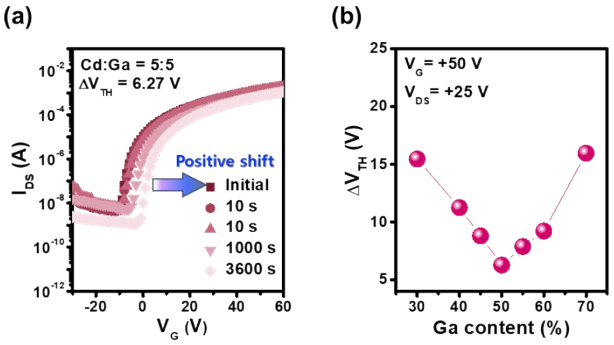

Figure S15. a) Transfer characteristics of the optimized *a*-$Cd_5Ga_5O_{12.5}$ TFT under positive bias stress (V_G = 50 V; V_{DS} = 25 V) for 3600 s annealed at 350 °C. b) Threshold voltage shift value of the *a*-CdGaO-based TFT with Cd/Ga ratios ranging from 7:3 to 3:7 under above-mentioned positive bias stress, annealed at 350 °C.

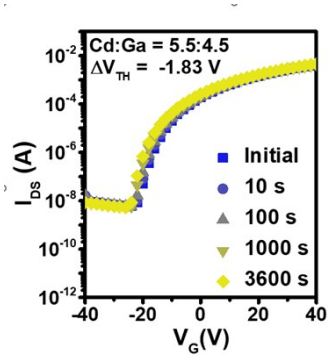

Figure S16. Transfer characteristics of the optimized *a*-$Cd_{5.5}Ga_{4.5}O_{12.25}$ TFT under negative bias stress (V_G = -50 V; V_{DS} = 25 V) for 3600 s, annealed at 500 °C.

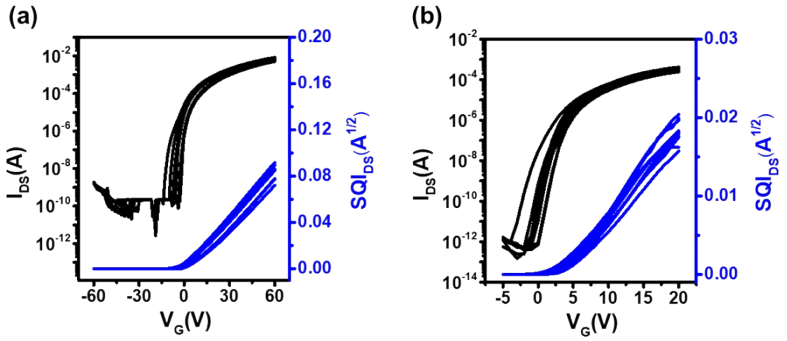

Figure S17. Transfer curves of optimized *a*-$Cd_{5.5}Ga_{4.5}O_{12.25}$ TFTs annealed at 500 °C on a) SiO_2 with simple wet etching and b) glass substrate with solution-processed alumina as dielectric obtained via the standard lithography patterning process.

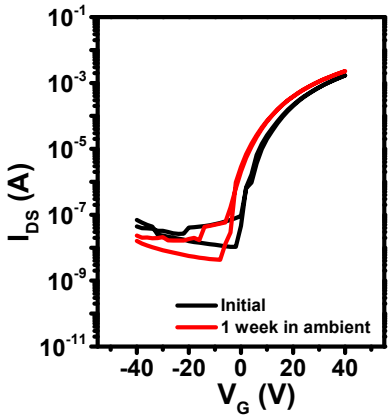

Figure 18. Transfer characteristics of the optimized *a*-$Cd_{5.5}Ga_{4.5}O_{12.25}$ TFT annealed at 500^{o}C : Comparison before and after one week exposure to ambient air.

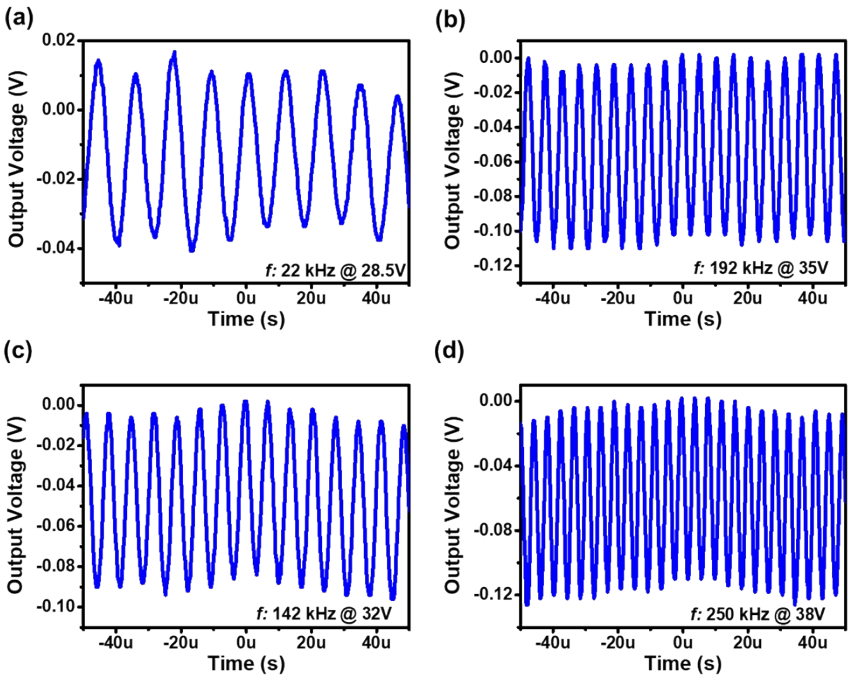

Figure S19. Output waveform of the seven-stage ring oscillator operating with supply voltages of a) 28.5, b) 32, c) 35, and d) 38 V and the optimized *a*-$Cd_{5.5}Ga_{4.5}O_{12.25}$ TFT.