

Supplementary materials

Effect of interfacial SiO_2 layer thickness on the memory performances in HfAlO_x -based ferroelectric tunnel junction for neuromorphic system

Yongjin Park,^{†a} Jihyung Kim,^{†a} Sunghun Kim^a, Dahye Kim^a, Wonbo Shim^{*b}, and Sungjun Kim^{*a}

^a Division of Electronics and Electrical Engineering, Dongguk University, Seoul 04620, South Korea.

^b Department of Electrical and Information Engineering, Seoul National University of Science and Technology, Seoul 01811, South Korea

E-mail: wbshim@seoultech.ac.kr, sungjun@dongguk.edu

[†]The authors contributed equally to this work.

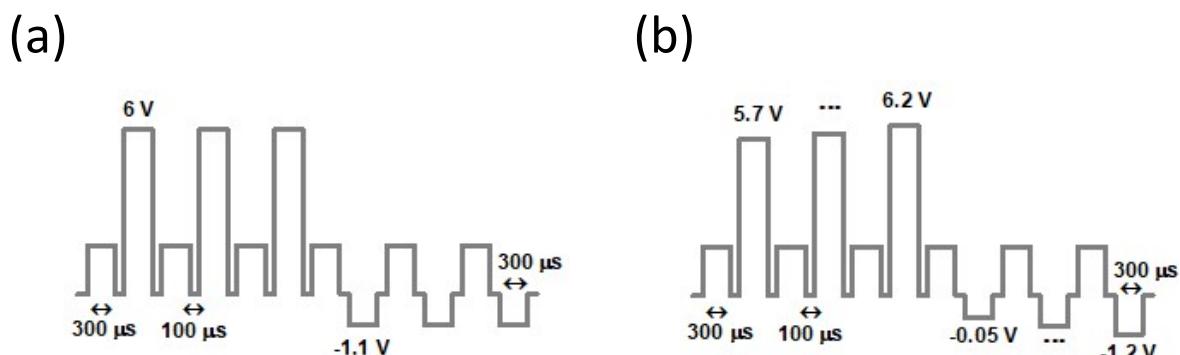


Fig. S1 (a) Identical and (b) incremental pulse schemes for potentiation and depression.

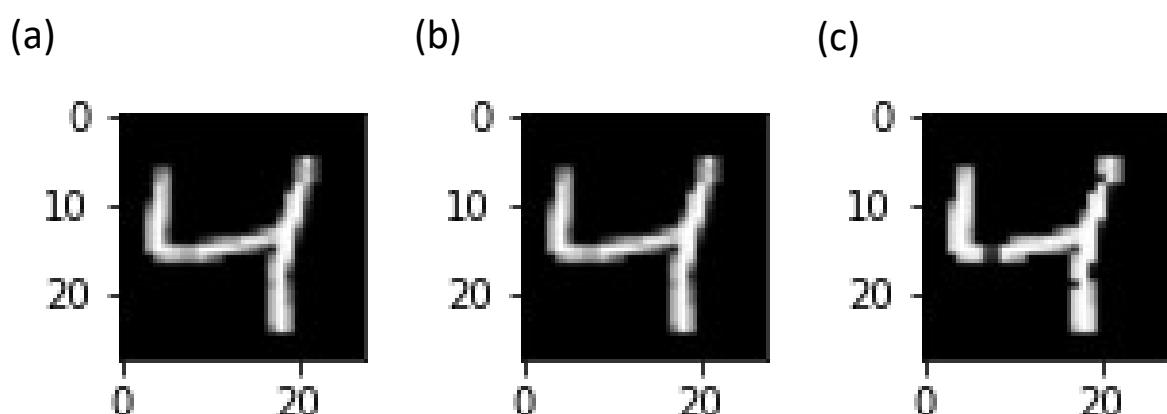


Fig. S2 Hand-written recognized MNIST numbers with respect to cycles of training of number 4 of (a) the ideal, (b) the incremental pulse scheme, and (c) the identical pulse scheme.