Electronic Supplementary Information

Reverse Schmitt trigger with adjustable hysteresis window implemented by mesoporous silica electrolyte gated transistors

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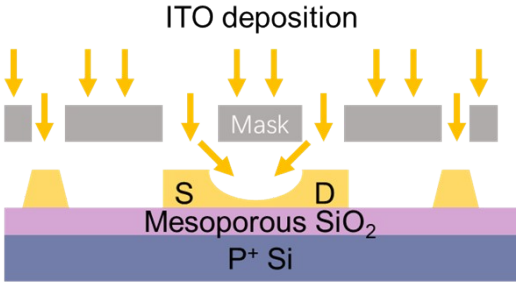

Fig. S1 Schematic diagram of the process for a self-assembled ITO TFT.

Using a nickel shadow mask, ITO channels and source drain electrodes were deposited on mesoporous silica films by RF magnetron sputtering. Leave approximately 100 μm gap between the shadow mask and substrate to complete the self-assembly of the channel with the source and drain electrodes. Most ITO particles are directly deposited on the corresponding areas of the electrode pattern to form a source and drain electrode with a thickness of approximately 170 nm. The channel is obtained through diffraction. Due to 100 μm gap, a small portion of ITO particles will bypass the masking area between the electrodes and deposit a channel approximately 30 nm thick between the source and drain electrodes. Similar methods have been reported.[1, 2]

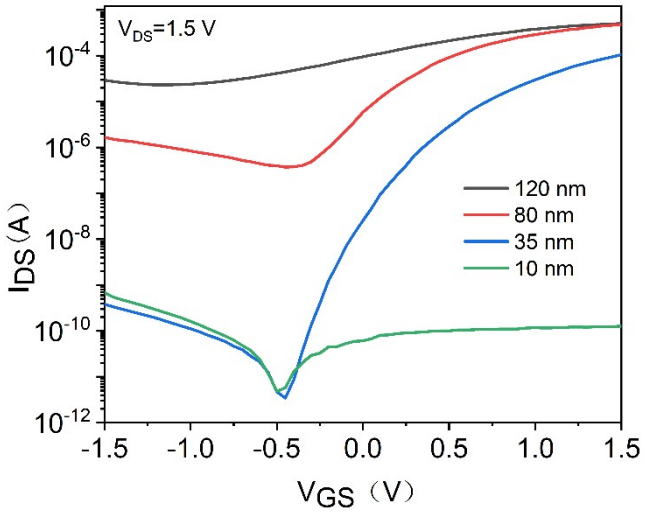

Fig. S2 Transfer curves of devices from the same batch but with different spatial locations.

By the method described above, various channel thicknesses can be simultaneously prepared on the same substrate have different channel conductivity, as shown in Fig. S2.

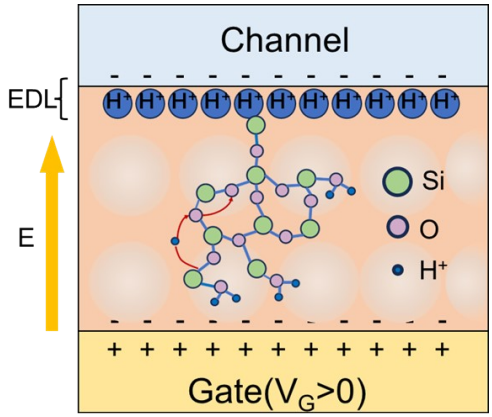

Fig. S3 Schematic of how the mesoporous silica EDL works.

Ordered mesoporous silica has abundant silicon hydroxyl functional groups on its surface and pore walls, which can form channels for proton transitions. When a voltage is applied to the gate, protons in mesoporous silica can migrate and form ion accumulation layers at the interface between the gate and electrolyte, as well as between semiconductor and electrolyte. These accumulated ions mirror the charges in the gate and induce carrier charges in the semiconductor channel. Under steady-state, almost all electric fields act on this double layer, with only a small portion of the potential drop acting inside the electrolyte. Due to the small spacing of the double layer (~1 nm), it has a huge specific capacitance (>1 μF/cm^2).

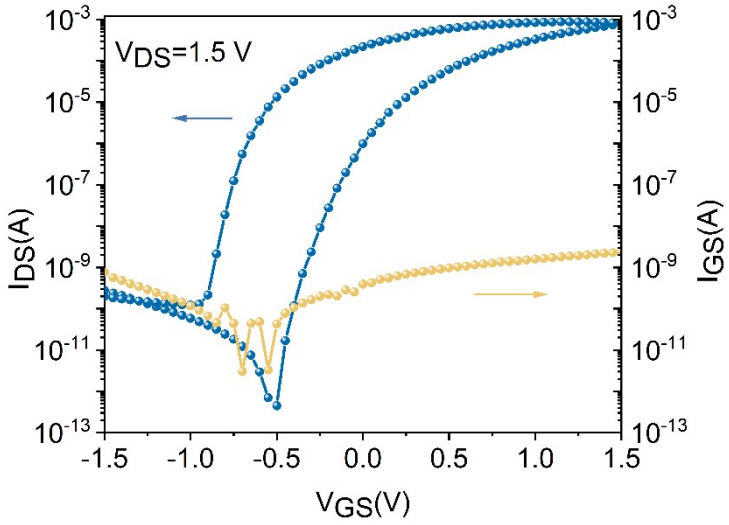

Fig. S4 Transfer characteristics at a fixed V_{DS} of 50 mV/s and the leakage current.

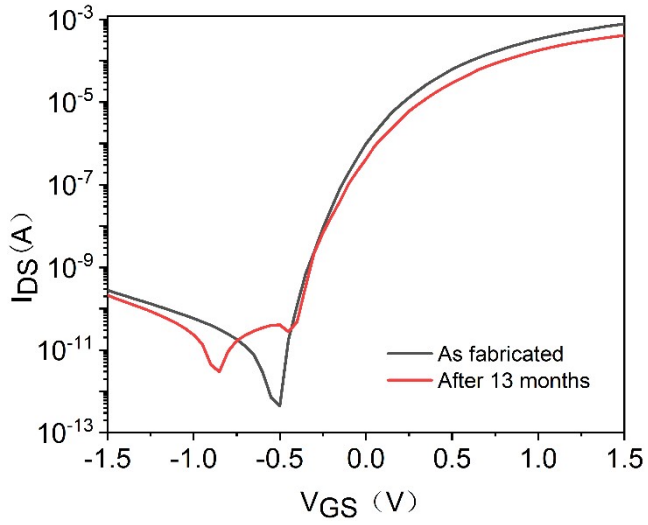

Fig. S5 Transfer curve of the mesoporous silica oxide TFT, tested in different time.

Table S1 Transistor performance parameters extracted from transfer curves.

	m($cm^2V^{-1}s^{-1}$)	**SS(mV/decade)**	**I_{ON}/I_{OFF}**	**V_{TH}(V)**
As fabricated	24.2	90.5	1.03×10^7	0.11
After 13 months	13.7	92.9	6.9×10^6	0.16

REFERENCE

1 Y. Liu, X. Wan, L. Zhu, Y. Shi, and Q. Wan, EEE Electron Device Letters, 2014, 35, 1257.

2 J. Guo, Y. Liu, Y. Li, F.Li, F. Huang, ACS Appl. Mater. Interfaces, 2020, **12**, 5006.