Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C.


Supporting Information

# Designing Buried-Gate InGaZnO Transistors for High-Yield and Reliable Switching Characteristics

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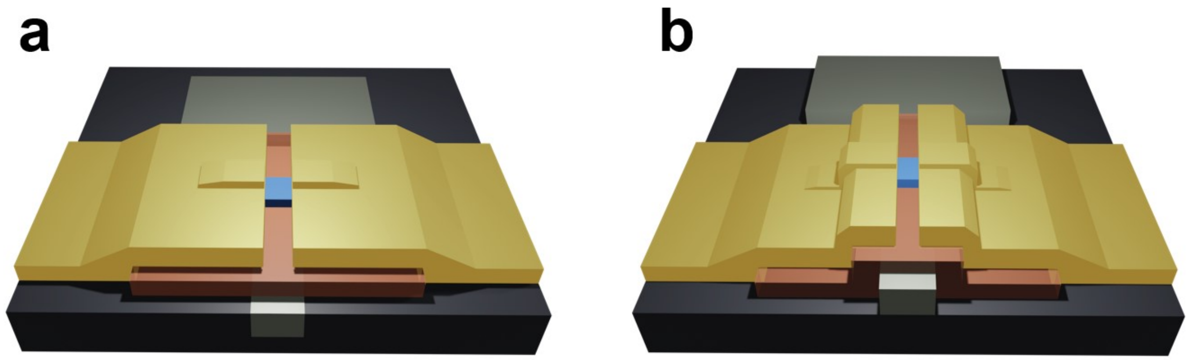


**Fig. S1** 3D schematic diagrams of (a) buried and (b) control gate transistors

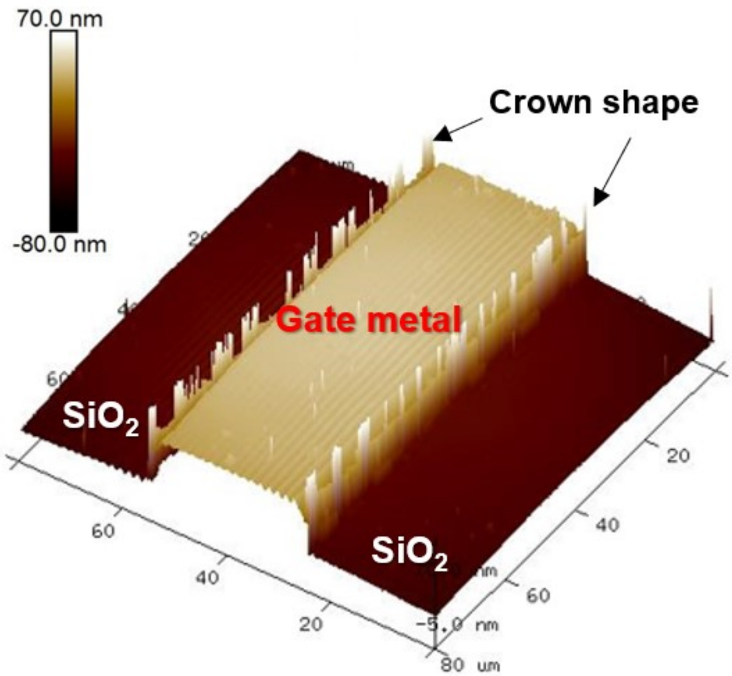


**Fig. S2** AFM image of control device with protruding back gate electrode, showing crown-shaped edge

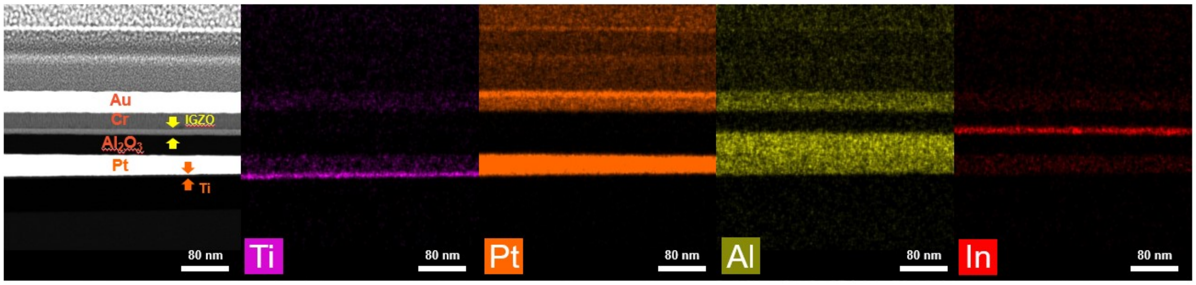


**Fig. S3** Energy dispersive spectroscopy mapping data of the elements constituting the buried gate transistor

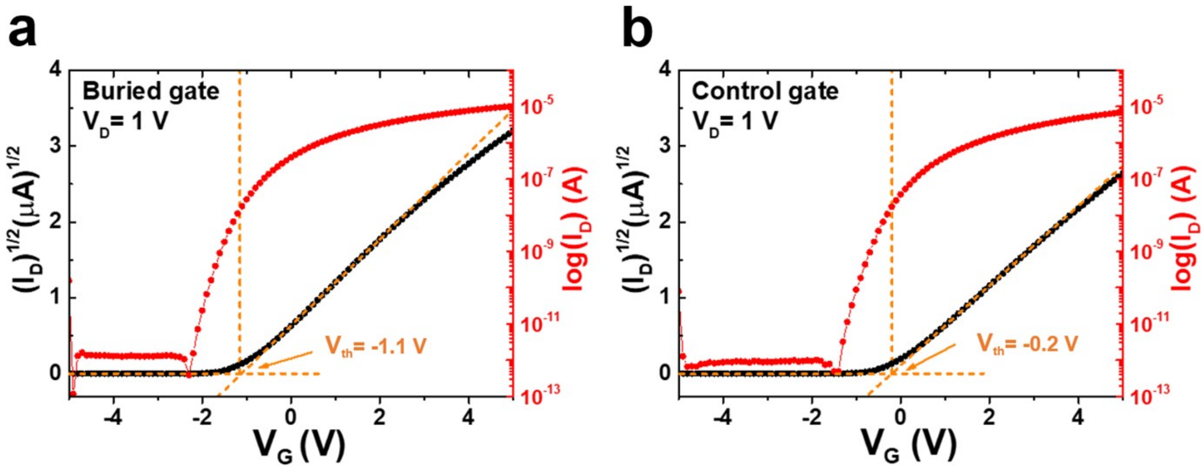


**Fig. S4** Threshold voltage extraction of (a) buried and (b) control gate transistors at $V_D = 1$ V

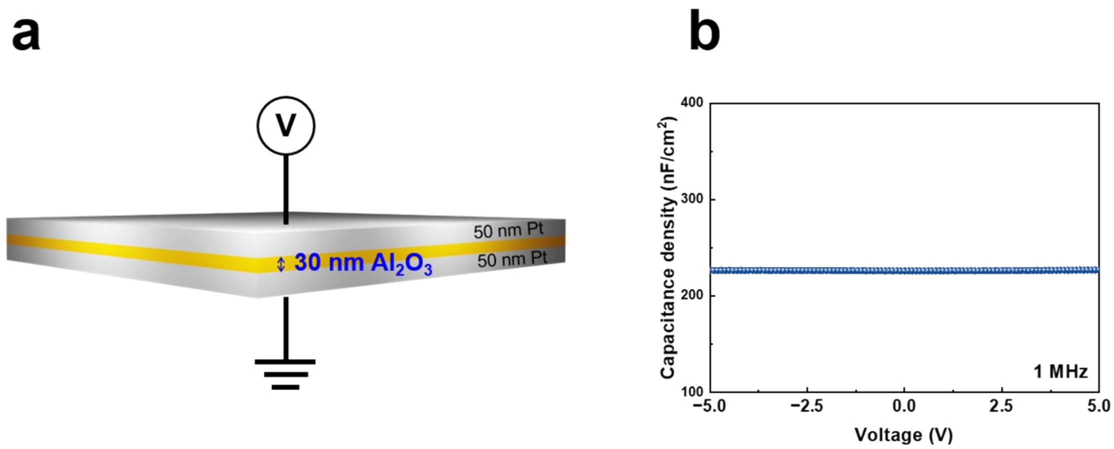


**Fig. S5** (a) 3D Schematic image of Pt/$Al_2O_3$/Pt capacitor. (b) capacitance-voltage characteristic of the Pt/$Al_2O_3$/Pt capacitor.

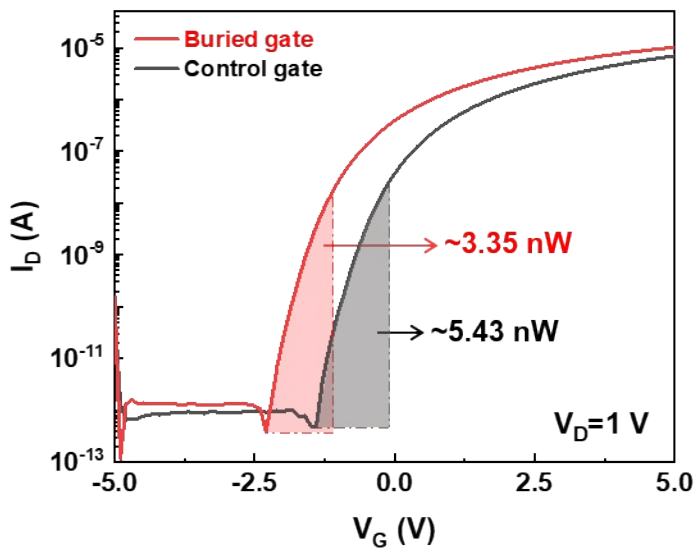


**Fig. S6** Comparison of switching power for buried- and control-gate transistors.

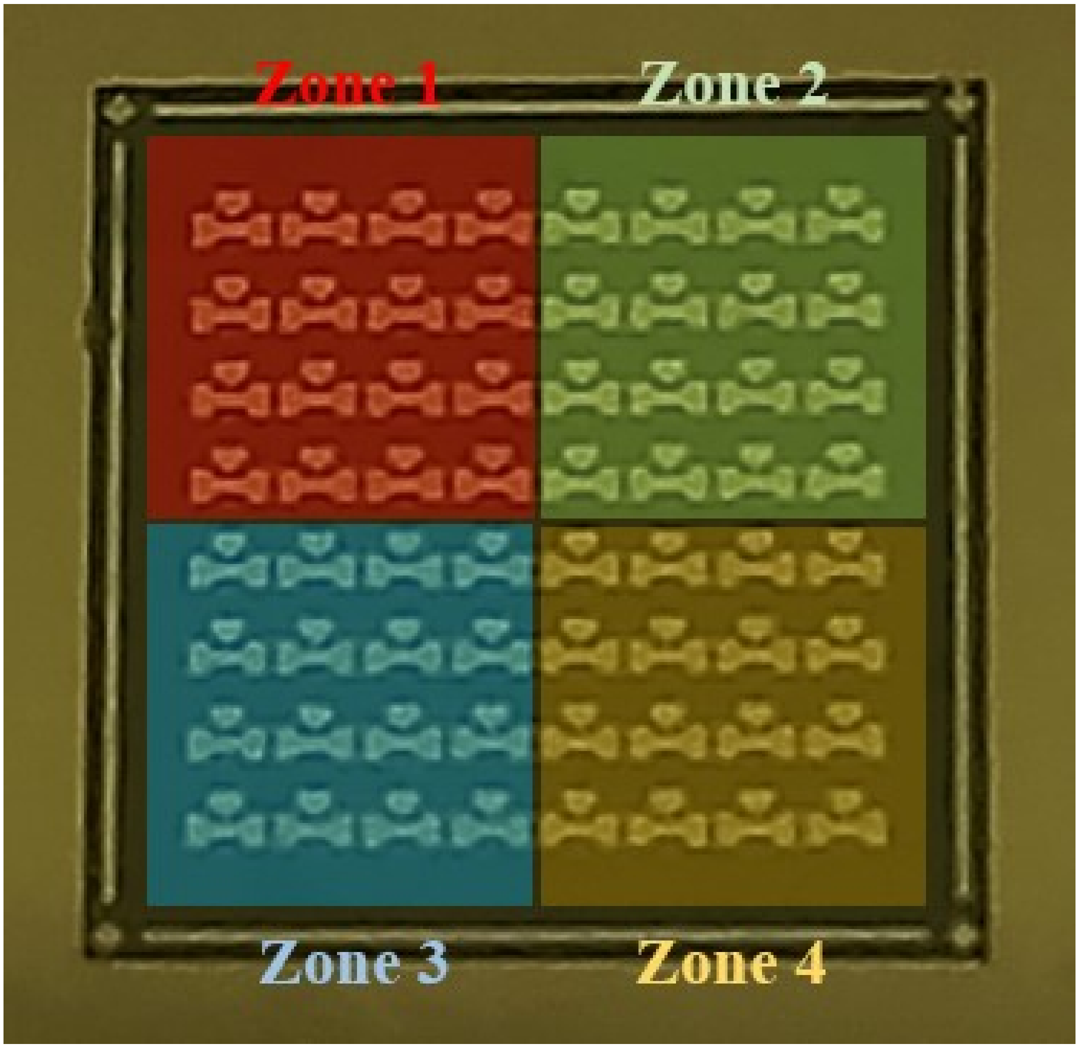


**Fig. S7** Real image showing 8×8 buried-gate transistor array with four zones.

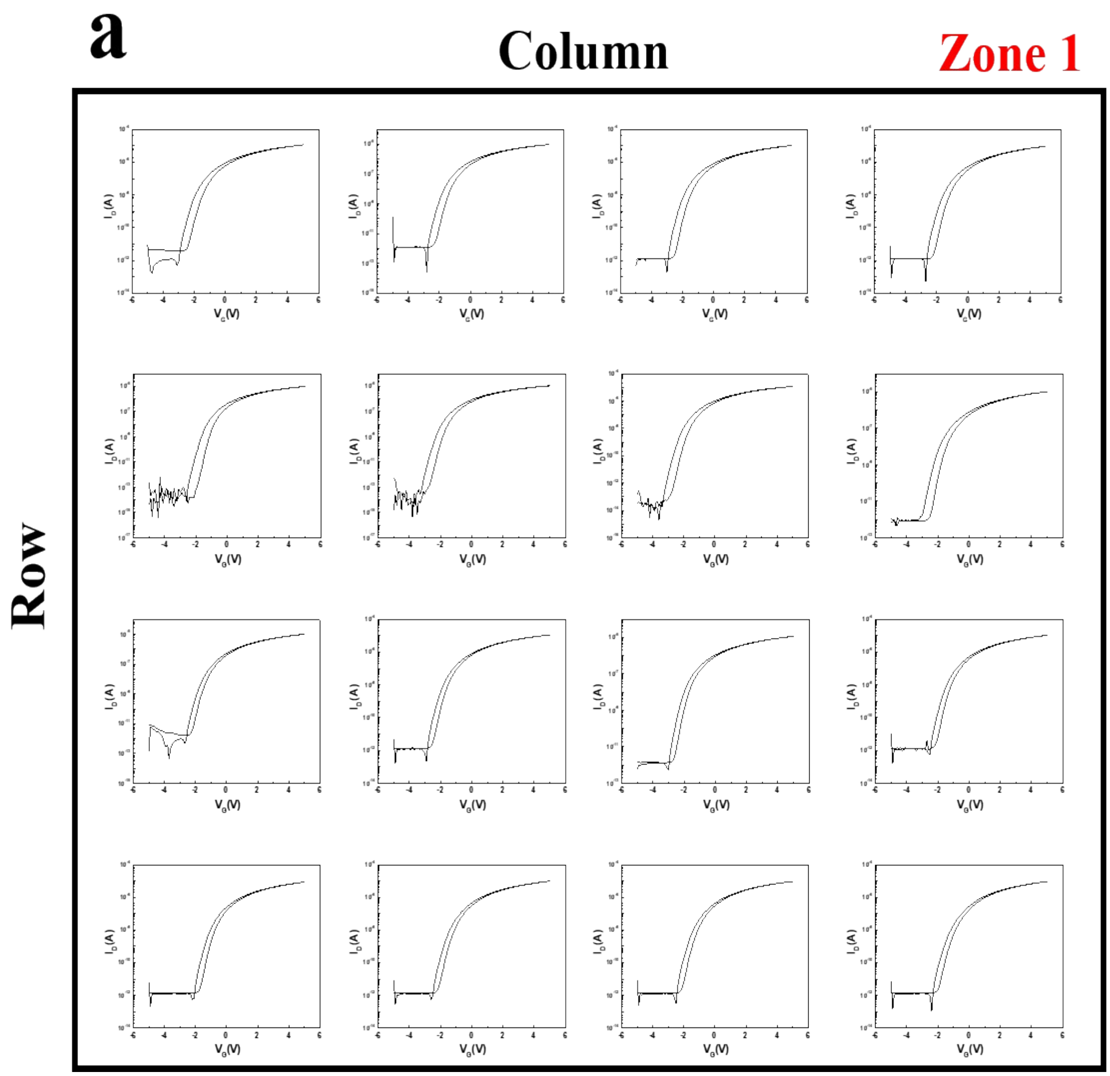


**Fig. S8a** Transfer characteristics of each buried-gate transistor located in zone 1.

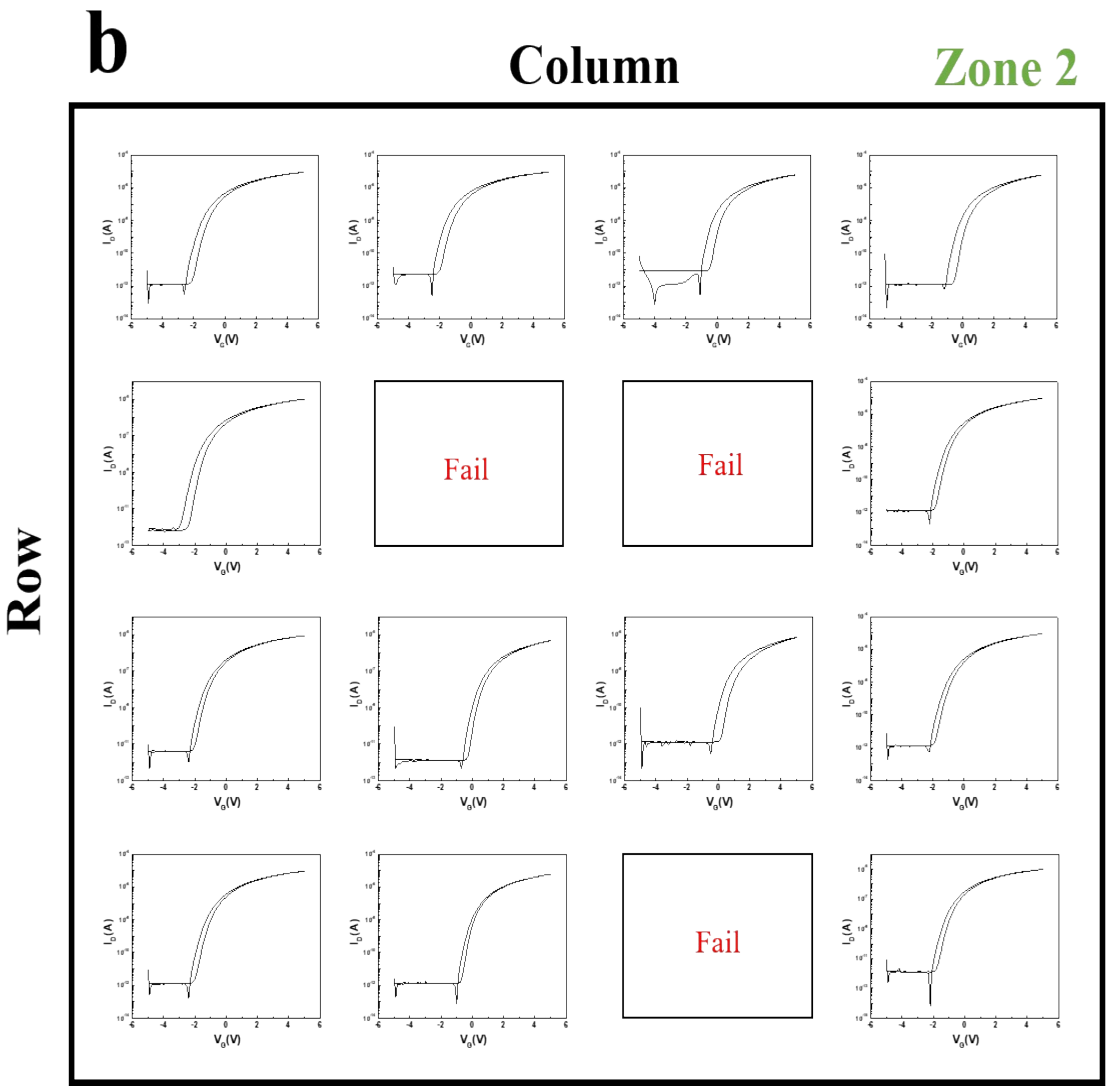


**Fig. S8b** Transfer characteristics of each buried-gate transistor located in zone 2.

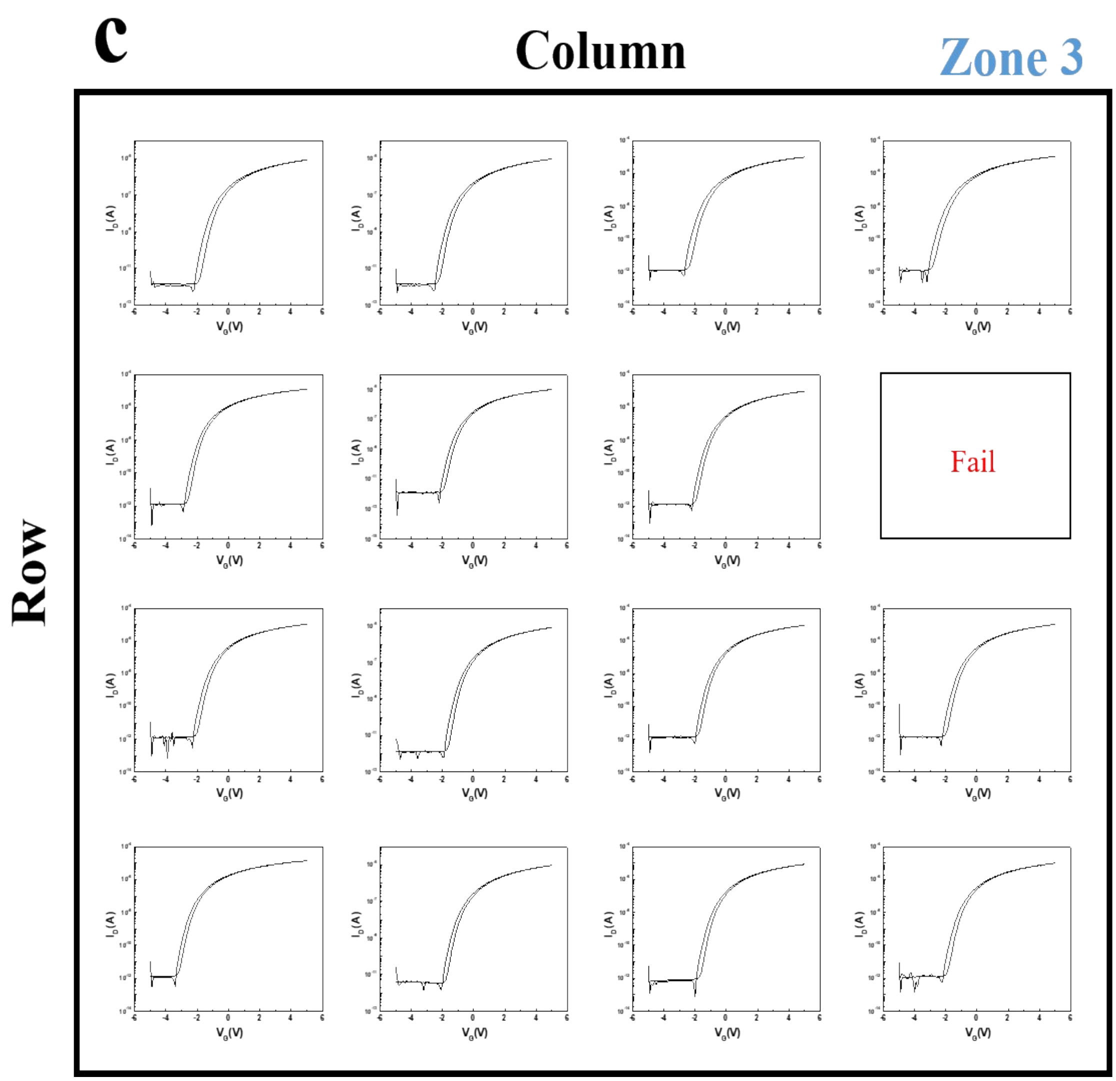


**Fig. S8c** Transfer characteristics of each buried-gate transistor located in zone 3.

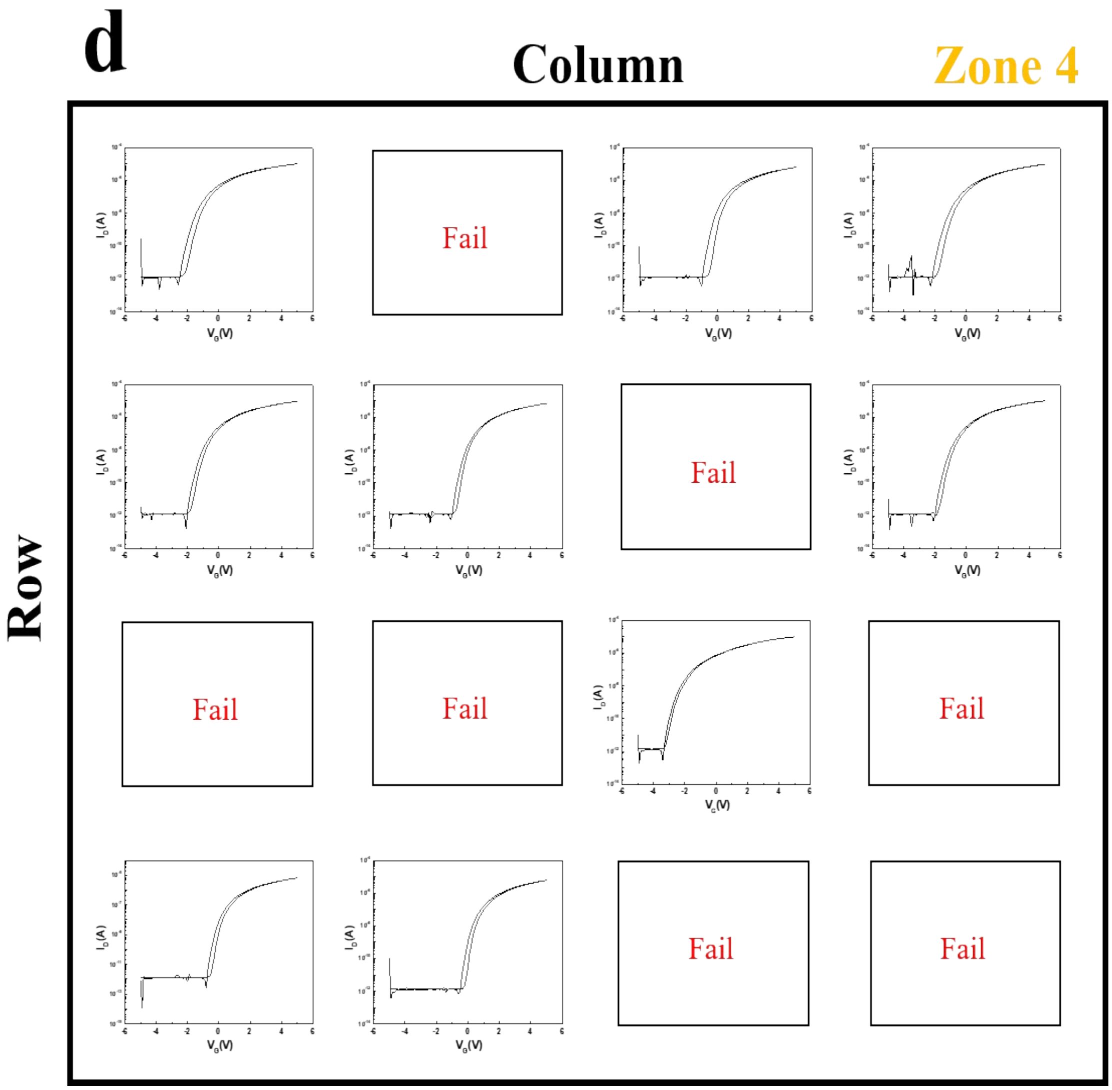


**Fig. S8d** Transfer characteristics of each buried-gate transistor located in zone 4.

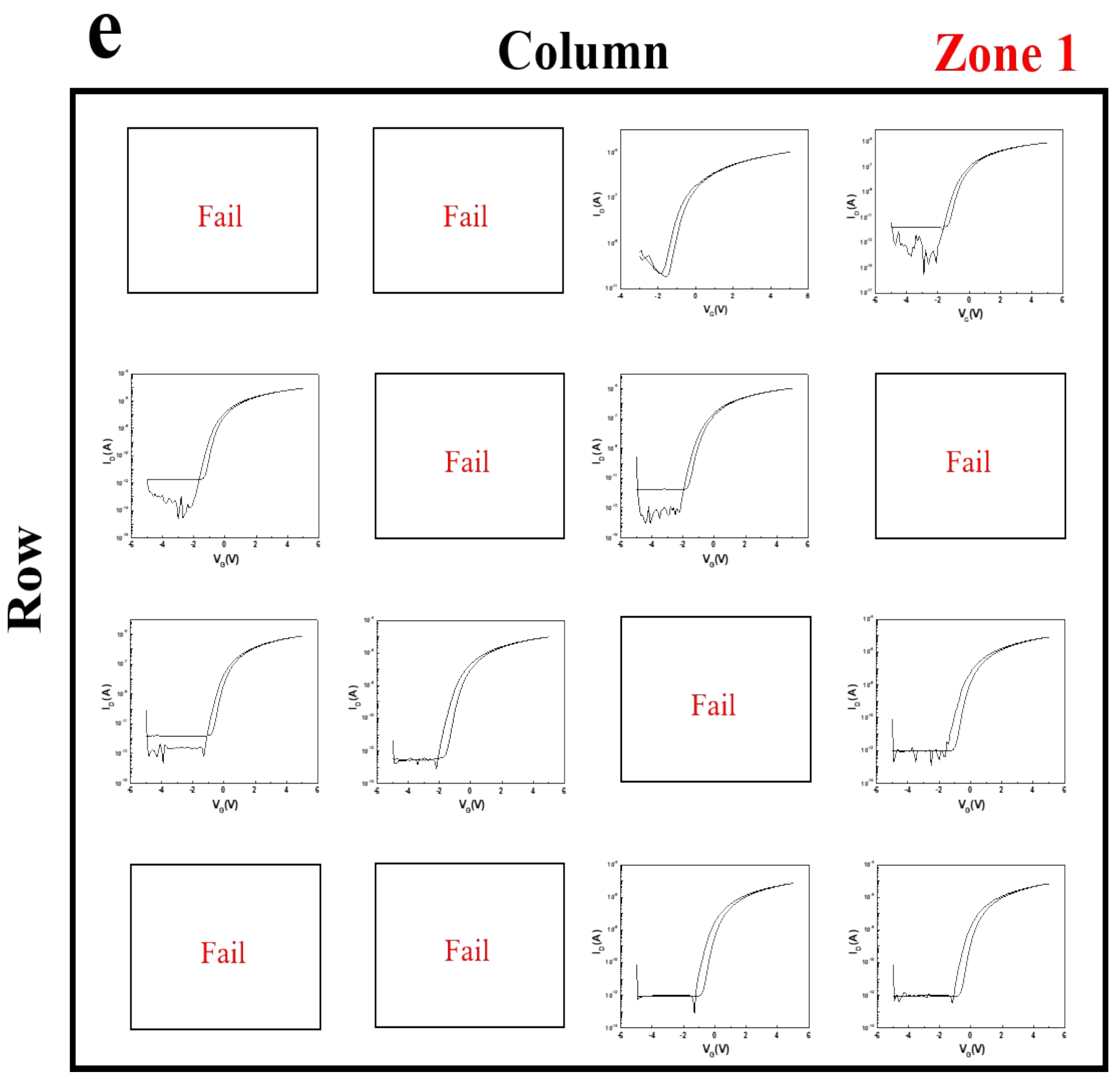


**Fig. S8e** Transfer characteristics of each control-gate transistor located in zone 1.

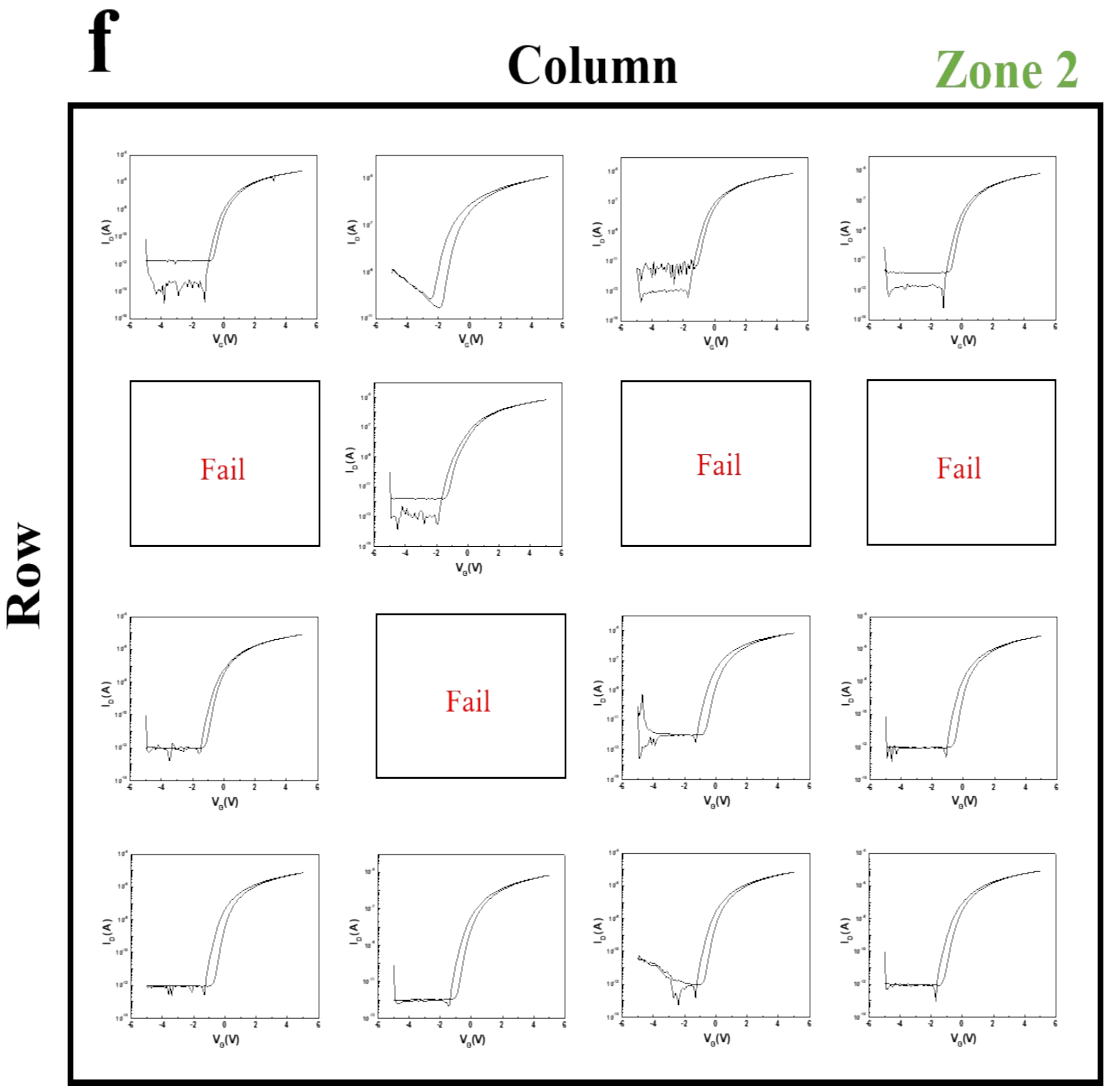


**Fig. S8f** Transfer characteristics of each control-gate transistor located in zone 2.

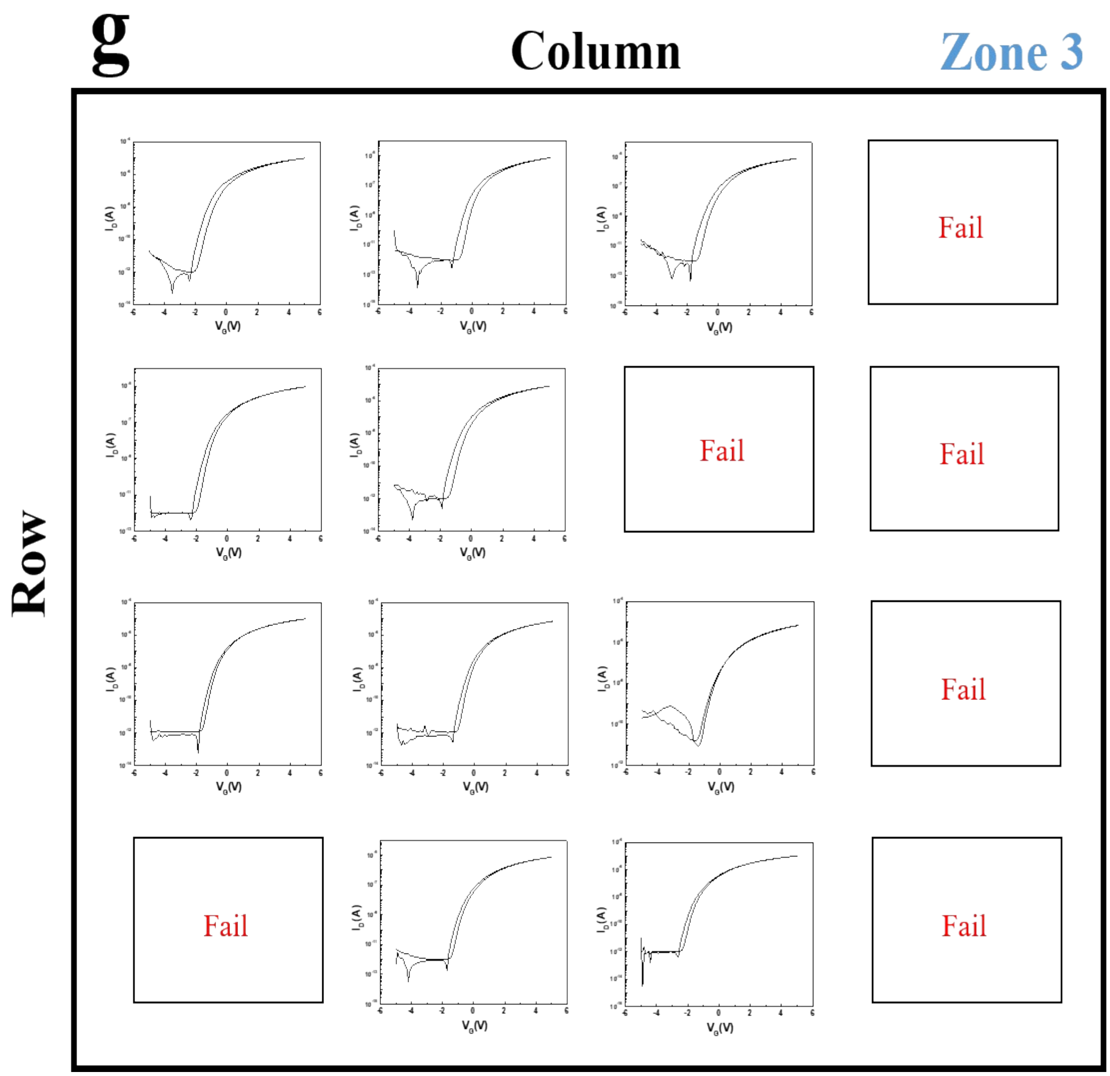


**Fig. S8g** Transfer characteristics of each control-gate transistor located in zone 3.

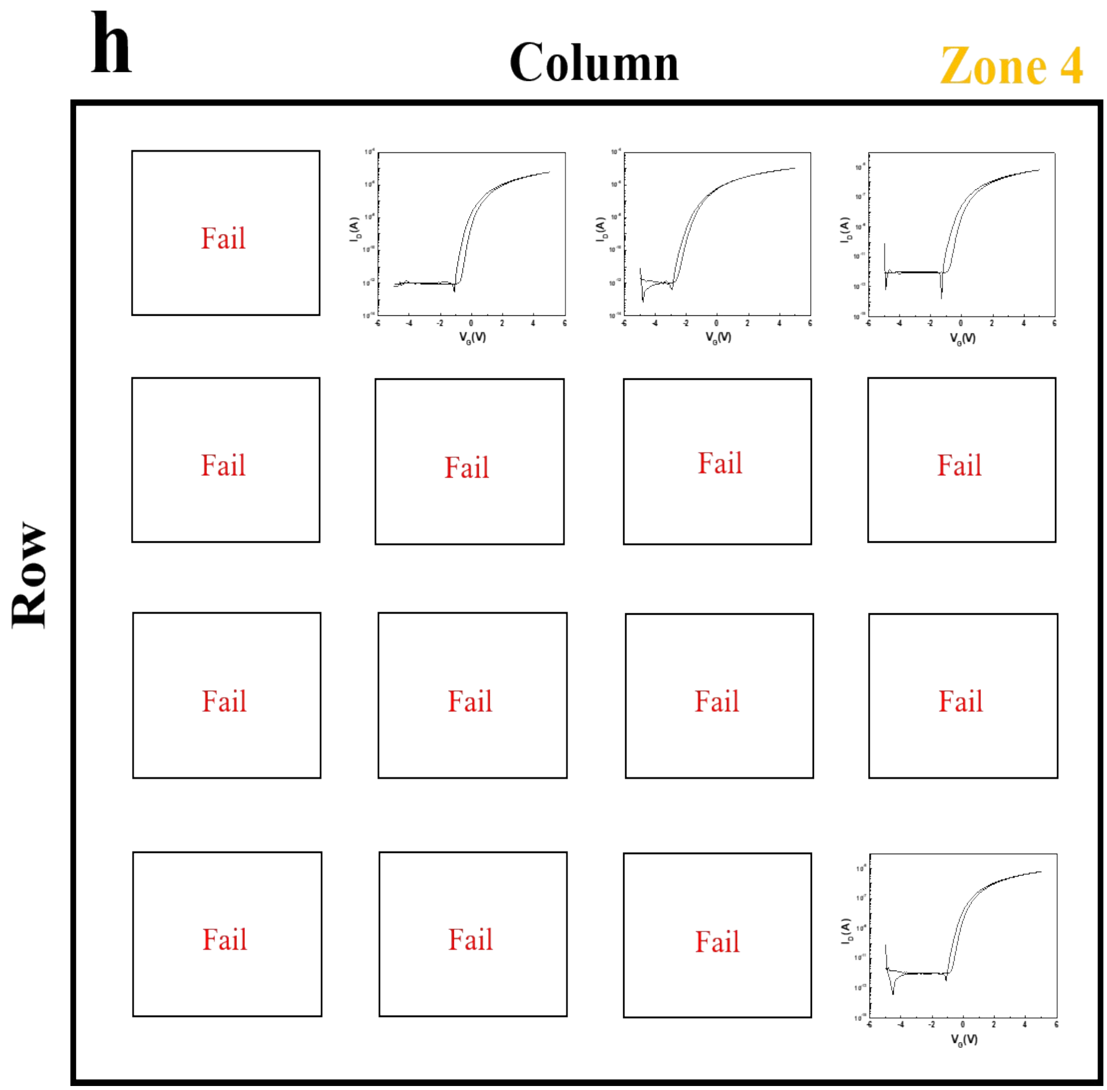


**Fig. S8h** Transfer characteristics of each control-gate transistor located in zone 4.

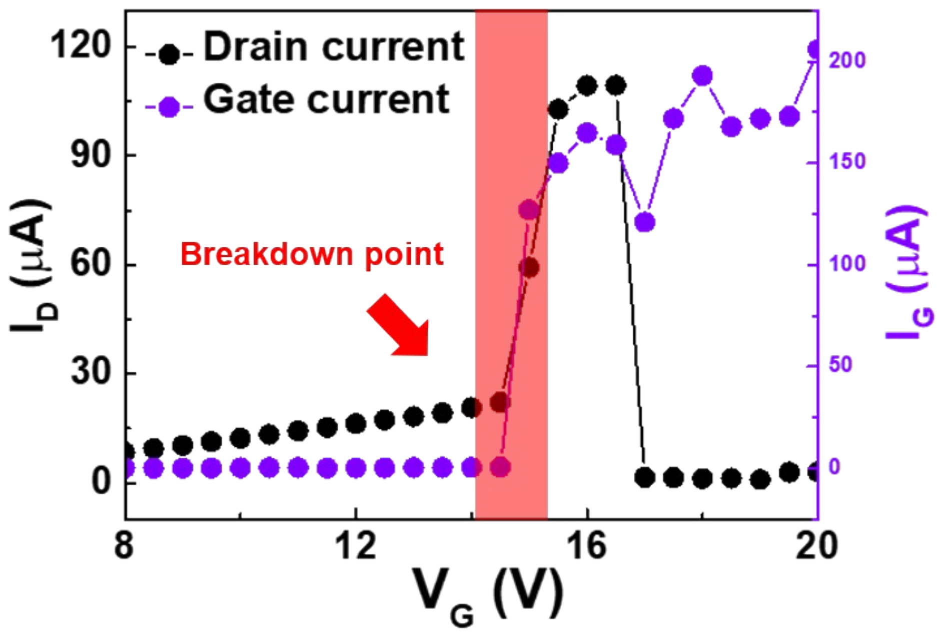


**Fig. S9** The test of defining device breakdown phenomena causing large gate leakage current

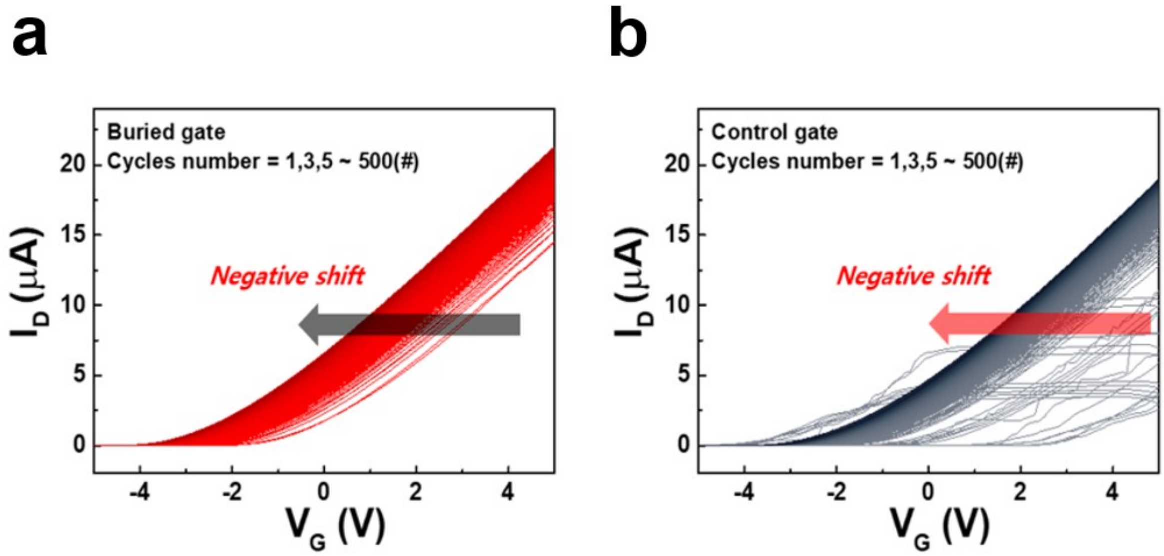


**Fig. S10** Negative shift of threshold voltage in $V_G$-$I_D$ sweeping endurance cycling test for (a) buried and (b) control gate transistors

## Series resistance calculation

The series resistance in Figure 4f was calculated using the conventional drain current equation (1) proposed as an extraction technique [1].

$$I_D = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} (V_G - V_{th} - \frac{I_D R_{SD}}{2})(V_D - I_D R_{SD}) \qquad (1)$$

where $\mu_{eff}$ is the effective mobility, $C_{ox}$ is the gate oxide capacitance, $W_{eff}$ /$L_{eff}$ is the effective channel width/length, $V_{th}$ is the threshold voltage, and $R_{SD}$ is the series resistance. The series resistance is extracted by utilizing the ratio of two linear transfer curves.

$$\frac{I_{D1}}{I_{D2}} = \frac{\mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} (V_G - V_{th1} - \frac{I_D R_{SD}}{2})(\mathrm{V}_{D1} - I_{D1} R_{SD})}{\mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} (V_G - V_{th2} - \frac{I_D R_{SD}}{2})(\mathrm{V}_{D2} - I_{D2} R_{SD})} \qquad (2)$$

By manipulating the equation (2) above, a quadratic equation was extracted and subsequently solved.

$$R_{SD}^2 (\frac{I_{D2} - I_{D1}}{2}) + \mathrm{R}_{SD} (V_{th2} - V_{th1} \frac{V_{D1} - V_{D2}}{2}) - \frac{(V_G - V_{th1}) I_{D2} V_{D1} - (V_G - V_{th2}) \mathrm{I}_{D1} \mathrm{V}_{D2}}{2} = 0$$

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## Reference

1 J. P. Campbell, K. P. Cheung, J. S. Suehle and A. Oates, *IEEE Electron Device Lett.*, 2011, **32**, 1047–1049.