(Supplementary Information) A universal framework for design and manufacture of deterministic lateral displacement chips

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1 Nanoimprint lithography —Defects

Nanoimprint lithography (NIL) is prone to several different types of defects including non-fill, template, plug, etc. [1]. Since the early stage in the development of NIL, a large amount of efforts have been devoted to diminish these defects and to achieve a high-yield process [2–6]. As a result of these efforts, competitive defectivity levels as low as $\sim$ 1.1 defects cm^{-2} have been achieved [7]. Herein, we provide a brief report on two major types of defects we had to deal with: non-fill defects, and particle-induced defects.

1.1 Non-fill defects

Using an appropriate droplet pattern is crucially important when using J-FIL. In order to achieve a successful, defect-free imprint, the residual layer thickness (RLT) needs to be 1. sufficiently small, and 2. uniform across the wafer. In the case that RLT does not meet these criteria, a relatively long etch process is required to completely remove the imprint resist in areas with high RLT. As a result, the imprint resist can be entirely etched away in regions with thin RLT, which becomes problematic for the areas that should possess intact imprint resist layer to serve as hard mask in the subsequent process steps when etching underlying film, *e.g.*, silicon dioxide.

Achieving a uniform, and thin RLT can become challenging in presence of complex patterns on template. For example, a mere uniform droplet pattern may not correctly fill patterns at interface between two regions wherein one has tight line-space patterns and the other contains sparse holes. An appropriate droplet pattern is typically designed depending on patterns residing on template. There are many factors playing role in the dynamics of spread and merge of droplets, the details of which are beyond the scope of this work. At the very least, however, the droplet pattern needs to take the volume of recessed areas on template into account *locally*. This typically leads to a droplet pattern with variable density across the field.

We applied a combination of modeling and experimental tools to achieve an optimized droplet pattern leading to successful, and almost free of non-fill defects. Some of the microscopy images of defected areas in absence of an optimized droplet patterns are shown in Fig. 1. Unless otherwise stated, the inkjet printhead dispensed 6-picoliter droplets. Some of the microscopy images of similar areas are also shown in Fig. 2 for wafers processed with an optimized droplet pattern.

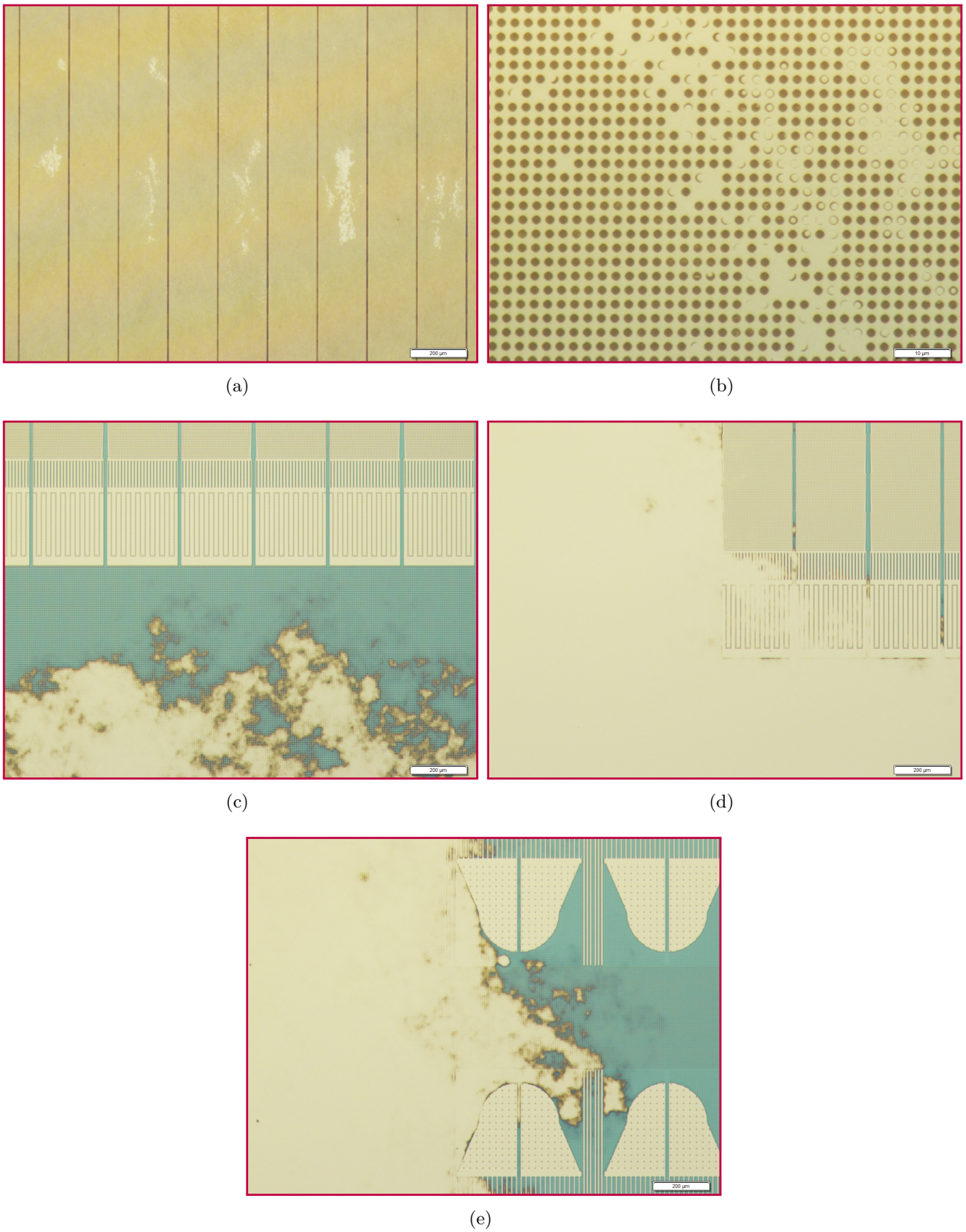


Figure 1: **Microscopy images of some non-fill defects and their effects on following pattern transfer process we encountered during the process of droplet pattern optimization.** (a, b) Non-fill defects resulted from a uniform droplet pattern on a 4×4 grid with a pitch of $\sim 84.5\ \mu m$ with low (a) and high magnification (b). Here, the liquid volume is not sufficient to fill all the holes in the template. (c, d, e) Post-NIL pattern transfer process, wherein underlying silicon dioxide layer is substantially removed due to non-fill defects close to interface between DLD structure and its surrounding decorating area resulted from a uniform droplet pattern on a 3×3 grid with a pitch of $\sim 84.5\ \mu m$.

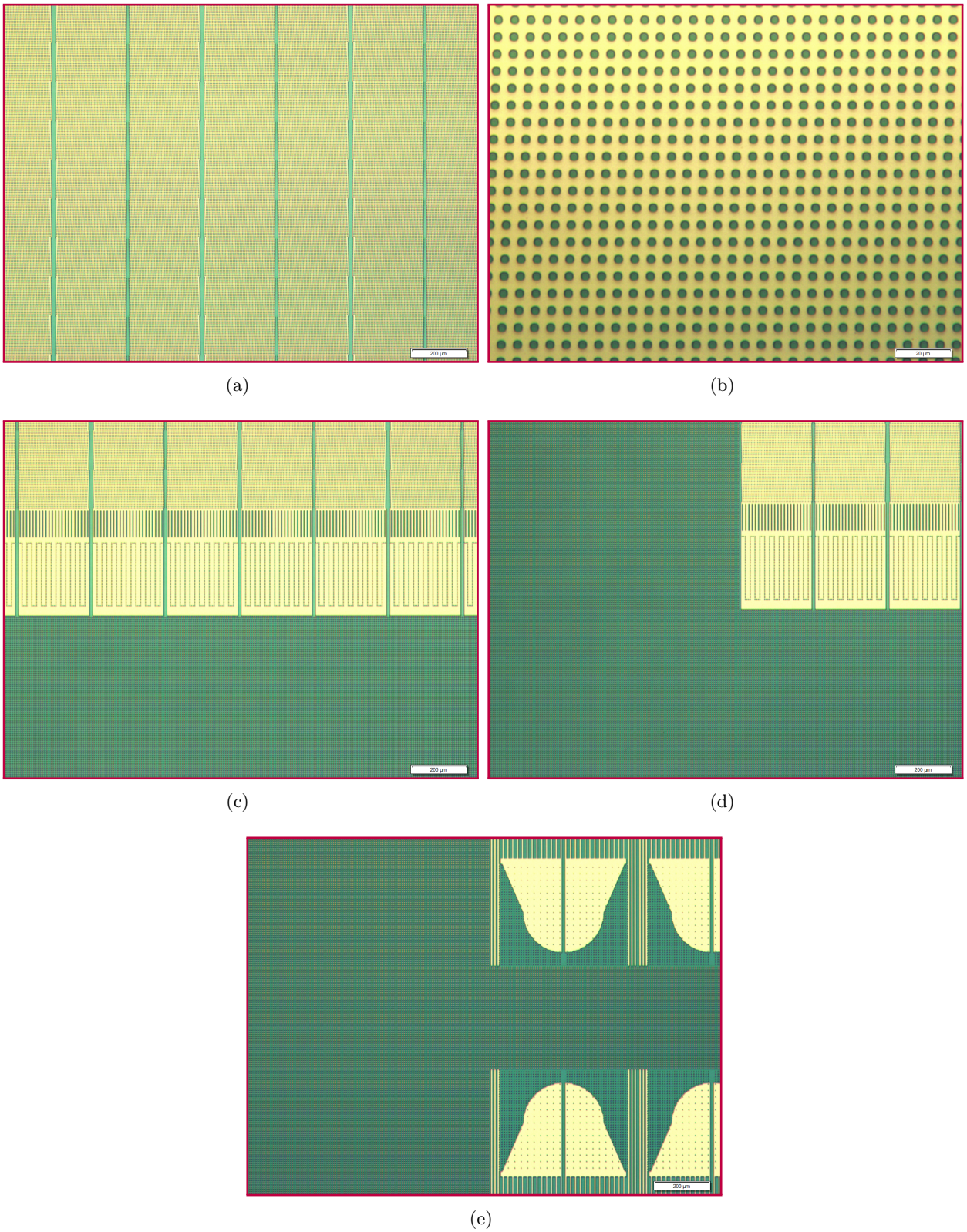
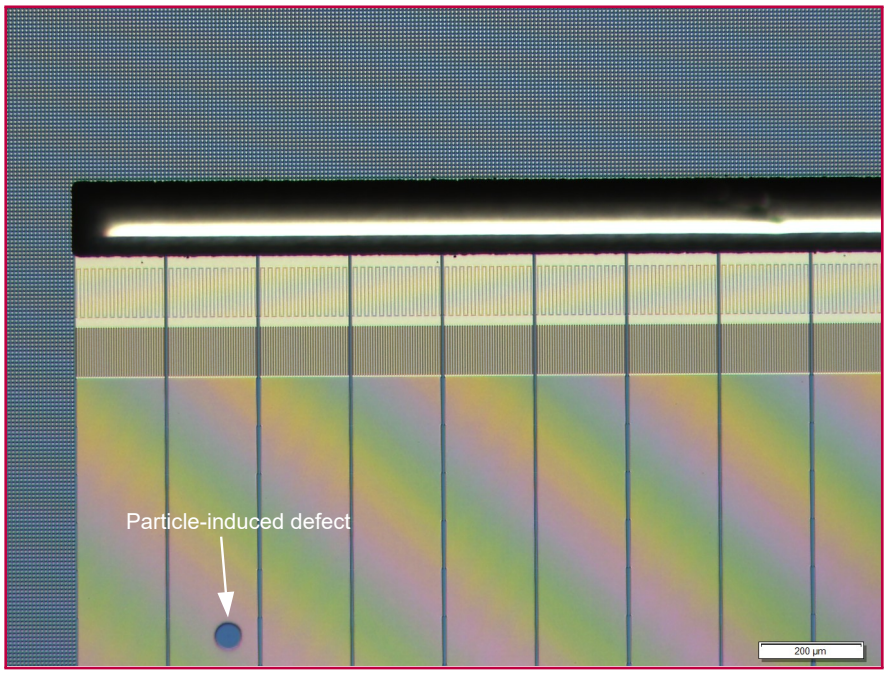


Figure 2: Microscopy images of areas similar to those in Fig. 1 for wafers processed with an optimized droplet pattern.



(a)

Figure 3: Microscopy image of a particle-induced local defect.

1.2 Particle-induced defects

Even by using an appropriate droplet pattern, the imprint process is still prone to defects particularly the particle induced defects. Our fabrication has not been completely defect-free. Some of the local defects are shown in Fig. 3.

2 DLD design automation

Herein, we start with providing more details on the design automation mechanisms for DLD structures of different themes following by that of optional up-/down-stream components.

2.1 DLD core & condenser design theme

Algorithm 1 provides a pseudo-code for determining the geometrical configurations defining the core of DLD automatically. There are some geometrical constraints implemented in the package to take into account some of the common constraints and considerations. For example, N_p and N_w are confined to the ranges of [8, 50] and [8, 100,000], respectively, while channel width and length are confined to [50 μm, 10 mm] and [0.5 mm, 40 mm], respectively. The specified ranges have been tried to be reasonably wide to cover most applications spanning from parallelized nano-DLD systems, wherein footprint of each **full** DLD block (condenser design theme) is small, to traditional DLD systems with relatively large footprints. Regardless, these constraints can be explicitly provided by user as needed. The constraints can also be turned off completely by passing `turn_off_constraints=True`.

The periodicity N_p and number of fluidic lanes N_w are among the most important design parameters to be determined. In the following, we try to describe these parameters and how they impact the performance metrics of final device.

Algorithm 1: The algorithm to automatically determine a set of geometrical configurations for a DLD block subject to a set of constraints.

Input: A valid set of one or a plurality of the following parameters:

d_c	Critical diameter
N_p	Periodicity
N_w	Count of fluidic lanes
w	Width of inlet channel
g_w	Gap between adjacent pillars along channel width
g_a	Gap between adjacent pillars along channel axis
λ_w	Pitch of pillars array along channel width
λ_a	Pitch of pillars array along channel axis
h	Pillars height
μ	Fluid viscosity
Γ	Extending the channel length l by this factor to be safe, by default 0.1
Geometrical constraints:	
Range of N_p	by default $[8, 50]$
Range of N_w	by default $[8, 100,000]$
Range of w	by default $[50\ \mu m, 10\ mm]$
Range of l	by default $[0.5\ mm, 40\ mm]$
Performance constraints:	
$[g_w/d_c]_{\min}$	Min allowed gap over critical diameter ratio, by default None
$Q_{\min}$	Min allowed volumetric flow rate, by default None
$A_{\max}$	Max allowed die area, by default None

for $N_p^* \leftarrow N_p^{max}$ **to** N_p^{min} **do**
  $g_w^* \leftarrow$ // Set from provided g_w if applicable; otherwise, calculate from provided d_c together with N_p^*
  $\lambda_w^* \leftarrow$ // Set from provided λ_w if applicable; otherwise, $2g_w^*$
  g_a^* & $\lambda_a^* \leftarrow$ // Set from provided g_a & λ_a if applicable; otherwise, infer from g_w^* & λ_w^*
  $h^* \leftarrow$ // Set from provided h if applicable; otherwise, consider a high depth-to-gap channel: $h^* = 4g_w^*$
  Constraint: check $[g_w/d_c]_{\min}$ if applicable
  if *Fail* **then**
    Go to next N_p^*
  end
  for $N_w^* \leftarrow N_w^{min}$ **to** N_w^{max} **do**
    $w^* \leftarrow N_w^* \lambda_w^*$ // Calculate width of unit
    $l^* \leftarrow \text{ceil}(N_w[1+\Gamma])N_p\lambda_a$ // Calculate length of channels
    Geometrical Constraints:
    if $w > w^{max}$ *or* $l > l^{max}$ **then**
      Go to next N_p^* // A larger N_w is not an option as channel is already too wide/long
    end
    Performance Constraints: check $Q_{\min}$, $A_{\max}$, and any other applicable criteria
    if *Fail* **then**
      Go to next N_w^*
    else
      Return the determined configurations // Parameters with asterisk superscript to be returned
    end
  end
end
Exit without finding an appropriate set of configurations

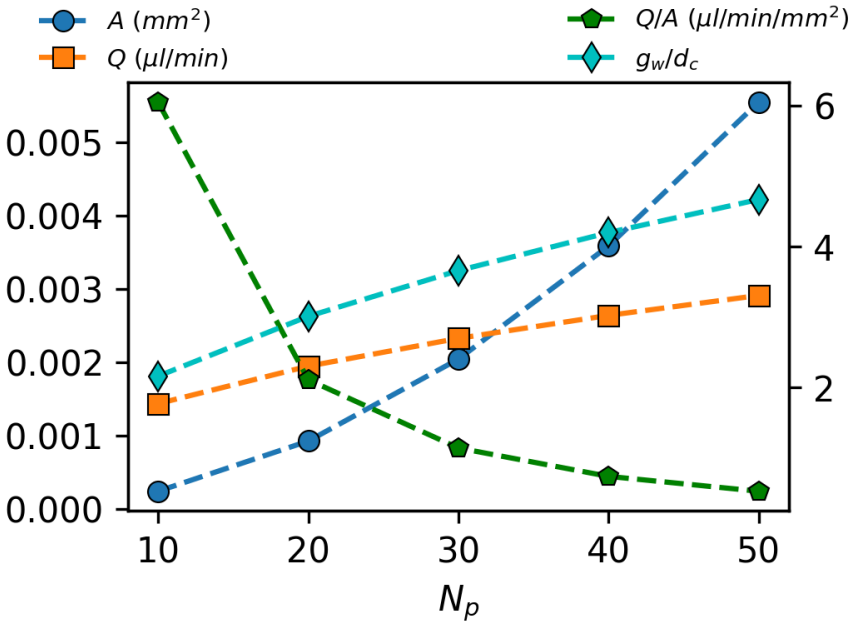


Figure 4: Performance metrics for multiple designs with similar number of fluidic lanes ($N_w = 10$) and different periodicity levels (N_p) to isolate 100-nm particles from an aqueous solution, *i.e.*, $d_c = 0.1\ \mu m$. The pillars height is assumed to be 4 times as large as its diameter.

2.1.1 Periodicity

A higher periodicity is typically preferred as it mitigates the clogging risk. As counterintuitive as it may seem, a higher periodicity can also potentially enhance the volumetric flow rate despite increasing the channel length. There are a couple of reasons as explained in the following:

- For a given critical diameter, a higher periodicity allows for a larger gap between pillars. A slight increase in the gap between pillars can potentially result in such a dramatic reduction of channels resistance, *e.g.*, with a power of ~ 3 for structures with high depth-to-gap ratios, that it can compensate for the linear resistance increase associated with a higher channel length.
- In practice, microchannels can be etched deeper safely as the posts diameter increases, which can contribute in enhancing the throughput of device.

The disadvantage, however, is that a higher periodicity increases the die area and potentially the final cost of device.

As an example, let us consider the separation of nano-particles of 100 nm in diameter from an aqueous solution. Here, we aim at comparing several DLD designs (non-mirrored, non-arrayed). Some of the performance metrics are compared in Fig. 4 for multiple configurations with different periodicity levels. The number of fluidic lanes is kept fixed for all designs: $N_w = 10$. It can be perceived that a higher periodicity leads to higher values of throughput (Q) and g_w/d_c, while the die area (A) increases nonlinearly. The compound metric of flow rate over die area (Q/A) can be considered as an efficiency indicator, wherein a higher score shows that a larger throughput can be achieved for a unit of die area. In general, all these metrics can be informative, but how much weight each should receive can be different from one application to another. Therefore, we have not specified any default threshold for these performance constraints. However, user can provide the requirements by passing valid arguments, *e.g.*, **max_die_area_mmsq=1.0**, **min_vfr_ml_per_hr_per_bar=2.0**, **min_gap_over_dc=4.0**, etc. The developed package reports the mentioned metrics to provide user with some insight on how efficient and/or effective the design really is.

It should be noted that the current implementation of constraints is ***relatively*** slow; it may take up to a few

seconds depending on system configurations. The underlying reason is that it attempts to scan the whole parameter space sequentially. More efficient algorithms, *e.g.*, bisection, etc., can be applied in the future to improve the performance.

2.1.2 Count of fluidic lanes/columns

While the design tool can automate the process of determining parameters like N_w, it is helpful if user is aware of some of the considerations taken into account when determining the count of fluidic lanes N_w. For example:

- For sufficiently deep channels, changing N_w does not cause noticeable effects on throughput as both width and length of channels vary with almost the same proportion. Regardless, the die footprint increases with N_w.
- N_w needs to be reasonably high to enable meaningful separation of particles with acceptable resolution and enhancement ratio. For example, a DLD structure with only 3 fluidic lanes (including depletion and accumulation lanes) is probably not a suitable design for many applications.
- For highly parallelized DLD structures with small pillars in general, and nano-DLD systems in particular, N_w needs to be sufficiently high to render channels a reasonably large footprint, compatible with the size of through wafer vias. For example, considering 20 fluidic lanes ($N_w = 20$) for a nano-DLD design consisting of 200-nm diameter pillars with a pitch of 400 nm, results in a channel width of $\sim 8\ \mu m$. In the case of mirrored design, this value would increase to $\sim 16\ \mu m$. The diameter of through wafer vias, therefore, should be smaller than $\sim 16\ \mu m$, which would probably necessitate thinning a substrate wafer at some point during the fabrication process flow. In the contrast, considering $Nw = 250$ would lead to 200 μm-wide mirrored channels, which makes it relatively easier to form through wafer vias without wafer thinning.

2.2 Multistage design theme

Detatiled information about this theme can be found from Davis *et. al.* [8]. There are a few automation mechanisms implemented for this design theme:

- Inferring number of stages from the arguments provided by user.
- Inferring effective inlet width of stages so that all stages have an almost identical inlet width.
- Inferring sidewall width of stages which aims at making adjustments for the outermost edge of sidewalls to line up well.
- Block-level automation inherited from DLD block (condenser theme) which aims at configuring each stage so that it can be potentially a full DLD block, completely displacing sufficiently large particles towards its accumulation sidewall.
- Any potential up-/down-stream components are automatically assigned to the upstreammost/downstreammost stage.

An example of three-stage design with critical diameters of 18 μm, 10 μm and 5 μm can be found in 3.2. It is worth mentioning that user can override the aforementioned automation mechanism by providing desired arguments, including pillar profile, gap, pitch, boundary treatment, etc.

2.3 Condenser-and-sorter design theme

Detatiled information about this theme can be found from Kim *et. al.* [9]. The automation of configurations is mainly inherited from that implemented in multistage theme. There are some differences in the implementations though. For example, herein, the stages related to sorters are automatically mirrored. Some sideway collections are also created automatically to enable collection of sufficiently large particles at the end of each sorter stage.

An example of three-stage design consisting of a condenser with critical diameters of 18 μm appended by two sorters with critical diameters of 10 μm and 5 μm can be found in 3.3. Again, user can override the aforementioned automation mechanism by providing desired arguments, including pillar profile, gap, pitch, boundary treatment, sideway collections presence and its configurations, etc.

2.4 Up-/down-stream components

There are several upstream components, *e.g.*, filer, preload, and single/multi-inlet, as well as downstream components, *e.g.*, sideway collections, single/multi-outlet that are automatically configured to consistently attach to their neighboring units as needed. These components are configured automatically to attach to a DLD block, *i.e.*, one of the lowest-level building blocks for different themes. As a result, the aforementioned components can be configured automatically to attach DLD systems of different themes.

To accomplish the design automation for these components, we resort to numerous design rules that are mainly in dimensionless form, or coexist with their dimensional counterparts. For example, when designing a filter for a DLD block, we try to set the effective opening width of component equal to that of the target DLD block, while considering a set of default values for different geometrical configurations such as length, period of serpentine, pitch of 1D array of entities in each segment, etc. In order to convert values from dimensional to dimensionless form and vice versa, we use reference lengths, typically the lateral and axial pitch values associated with the target DLD block. This approach enables designing these auxiliary components automatically and attach them to DLD systems consistently regardless of the footprint of device being small, *e.g.* nano-DLD systems, or large.

A caveat, however, is that there is currently only one set of such rules implemented for these components. As a result, for example, a default value for filter length, say, 50 (nondimensionalized by λ_a), gives a filter of 20 μm long when designed for a DLD block with axial pitch of entities equal to 400 nm. This may be reasonable for a nano-DLD device. However, the same rule would give a filter of 5 mm long when designed for a DLD block with axial pitch of entities equal to 100 μm. Depending on the application needs, *e.g.*, how long the device will be running, how many particles and of what sizes are expected to be trapped upstream of device, etc., the designer may consider this filter long, short, or appropriate. Therefore, our design tool should not be considered as a complete replacement of human designer. Yet, it enables user to explicitly fine tune various aspects of the design as needed. Adjusting the filter length in Listing 7 can be considered as an example of human intervention.

3 Examples

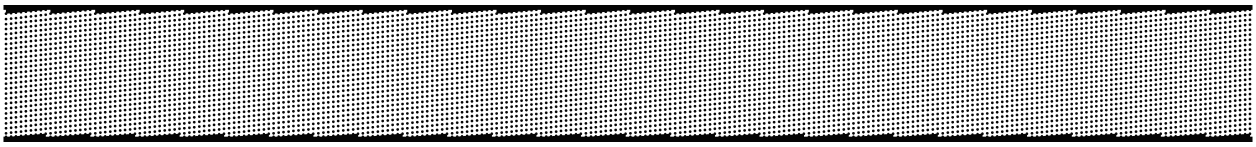
Some of the features of the developed DLD design automation (DDA) tool are illustrated in the following. For the purpose of better arrangement of contents in this document, we pass `rotation_angle_deg_before_array=90` or `rot_last=90` in most cases to generate a horizontal layout.

3.1 Condenser design theme & optional up-/down-stream components

For running these examples, the Block theme needs to be loaded as:

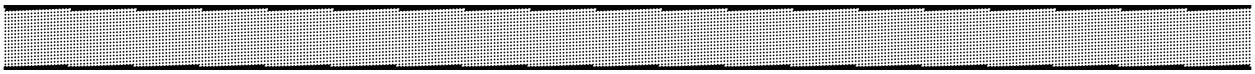
from mnflow.mfda.cad.dld.theme.block import DLD

In addition, we pass turn_off_constraints=True unless otherwise stated.



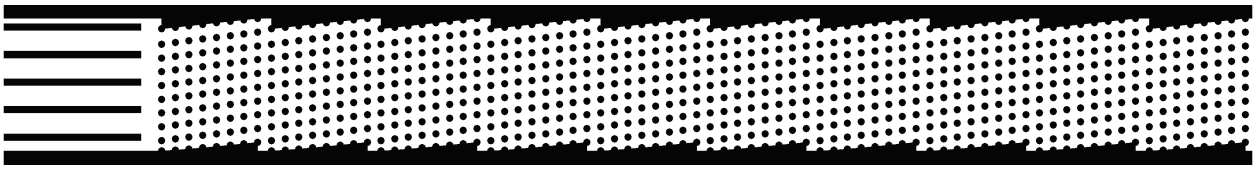
```
DLD(
  d_c=0.5,
  max_die_area_mmsq=0.03,
  rotation_angle_deg_before_array=90
)
```

Listing 1: Benchmark: (High-resolution online) Applying constraints – Max die area: 0.03 mm^2.The configurations are determined to be $N_p = 9$, $Nw = 25$, $g_w = 1.025$, $\lambda_w =: 2.051$, $g_a = 1.025$, and $\lambda_a = 2.051$.



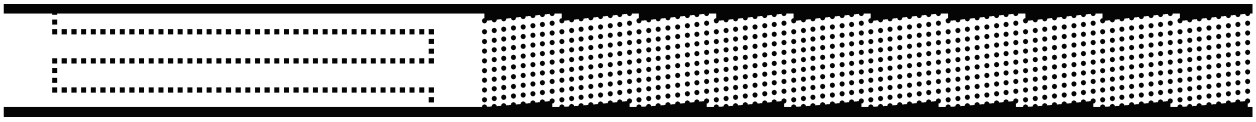
```
DLD(
  d_c=0.5,
  max_die_area_mmsq=0.06,
  rotation_angle_deg_before_array=90
)
```

Listing 2: Benchmark: (High-resolution online) Applying constraints – Max die area: 0.06 mm^2. The configurations are determined to be $N_p = 20$, $Nw = 17$, $g_w = 1.504$, $\lambda_w =: 3.009$, $g_a = 1.504$, and $\lambda_a = 3.009$.



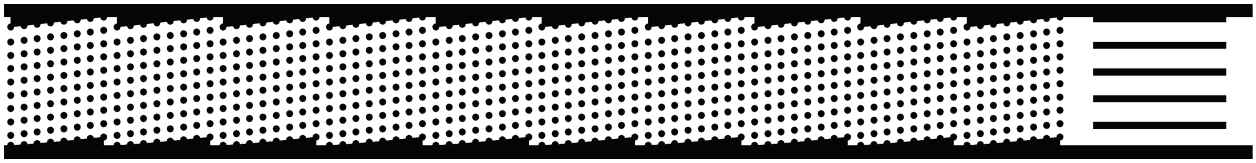
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  opt_preload=True,
  rotation_angle_deg_before_array=90
)
```

Listing 3: Benchmark: Adding a preload upstream of device.



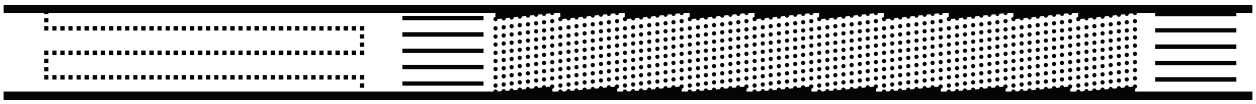
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  opt_filter=True,
  rotation_angle_deg_before_array=90
)
```

Listing 4: Benchmark: Adding a filter upstream of device.



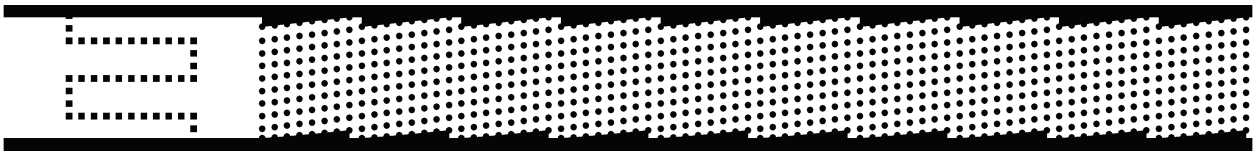
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  opt_collection=True,
  rotation_angle_deg_before_array=90
)
```

Listing 5: Benchmark: Adding collection channels downstream of device.



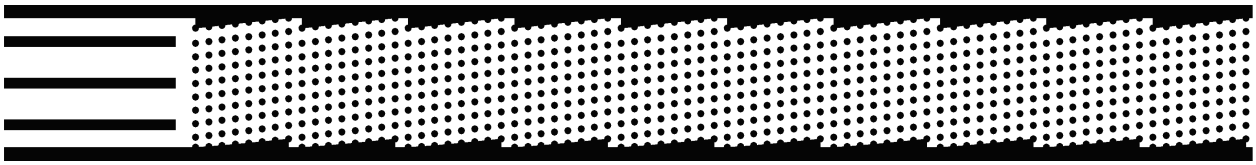
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  opt_filter=True,
  opt_preload=True,
  opt_collection=True,
  rotation_angle_deg_before_array=90
)
```

Listing 6: Benchmark: Adding preload and filter upstream and collection channels downstream of device.



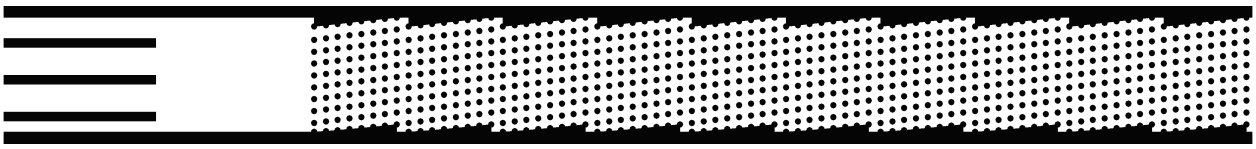
```
DLD(
  Np=8,
  d_c=1.,
  opt_filter=True,
  Nw=9,
  filter_len_nondim=10,
  rotation_angle_deg_before_array=90
)
```

Listing 7: Benchmark: Adjusting the length of filter upstream of device.



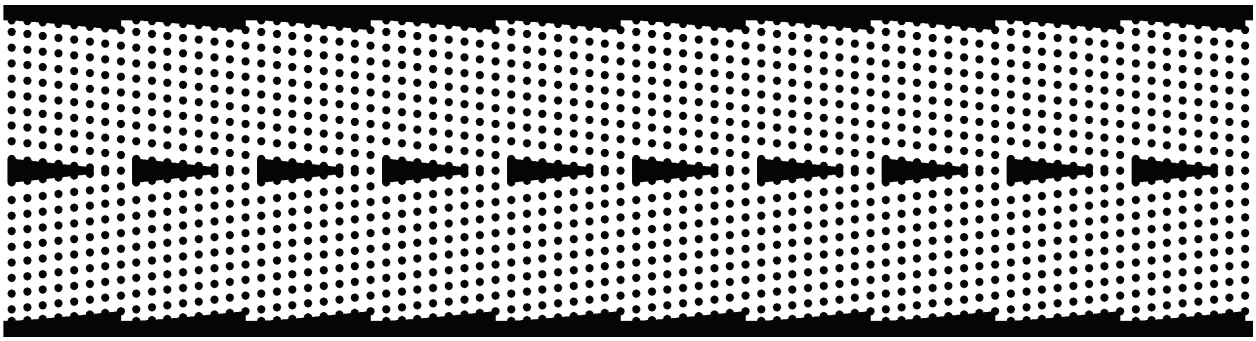
```
DLD(
  Np=8,
  d_c=1.,
  opt_preload=True,
  Nw=9,
  preload_bar_dims=[3, 50],
  preload_bar_pitch= 12,
  rotation_angle_deg_before_array=90
)
```

Listing 8: Benchmark: Adjusting the preload dimensions.



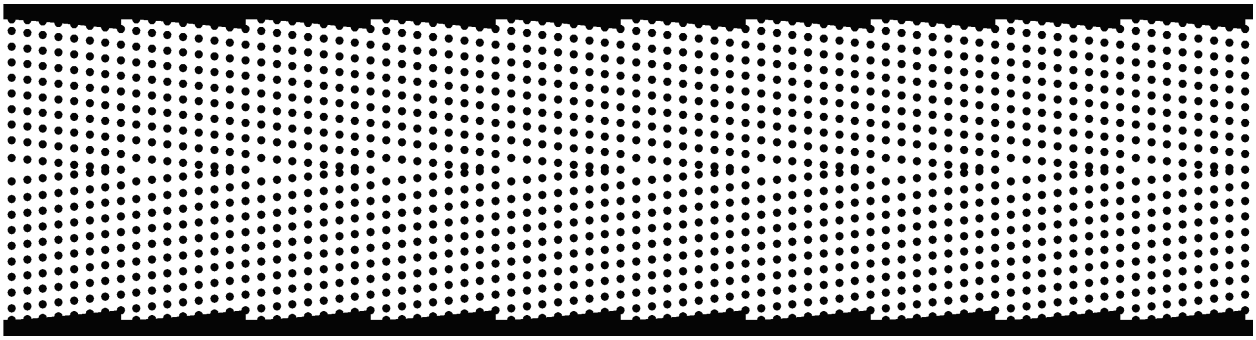
```
DLD(
  Np=8,
  d_c=1.,
  opt_preload=True,
  Nw=9,
  preload_bar_dims=[3, 50],
  preload_bar_pitch=12,
  preload_offset_w=-1.5,
  preload_offset_a=50,
  rotation_angle_deg_before_array=90
)
```

Listing 9: Benchmark: Adjusting the lateral and axial offsets of preload entities.



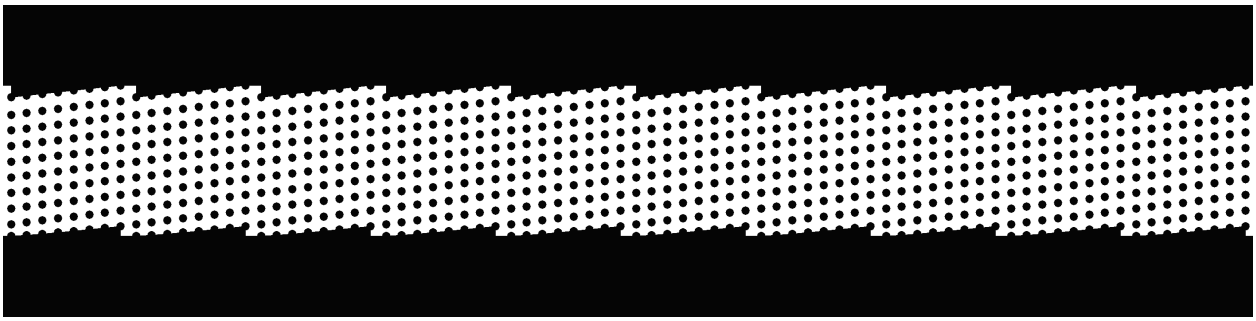
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  opt_mirror=True,
  rotation_angle_deg_before_array=90
)
```

Listing 10: Benchmark: A mirrored design.



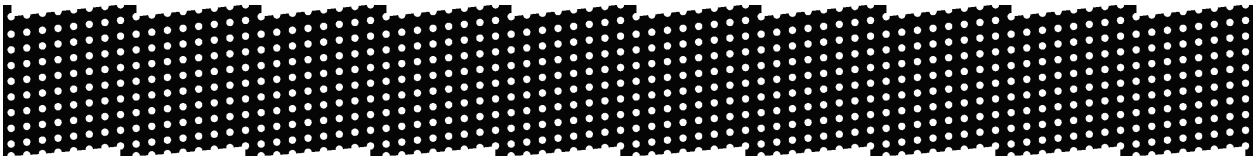
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  opt_mirror=True,
  opt_cover_acc=False,
  rotation_angle_deg_before_array=90
)
```

Listing 11: Benchmark: A mirrored design without cap.



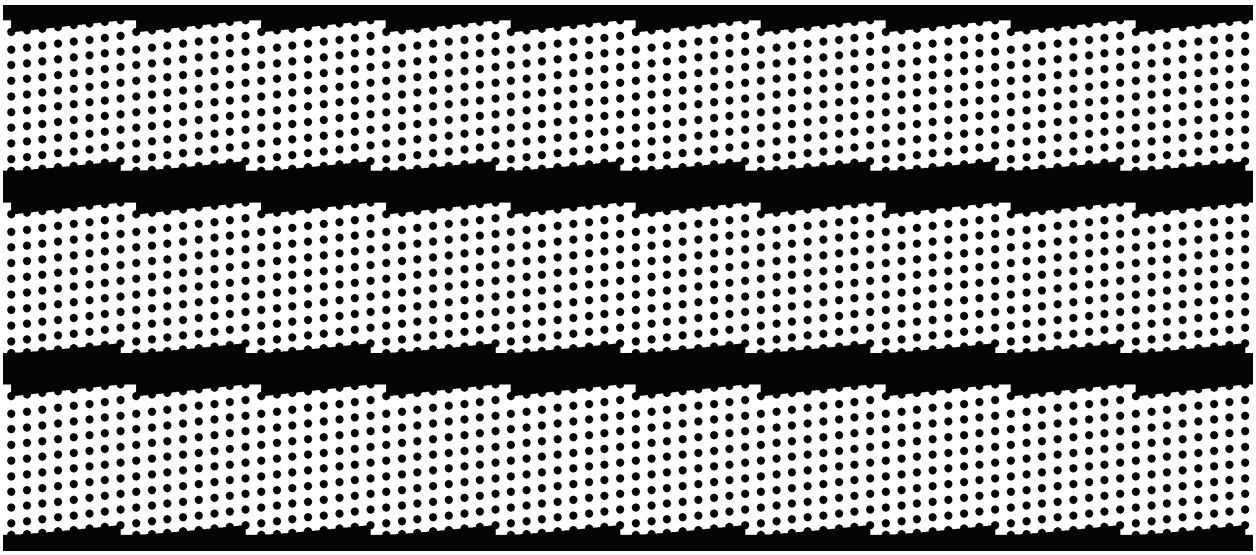
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  sidewall_width=20,
  rotation_angle_deg_before_array=90
)
```

Listing 12: Benchmark: Adjusting the sidewall width.



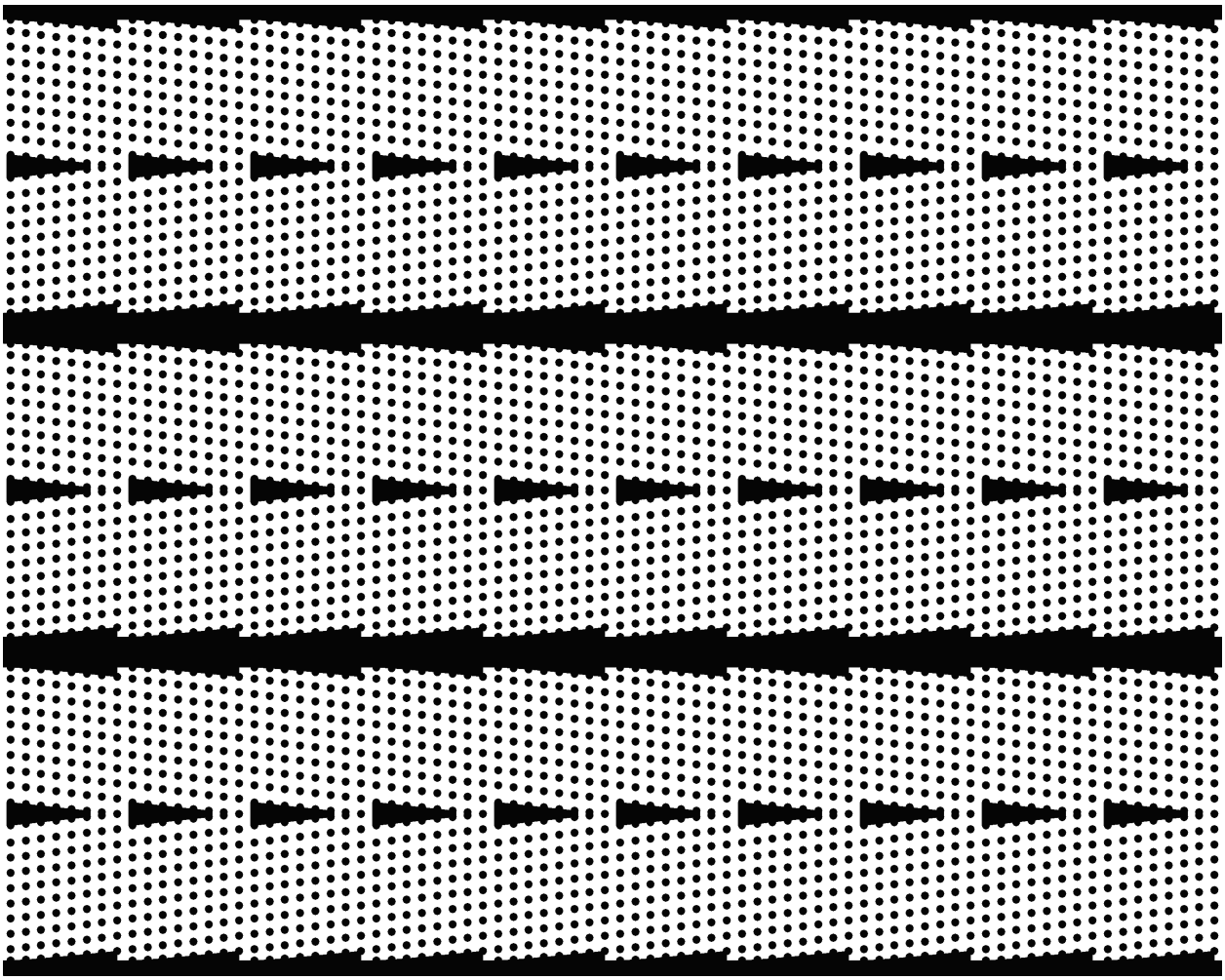
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  opt_reverse_tone=True,
  rotation_angle_deg_before_array=90
)
```

Listing 13: Benchmark: Adjusting the tone of layout.



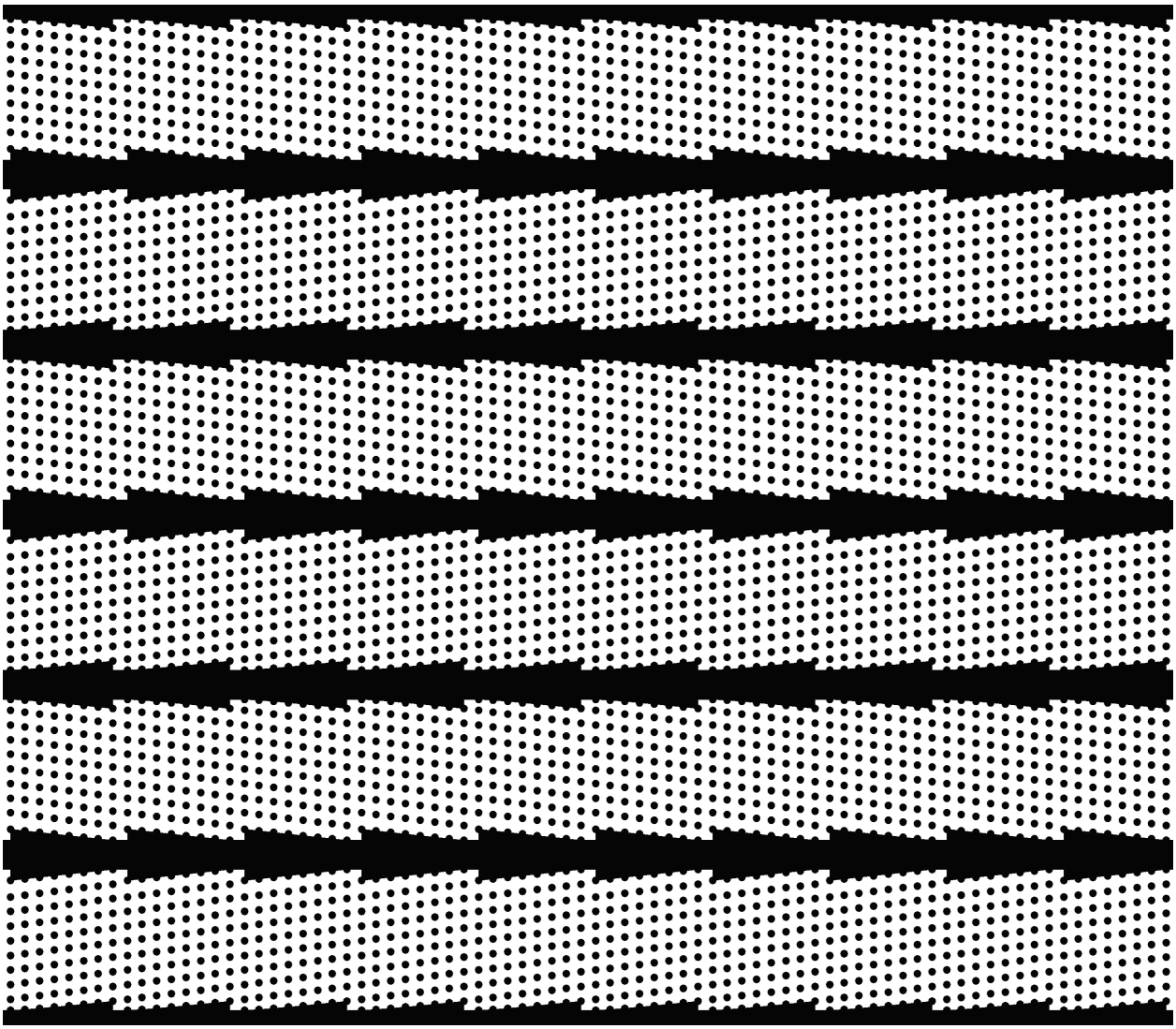
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  array_counts=[1, 3],
  opt_mirror_before_array = [False, False],
  rotation_angle_deg_before_array=90
)
```

Listing 14: Benchmark: Arraying DLD structures.



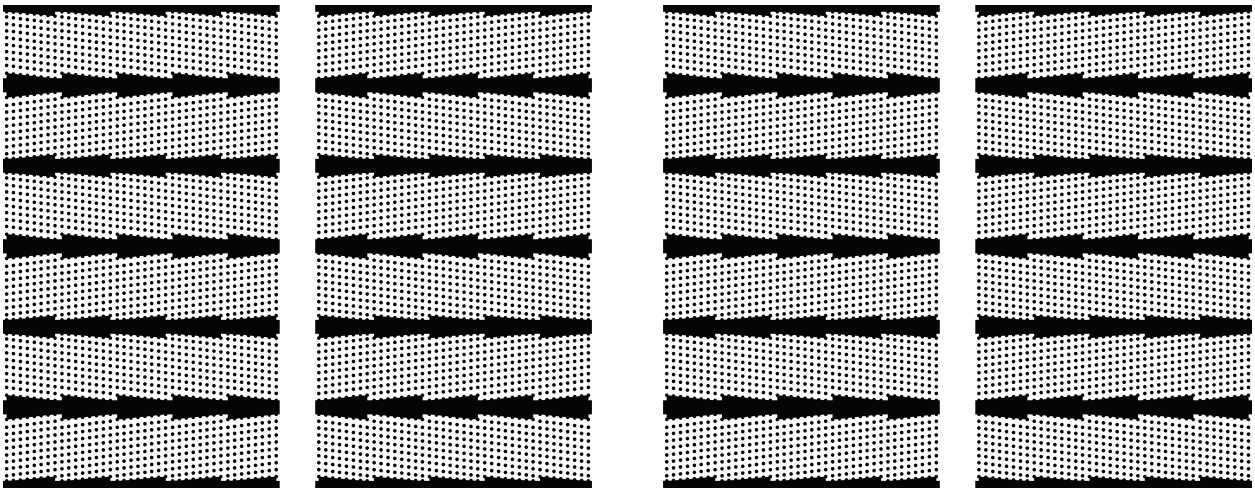
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  opt_mirror=True,
  array_counts=[1, 3],
  opt_mirror_before_array = [False, False],
  rotation_angle_deg_before_array=90
)
```

Listing 15: Benchmark: Arraying DLD structures with mirrored design.



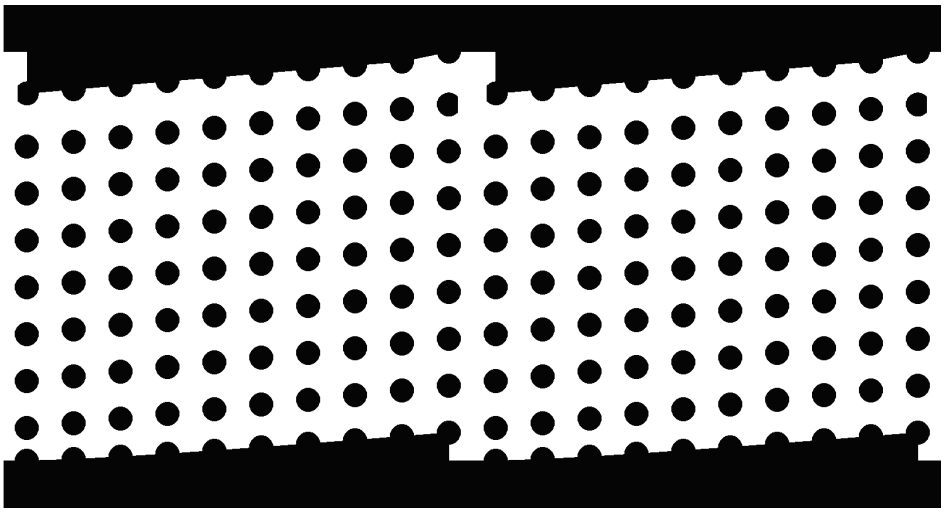
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  array_counts=[1, 3],
  opt_mirror_before_array=[False, True],
  spacing_between_mirrors_before_array=[0,0],
  rotation_angle_deg_before_array=90
)
```

Listing 16: Benchmark: Mirroring following by arraying of DLD structures.



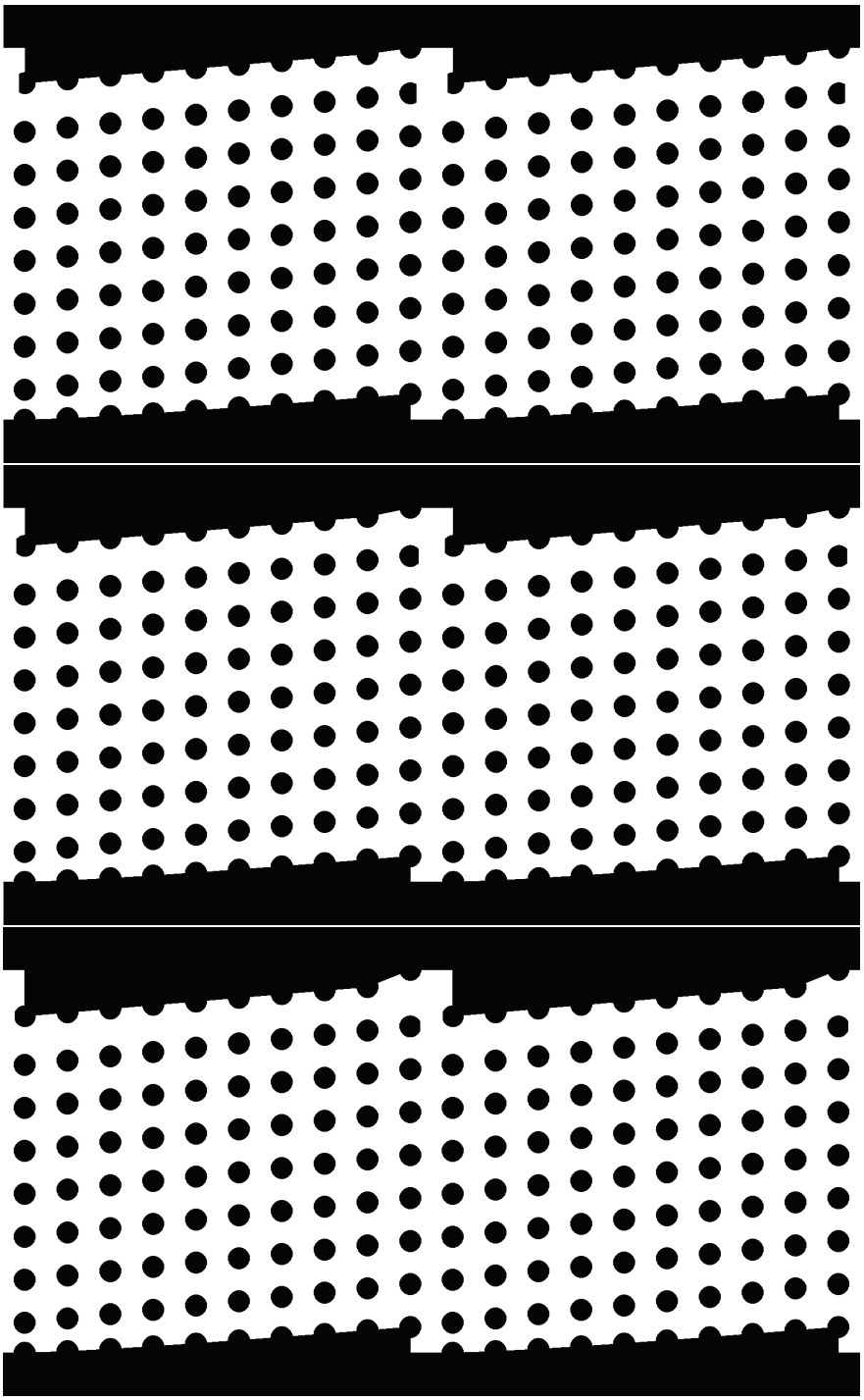
```
DLD(
  Np=8,
  d_c=1.,
  Nw=9,
  num_unit=5,
  array_counts=[2, 3],
  opt_mirror_before_array=[True, True],
  spacing_between_mirrors_before_array=[20, 0],
  array_spacing=[40, 0],
  rotation_angle_deg_before_array=90
)
```

Listing 17: Benchmark: Mirroring following by arraying of DLD structures while adjusting spacing between mirrors and copies.



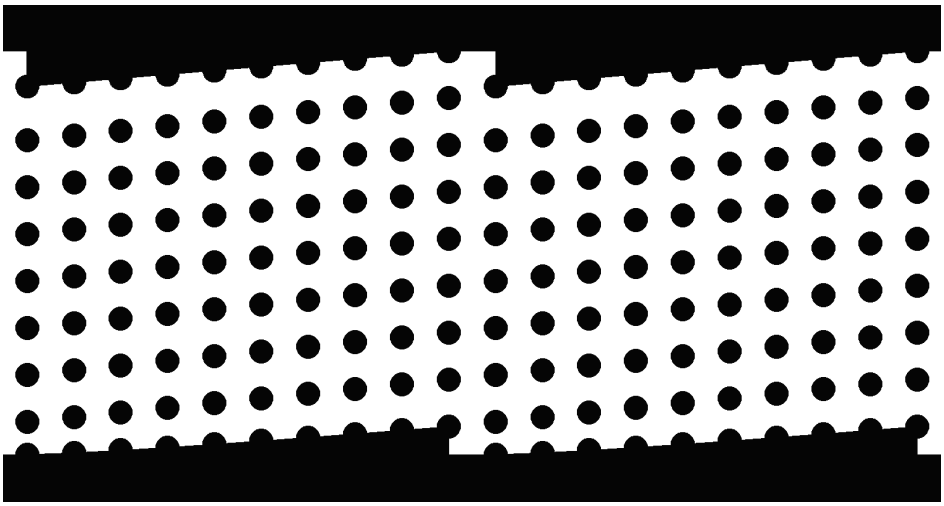
```
DLD(
  Np=10,
  Nw=8,
  gap_w=1.,
  boundary_treatment='3d',
  num_unit=2,
)
```

Listing 18: Benchmark: Boundary treatment '3d' [10].



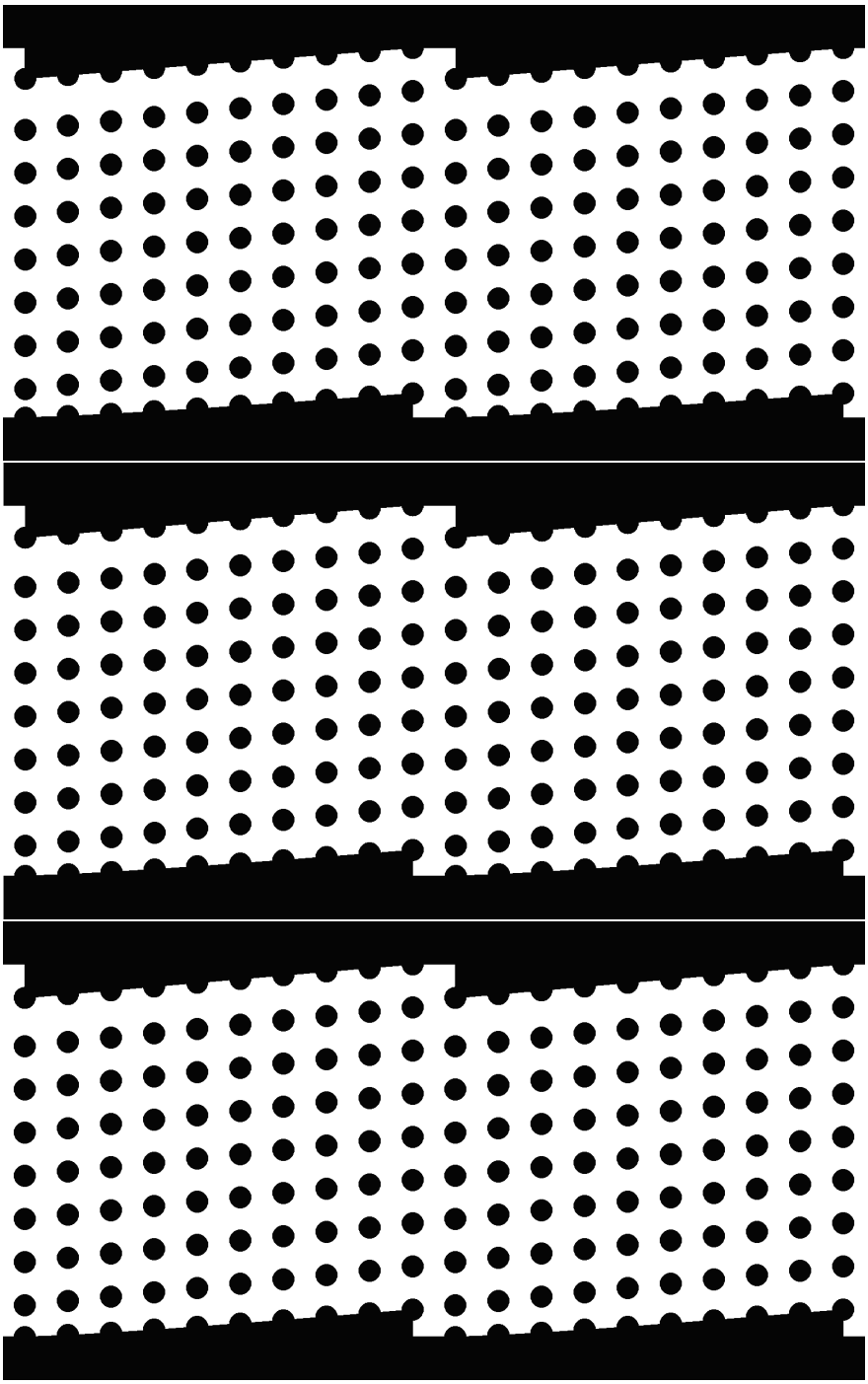
```
DLD(
  Np=10,
  Nw=8,
  gap_w=1.,
  boundary_treatment='3d',
  num_unit=2,
)
```

Listing 19: Benchmark: Boundary treatment '3d' [10]; adjusting resistance ratio: from top to bottom: $\phi = 0.5, 1.0,$ and 3.0. It can be perceived that as ϕ increases, the axial and lateral gaps of unit cell on N^{th} row of accumulation sidewall increases and decreases, respectively, to allow for the ratio of lateral to axial resistance to increase.



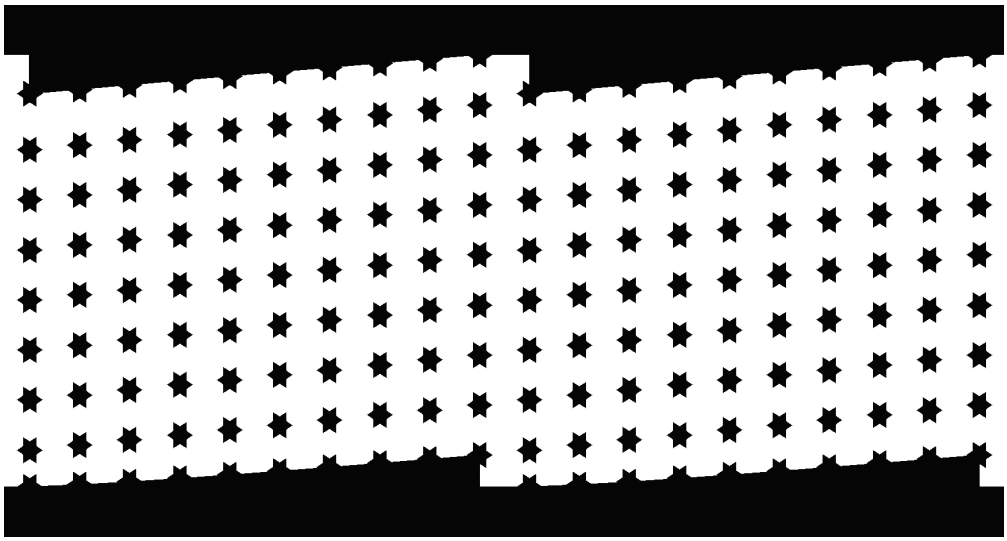
```
DLD(
  Np=10,
  Nw=8,
  gap_w=1.,
  boundary_treatment='pow',
  num_unit=2,
)
```

Listing 20: Benchmark: Boundary treatment 'pow' [11].



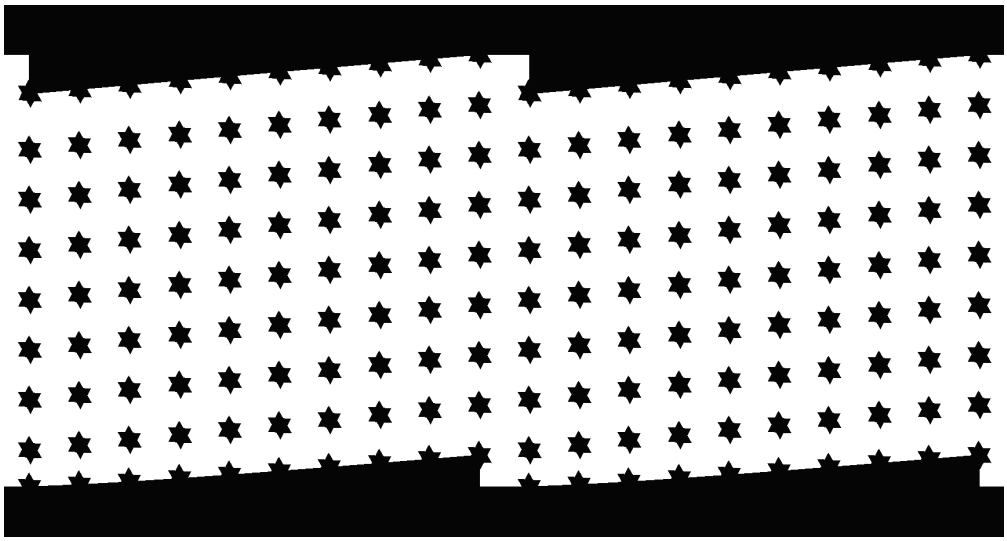
```
DLD(
  Np=10,
  Nw=8,
  gap_w=1.,
  boundary_treatment='3d',
  num_unit=2,
)
```

Listing 21: Benchmark: Boundary treatment 'pow' [11]; adjusting power value: from top to bottom: $b = 2.0, 2.5,$ and 3.0. It can be perceived that as b increases, the maximum gap decreases. The maximum gap is about 38%, 30%, and 24% larger than that in the bulk of domain for $b = 2,$ 2.5 and 3.0, respectively.



```
import numpy as np

shape = np.array([
  (0.34, 0.),
  (0.5, 0.25),
  (0.17, 0.25),
  (0., 0.5),
  (-0.17, 0.25),
  (-0.5, 0.25),
  (-0.34, 0.),
  (-0.5, -0.25),
  (-0.17, -0.25),
  (0., -0.5),
  (0.17, -0.25),
  (0.5, -0.25),
  ])

DLD(
  d_c=1.,
  Np=10,
  Nw=8,
  core_shape=shape,
  num_unit=2,
)
```

Listing 22: Benchmark: User-defined pillars profile.



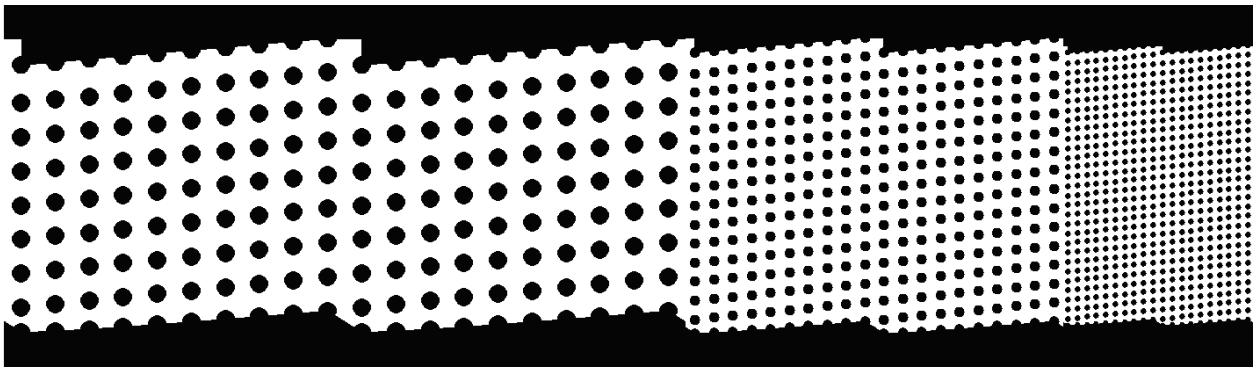
```
import numpy as np

shape = np.array([
  (0.34, 0.),
  (0.5, 0.25),
  (0.17, 0.25),
  (0., 0.5),
  (-0.17, 0.25),
  (-0.5, 0.25),
  (-0.34, 0.),
  (-0.5, -0.25),
  (-0.17, -0.25),
  (0., -0.5),
  (0.17, -0.25),
  (0.5, -0.25),
  ])

DLD(
  d_c=1.,
  Np=10,
  Nw=8,
  core_shape=shape,
  num_unit=2,
  core_shape_rot_angle=30,
)
```

Listing 23: Benchmark: Rotation of pillars.

3.2 Multistage design theme

For running these examples, the multistage theme needs to be loaded as:

```
from mnflow.mfda.cad.dld.theme.multistage import DLD
```



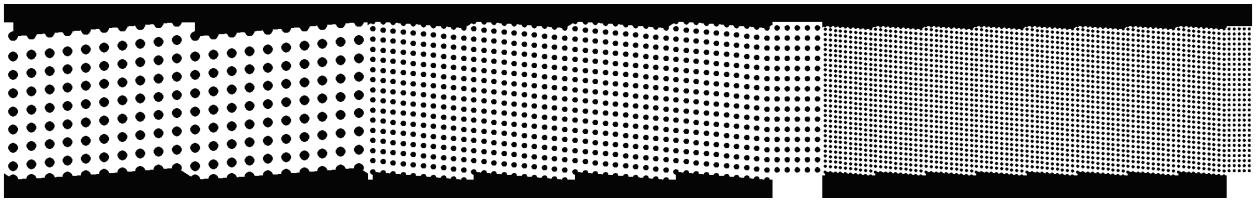
```
dld=DLD(
  config={
    'd_c':[18,10,5],
    'Np':10,
    'num_unit':2,
  },
)
```

Listing 24: Benchmark: Theme: multistage.

3.3 Condenser-and-sorter design theme

For running these examples, the condenser-and-sorter theme needs to be loaded as:

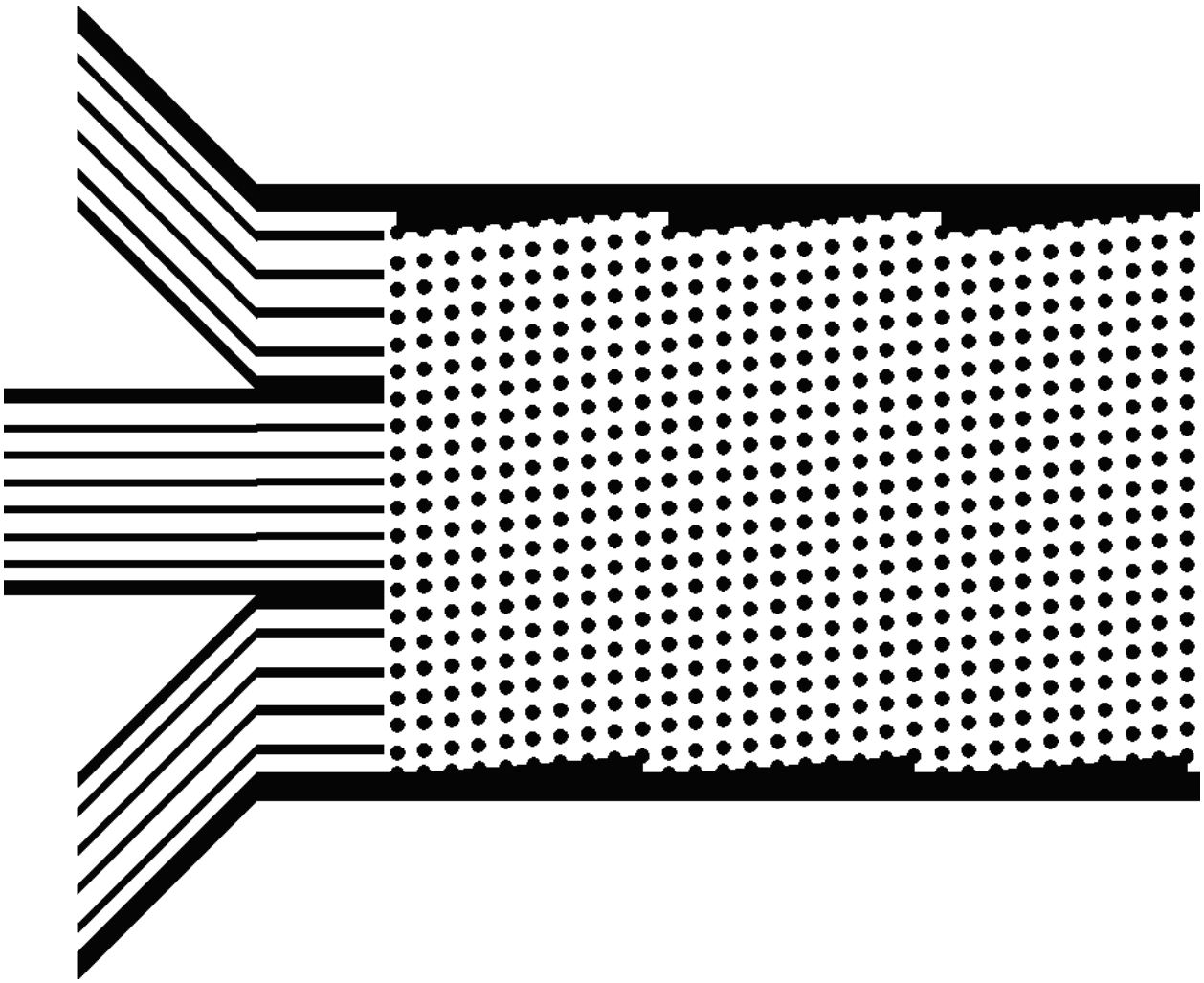
```
from mnflow.mfda.cad.dld.theme.condenser_sorter import DLD
```



```
dld=DLD(
  config={
    'd_c':[18,10,5],
    'Np':10,
    'num_unit':[2,4,8],
  },
)
```

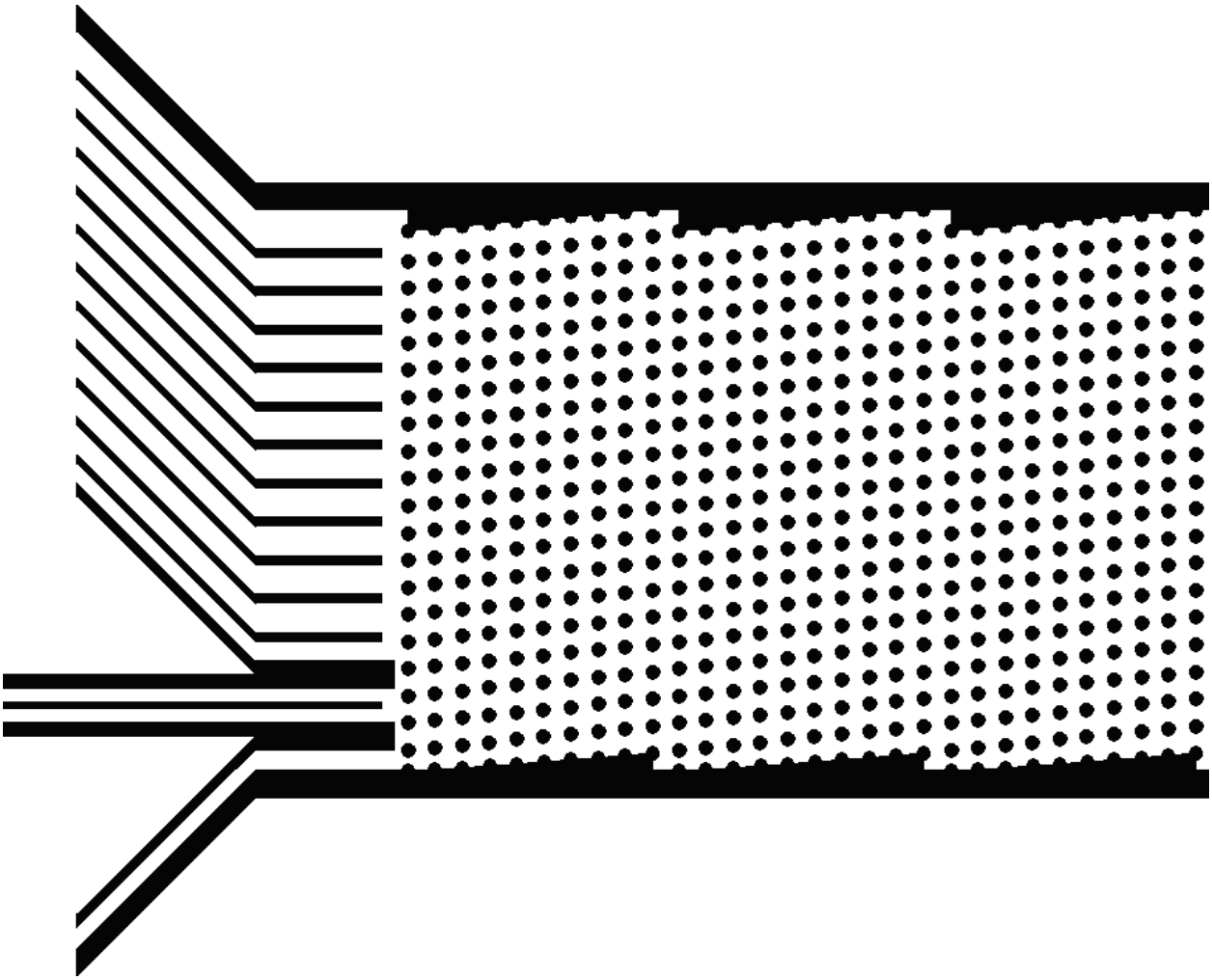
Listing 25: Benchmark: Theme: condenser-and-sorter.

3.4 Multi-branch inlet



```
dld=DLD(
  d_c=5,
  config_multi_inlet={
    'bar_dims':[5, 200],
    'num_branch':3,
  },
  Np=10,
  Nw=20,
  num_unit=3,
)
```

Listing 26: Benchmark: condenser with multi-inlet.



```
dld=DLD(
  d_c=5,
  config_multi_inlet={
    'bar_dims':[5, 200],
    'width_nondim':[0.1, 0.1, 0.8],
    'lst_config_extension':{
      'bar_len':100,
      'margin_top':0,
      'margin_down':10,
    },
  },
  Np=10,
  Nw=20,
  num_unit=3,
)
```

Listing 27: Benchmark: condenser with multi-inlet with non-uniform widths.

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