Supplementary Information for Enhancing Memristor Multilevel Resistance State with Linearity Potentiation via Feedforward Pulse Scheme

Zhuo Diao[1*], Ryohei Yamamoto[1], Meng Zijie[1], Tetsuya Tohei[1], Akira Sakai[1*]

[1*]Graduate School of Engineering Science, Osaka University, 1-3 Machikaneyama-Cho, Toyonaka, 560-8531, Osaka, Japan.

*Corresponding author(s). E-mail(s): diao.zhuo.es@osaka-u.ac.jp; sakai@ee.es.osaka-u.ac.jp;

We utilize a four-terminal TiO_{2-x} device to fabricate a bulk-switching memristor. The RS mechanism of the bulk-switching device can be explained by the transport processes of oxygen vacancies (Vo^{+2}). During the write process shown in Fig. 1(c), positively charged oxygen vacancies drift and diffuse towards or away from the electrodes with the applied V_w, forming Vo^{+2} domains of varying sizes around each electrode. As V_w increases, the expansion of the Vo^{+2} domains leads to a gradual approach to a low resistance state (LRS) in the devices [Fig. 1(e)]. During the read process, models such as tunneling junctions and Schottky junctions can explain the conductive relationship between Vo^{+2}. At this point, the contact path between terminals depends on the area of the Vo^{+2} domain, which can be incrementally controlled by different write pulses.

Fig. S1 illustrates the Vo^{+2} distribution captured through optical micrographs. Due to electrochromism, regions with Vo^{+2} appear dark, while the typical TiO_2 surface exhibits a lighter color. During the depression and potentiation processes, the device undergoes -14 V and +14 V write process, respectively, over a duration of 300 s. A difference map was generated by aligning the images using image registration techniques and subtracting the pixels near the resistance-switching region. We observe that the application of voltages to specific electrodes results in the accumulation of Vo^{+2} at the corners of the electrodes. The movement of Vo^{+2} is confined to the vicinity of the electrodes, allowing its distribution to expand or contract, thereby controlling the size

of the conduction path. This implementation enables precise resistance adjustments at each level, achieving the analog functionality required for advanced applications.

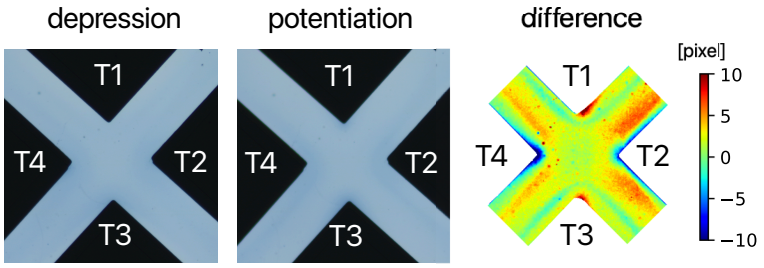

Fig. S1 Optical micrographs showing a four-terminal TiO_{2-x} device after the depression and potentiation process. The difference map between depression and potentiation optical micrographs is also illustrated.

During the calculation of v_d and v_p, we also observed that increasing the number of multilevel resistance settings in the device leads to a deterioration in the linearity of resistance updates. To quantify the programming error under various multilevel resistance configurations, we introduced the Non-Linearity Factor (NLF) metric:

$$\mathrm{NLF} = \frac{\Sigma_{j=1}^{n} |r_{a,j} - r_{i,j}|}{r_{max} - r_{min}} \tag{1}$$

where r_i and r_a represent the ideal and actual normalized multilevel resistance update curves, respectively, and n denotes the total number of pulse events.

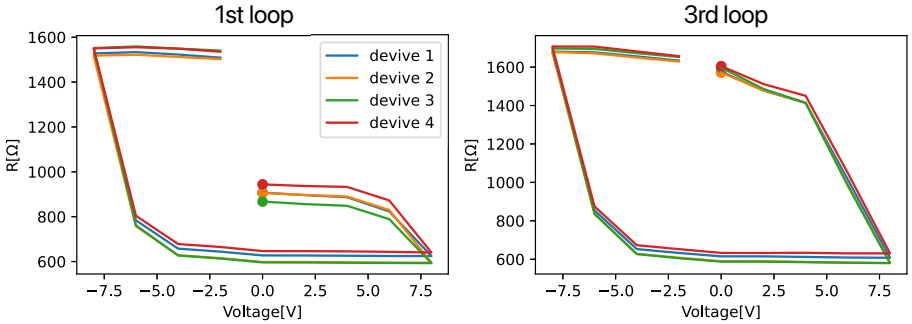

Fig. S2 The comparison of device to device variation on TiO_{2-x}-based resistive switching layer. Three loop protocols shown in Fig. 1d are conducted in a vacuum environment using different four-terminal TiO_{2-x} devices on one sample.

Fig. S2 illustrates the resistive switching characteristics of 4 devices on the same sample. This device has a TiO_{2-x} film thickness of 60 nm. The Pt electrodes in this sample are deposited via DC sputtering, and the patterning is performed with a maskless exposure system. Defining the resistance state after applying -8V as HRS and after applying 8V as LRS, the initial resistance, LRS, and HRS among different devices are

represented by their average values and standard deviations as 828.8 ± 29.7 Ω, 599.5 ± 21.1 Ω, and 1691.0 ± 11.9 Ω, respectively. This type of bulk-type memristor tends to have a good device-to-device variation since the resistance change based on the 2D distribution of VO^{2+} is deterministic.

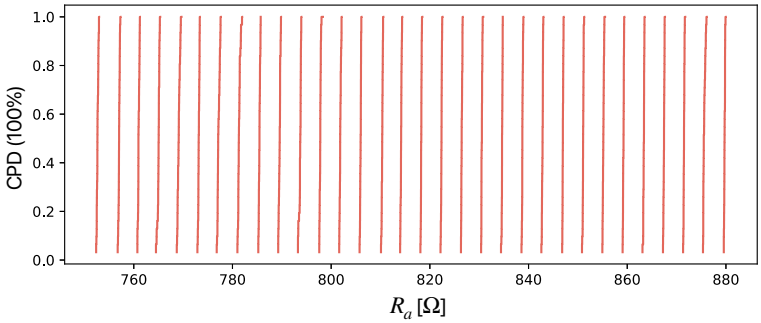

Fig. S3 Cumulative probability density(CPD) plot on configuring 32 program levels on depression process using feedforward pulse scheme.

The reliability of resistance values for each 32 multi-level resistance setting depression process is validated by the cumulative probability density(CPD) plot shown in Fig. S3. Each program level is vertically distributed, confirming the high reliability of the resistance values.

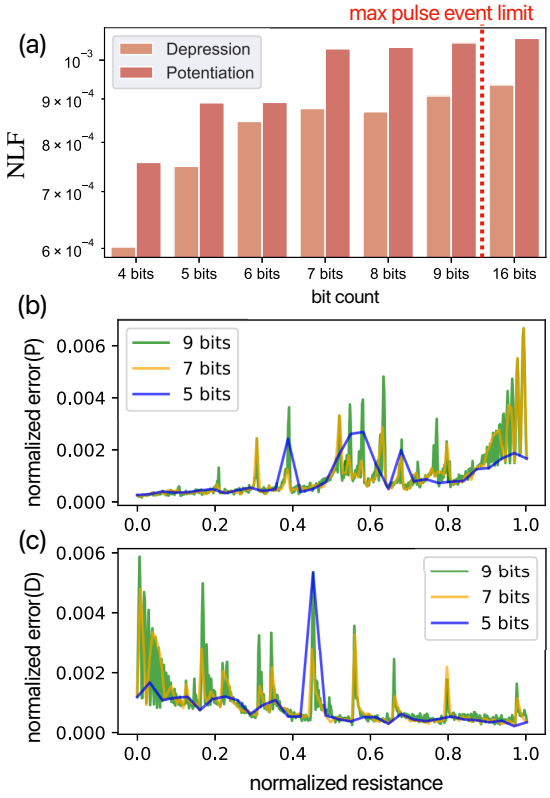

Fig. S4 (a) Non-linearity factor(NLF) depending on resistance level count. Normalized resistance error ($|r_i - r_a|$) depending on the normalized resistance level value for (b) Potentiation and (c) Depression processes.

Fig. S4(a) illustrates the NLF for devices with 4, 5, 6, 7, 8, 9, and 16 bits of analog states. As NLF values shown in Fig. S4(a), the error in potentiation processes is greater than in depression processes. This could be due to asymmetrical RS characteristics. With the same absolute write voltage, the control precision of Vo^{2+} movement during potentiation is lower than during depression within the resistance range we set.

As the number of bits increases, the NLF saturates at approximately 0.0009 for depression and 0.001 for potentiation processes. In the case of potentiation, as a worst-case scenario, the error sum in setting each resistance level corresponds to roughly 0.1% of the dynamic range. For instance, a 16-bit analog memristor requires a resolution of $1/2^{16}$ of the dynamic range, while the observed NLF of 0.001 will limit the number of programable resistance levels to less than 1000. Nevertheless, our device can successfully implement a 512 program-level division.

We further analyzed the normalized error for each resistance level by calculating the average of $|r_i - r_a|$. Fig. S4(b) and (c) depict the relationship between normalized resistance and normalized error for the potentiation and depression processes, respectively. Most of the errors are concentrated around the HRS region (normalized

resistance = 1) during the potentiation and around the LRS region (normalized resistance = 0) during the depression. The cause of errors in these regions may be due to the Joule heating effect. Write voltage will heat and raise the temperature. This phenomenon leads to a worse performance in retention [Fig. S5]. Additionally, there are several jumping error peaks in other regions. These errors occur because when the resistance reaches a certain threshold, the system switches to a different V_w, causing a sudden change in the write pulse value. This abrupt transition results in a large resistance change that overshoots the target resistance level.

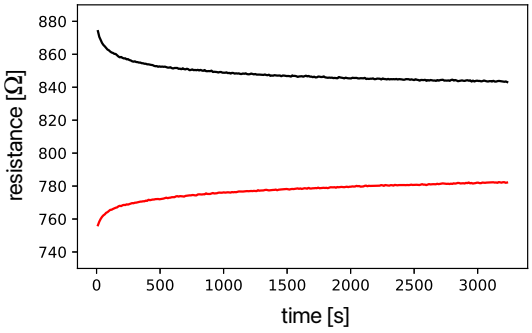

Fig. S5 The retention characteristic of HRS(black) and LRS(red) with 100 mV read voltage and ±14V write voltage.

Since the retention time issue is attributed to the Joule heating effect, it can be mitigated by reducing the operating current in the future. We also observed that applying higher write voltages during potentiation or depression results in improved retention performance. To leverage this phenomenon more effectively, further studies are needed to investigate the mechanism of dopant ion drift within the device during bulk switching. Additionally, retention-induced value drift can be reconfigured through in-memory training techniques, providing a potential solution to maintain computational accuracy.

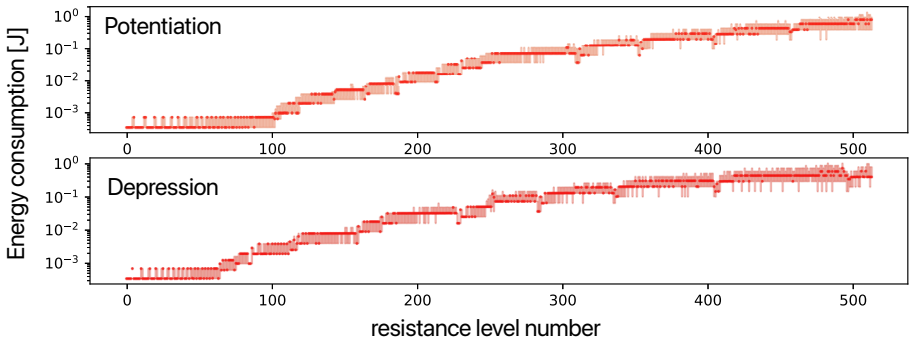

Fig. S6 The energy consumption characteristic for potentiation and depression at each 512 resistance levels.

The power consumption per program level, as shown in Fig. S6, appears high because we use 15 μm-sized devices and apply a large voltage of 7 V for program-level configuration. To reduce power consumption, our future goal is to develop integrated devices with smaller feature sizes. By scaling the device down to the nanometer level, not only can we reduce the current, but the movement of oxygen vacancies will become easier to drive. At this stage, we can lower the write voltage and shorten the write pulse duration. Considering both the current-to-area size ratio and the change in voltage application protocol, integrating devices at scales of a few hundred nanometers could reduce energy consumption to the order of 10^{-6}.